UM7106/07A/07B

3 1/2 Digit A/D Converter

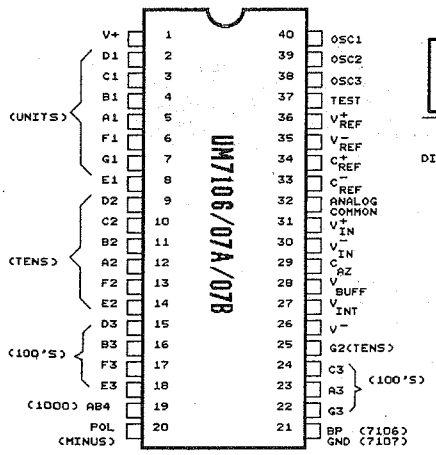
Features

- Guaranteed zero reading with zero input
- True polarity indication for precision null detection
- Low noise
- Convenient 9V battery operation
- Low power operation-10mW
- High Impedance CMOS differential inputs $10^{12}\Omega$
- True differential input and reference
- Direct display drive for UM7106 LCD, UM7107A/B LED
- No additional active components required
- Low linearity error: guaranteed less than 1 count
- Internal reference with low temperature drift
- Applications: digital panel meters, digital multimeters, thermometers, capacitance meters, pH meters, photometers, etc.
- 40-pin DIP package

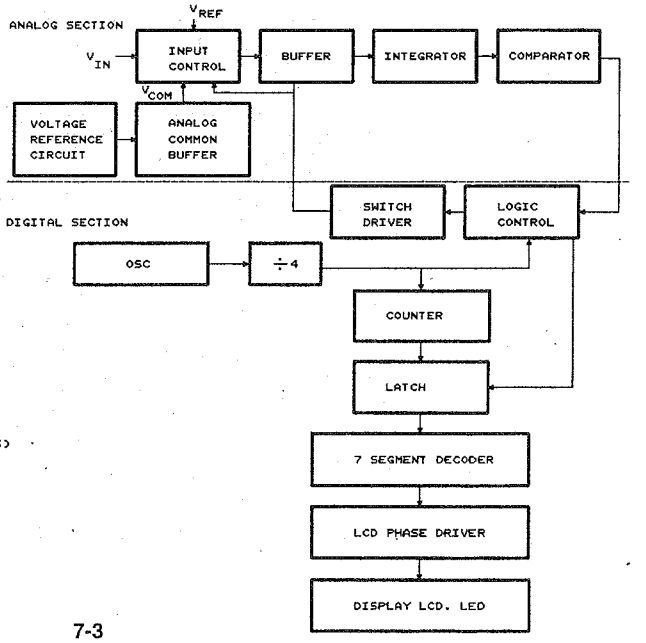
General Description

The UM7106 and UM7107A/B are high performance, low power 3 1/2 digit A/D converters. All the necessary active devices are contained in a single CMOS IC, including a seven-segment decoder, display driver, voltage reference, and clock. UM7106 is designed to interface with a liquid crystal display (LCD) and UM7107A/B will directly drive an instrument sized light emitting diode (LED) display. The UM7106 and UM7107A/B bring together a combination of high accuracy, versatility and economy. High accuracy, like auto-zero to less than 100 μV for 2.00V full-scale measurement, or 10 μV for 200.0 mV full-scale measurement, input bias current of 10 pA max, and rollover of less than one count. The versatility of true differential input and voltage reference is useful in systems such as strain gauges or bridge-type tranducers.

Pin Configuration



Block Diagram



A/D Converter

Absolute Maximum Ratings*

Supply Voltage (V+ to V-) 15V
Analog Input Voltage (either input) . . . . . V+ to V–
Reference Input Voltage (either input) . . . . V+ to V–
Clock Input . . . . . Test to V+
Power Dissipation 800mW
Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -55°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . .300°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Unless otherwise noted, specifications apply to UM7106 at V_{supply} (V^+ to V^-) = 9.0V, and UM7107A/B at V_{supply} (V^+ to V^-) = 10.0V

T_A = 25°C, f clock = 48 KHz, UM7106 is tested in the CKT of Fig 8, UM7107A/B is tested in the CKT of Fig 9.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Zero input Reading	–	-000.0	±000.0	+000.0	Digital Reading	V_{in} = 0.0V Full Scale = 200.0mV
Ratiometric Reading	–	999	999/1000	1000	Digital Reading	V_{in} = V_{ref} V_{ref} = 100.0mV
Linearity (Max. Deviation From Best Straight Line Fit)	–	-1	±0.2	+1	Counts	Full Scale 200.0 mV or 2.000V
Noise	V_N	–	15	–	μV	V_{in} = 0V Full Scale 200.0mV
Leakage Current Input	I_{LEAK}	–	1	10	PA	V_{in} = 0V
Zero Reading Drift	–	–	0.2	1	μV/°C	V_{in} = 0 0° < T_A < 70°C
Scale Factor Temp Coeff	–	–	1	5	ppm/°C	V_{in} = 199.0mV 0° < T_A < 70°C
Analog Common Voltage (With Respect to Positive Supply)	$V_{ANA-COM}$	2.7	3.0	3.3	V	25KΩ Between Common and Positive Supply
Temp Coeff of Analog Common	–	–	20	50	ppm/°C	25KΩ Between Common and Positive Supply

DC Electrical Characteristics (continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Current (Doesn't Include LED and Com. Current)	I_{DD}	–	0.8	1.8	mA	V_{in} = 0
UM7106 Only, Pk-Pk Segment Drive Voltage	V_{LCDS}	4	5	6	V	
UM7106 Only, Pk-Pk Back Plane Drive Voltage	V_{LCDS}	4	5	6	V	
UM7107A/B Only, Segment Sinking Current (Except Pin 19)	I_{LED}	5	8.0	–	mA	V_{supply} = 5.0V Segment Voltage = 3V
UM7107A/B Only, Segment Sinking Current (Pin 19 Only)	I_{LED}	10	16	–	mA	V_{supply} = 5.0V Segment Voltage = 3V
Rollover Error	–	–1	±0.2	+1	Counts	$V_{in}^{-} = V_{in}^{+}$ = 200.0mV
Common-mode Rejection Ratio	–	–	50	200	μV/V	V_{cm} = ±1V_{in}, V_{in} = 0V Full-scale = 200.0mV

Pin Description

Pin No.	Designation	Description
1	V+	Positive supply voltage
2	D1	Activates the D section of the units display
3	C1	Activates the C section of the units display
4	B1	Activates the B section of the units display
5	A1	Activates the A section of the units display
6	F1	Activates the F section of the units display
7	G1	Activates the G section of the units display

Pin Description (continued)

Pin No.	Designation	Description
8	E1	Activates the E section of the units display
9	D2	Activates the D section of the units display
10	C2	Activates the C section of the tens display
11	B2	Activates the B section of the tens display
12	A2	Activates the A section of the tens display
13	F2	Activates the F section of the tens display
14	E2	Activates the E section of the tens display
15	D3	Activates the D section of the hundreds display
16	B3	Activates the B section of the hundreds display
17	F3	Activates the F section of the hundreds display
18	E3	Activates the E section of the hundreds display
19	AB4	Activates both halves of the 1 in the thousands display
20	POL (MINUS)	Activates the negative polarity display
21	BP GND	LCD Backplane drive output (UM7106) Digital Ground (UM7107A), but keep floating for UM7107B
22	G3	Activates the G section of the hundreds display
23	A3	Activates the A section of the hundreds display
24	C3	Activates the C section of the hundreds display
25	G2	Activates the G section of the tens display
26	V^-	Negative power supply voltage
27	VINT	Integrator output. Connection point for integration capacitor
28	VBUFF	Integration resistor connection. Use 47KΩ for a 200mV full-scale range and 470KΩ for 2V full-scale range

Pin Description (continued)

Pin No.	Designation	Description
29	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47μF capacitor for 200mV full-scale, and a 0.047μF capacitor for 2 volt full-scale
30	V_{IN}^-	The analog low input is connected to this pin
31	V_{IN}^+	The analog high input signal is connected to this pin
32	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply
33	C_{REF}^-	See pin 34
34	C_{REF}^+	A 0.1μF capacitor is used in most applications. If a large common-mode voltage exists (for example the V_{IN}^- pin is not at analog common), and a 200 mV scale is used, a 1.0μF capacitor is recommended which will hold the rollover error to 0.5 count
35	V_{REF}^-	See pin 36
36	V_{REF}^+	This analog input is required to generate a full-scale output (1,999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full-scale. Place 1.00 volt between pins 35 and 36 for 2 volt full-scale
37	TEST	Lamp test. When pulled high (to V^+), all segments will be turned on and the display should read-1888. It may also be used as a negative supply for externally generated decimal points
38	OSC3	See pin 40
39	OSC2	See pin 40
40	OSC1	Pins 40, 39 & 38 make up the oscillator section. For a 48 KHz clock (3 readings per second), connect pin 40 to the junction of a 100KΩ resistor and a 100 pF capacitor. The 100KΩ resistor is tied to pin 39 and the 100pF capacitor is tied to pin 38

Functional Description

An input signal to be measured is applied to the integrating capacitance for a fixed time as determined by a clock counter. The accumulated charge will be proportional to the input signal for a fixed clock rate and constant current. The resulting integral is returned to zero by integrating a reference signal of polarity opposite that of the input signal. The length of time required for the integrator to return to zero, as measured with the clock counter to display at output, is proportional to the average magnitude of the input signal over the integration period.

a. Analog Section

Fig. 1 shows the block diagram of the Analog Section for UM7106 and UM7107A/B. Each measurement cycle is divided into three parts. They are: (1) Auto-zero [A-Z] (2) Signal integrated [INT] (3) Deintegrated [DE].

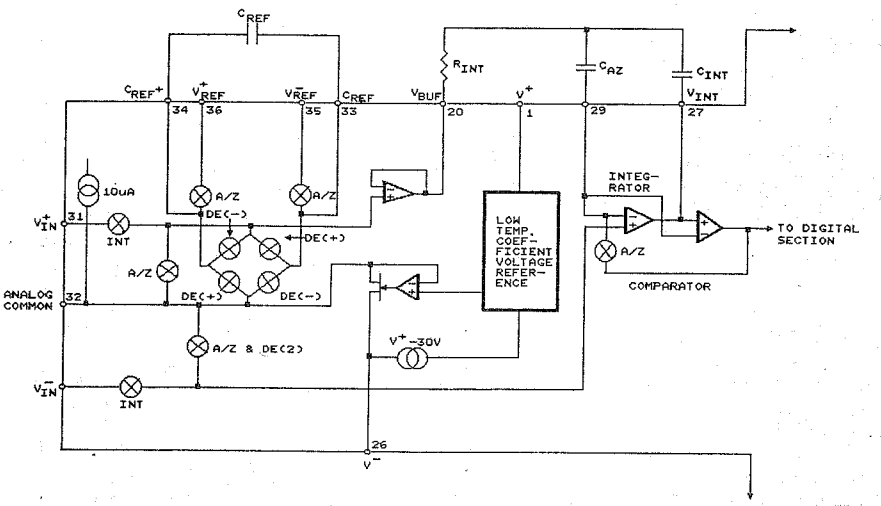


Figure 1. UM7106/07A/07B Analog Section

1. Auto Zero Phase

During Auto-Zero, three things happen:

(1) Input high and low are disconnected from the PIN and shorted to analog COMMON.
(2) The reference capacitor is charged to the reference voltage.
(3) A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator and comparator.

2. Signal Integrate Phase

During signal integrate, the auto zero loop is opened, the internal short is removed, and the internal inputs high and low are connected to the external pins. The converter then integrates the differential voltage between input high and input low for a fixed time (1000 counts). At the end of this phase, the polarity of the integrated signal is determined.

3. De-Integrate Phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to Analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required to return to zero is proportional to the input signal. Specifically, the digital reading displayed is $1000\ (\frac{Ain}{Vref})$.

b. Digital Section

Fig. 2, Fig. 3 and Fig. 4 show the digital section for the UM7106 and UM7107A/B, respectively. In the UM7106, the internal digital ground is generated from a 6.2 volt Zener diode and a large p-channel follower. This supply is made stiff to absorb the relatively large capacitive current when the back plane (BP) is switched. The BP frequency is the clock frequency divided by 800. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases, negligible DC voltage exists across the segments.

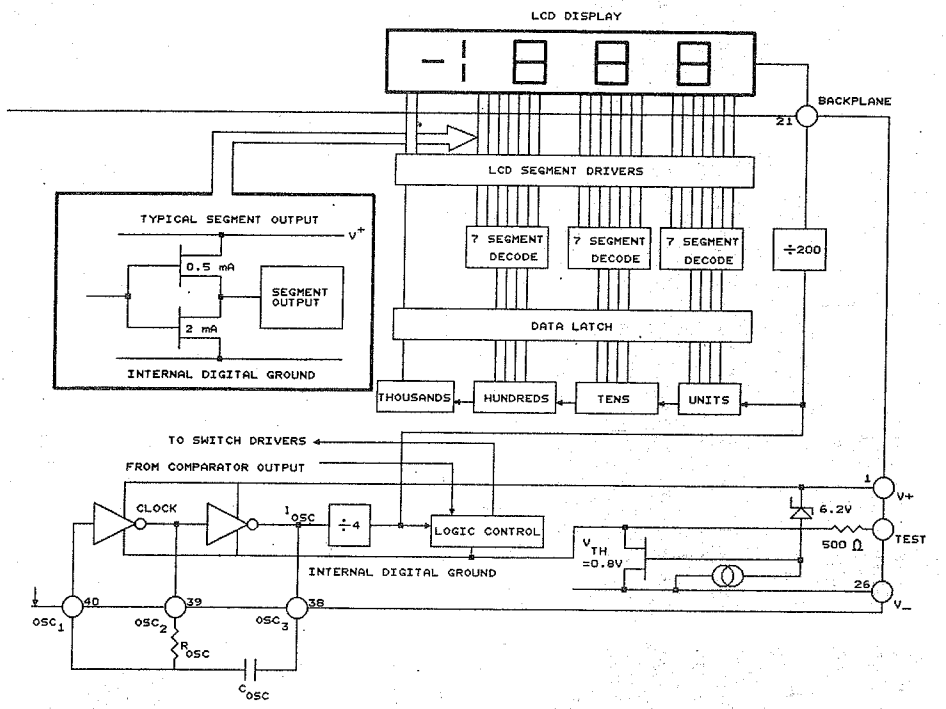


Figure 2. UM7106 Digital Section

Fig. 3 is the Digital Section of the UM7107A. It is identical to Fig. 2 except the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 mA to 8 mA. Pin 19 must sink current twice the drive capability.

Fig. 4 is the Digital Section of the UM7107B. It is similar to UM7107A except UM7107B provides an internal digital ground (same as UM7106), hence the user does not need to provide an external digital ground for UM7107B and keep pin 21 floating. It is suggested that user place a 120 Ω resistor between V^+ and common anode LED to limit the current into UM7107B to gain better performance and save energy.

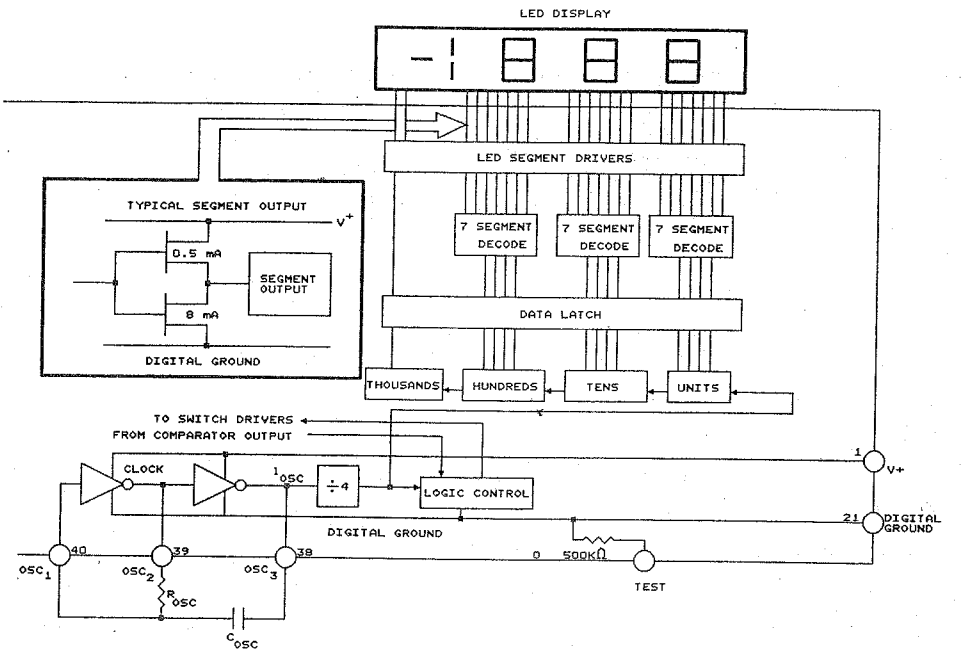


Figure 3. UM7107A Digital Section

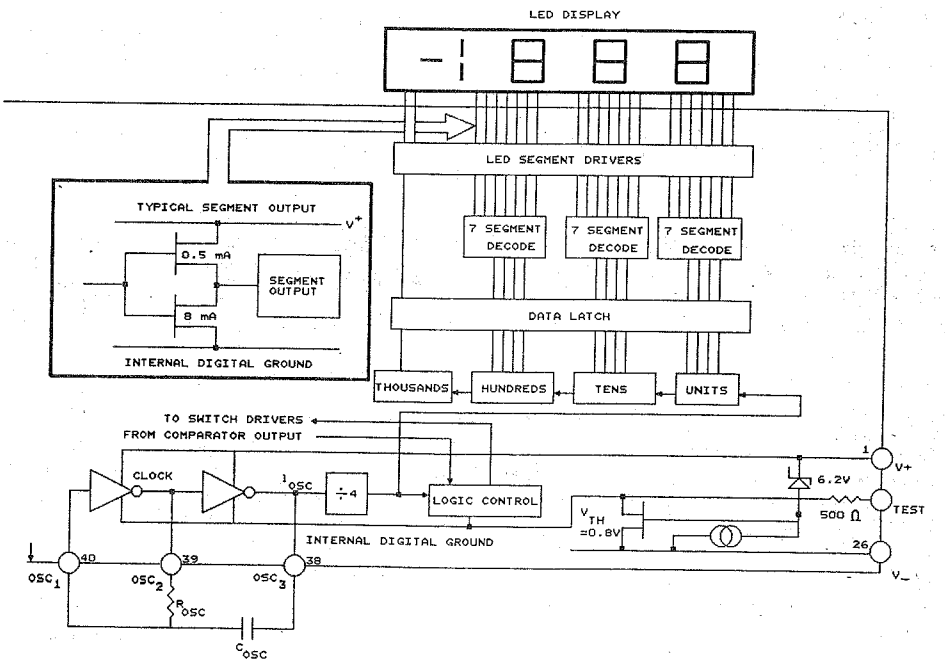
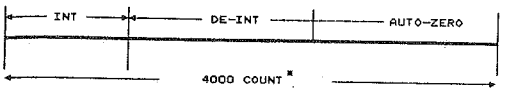


Figure 4. UM7107B Digital Section

System Timing

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phase. These are: signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference de-integrate. This makes complete measure cycles of 4000 (16000 clock pulses) independent of input voltage.



* Note: Actually, the total measurement cycle is 4001 counts for measured values less than 2000 counts. The measurement cycle becomes 4000 counts for overflow measurement.

Clock Circuit:

UM7106/07A/07B may use the following three clocking methods:

1. An external oscillator connected to pin 40.
2. A crystal between pin 39 and pin 40.
3. An RC oscillator using all three pins (pin 38, 39 & 40).

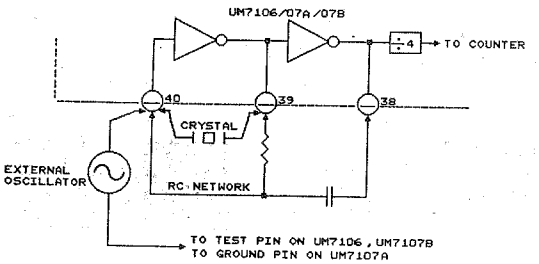


Figure 5. Clock Circuit

To achieve maximum rejection of 50/60 Hz pick up, the signal integrate cycle should be a multiple of 50/60 Hz. The following table describes the selection of oscillator frequencies for 50 or 60Hz respectively.

	Oscillator Frequencies
50 Hz	..40 KHz, 50 KHz, 66 2/3 KHz, 100 KHz...
60 Hz	..33 1/3 KHz, 40 KHz, 48 KHz, 60 KHz, 80 KHz, 100 KHz....

Note that 40 KHz (2.5 readings/second) will reject both 50 and 60 Hz.

Component Value Selection:

Integrating Resistor (RINT):

The buffer amplifier and integrator are designed with class A output stages with 100 μA of quiescent current each. They can supply 20 μA drive current with negligible linearity errors. RINT should be large enough to remain in linear region but small enough to reduce the leakage current on the PC board. For 200mv full scale, RINT is 47KΩ ; 2 volt full scale needs a 470KΩ RINT.

Integrating Capacitor (CINT):

CINT should be chosen to give the maximum voltage swing without causing the saturation of integrator output swing. According to the superior temperature coefficient — 20ppm/ °C of analog common will be normally used as the differential voltage reference. It is fine for a nominal ±2V full scale integrator output swing. For three readings/second (48KHz clock), a 0.22μF capacitor is suggested.
If a different oscillator frequency is used, CINT must be changed in inverse proportion to maintain the nominal ±2V full scale integrator output swing.
An additional requirement of CINT is that CINT must have low dielectric absorption to minimize rollover error. Polypropylene capacitors give undetectable errors at reasonable cost.

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Reference Voltage Capacitor (CREF):

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on CREF. A 0.1μF capacitor gives good performance when V_{IN}^- is tied to analog common. If a large analog common voltage exists (V_{REF}^- unequal analog common) and a 200.0mV scale is used, a larger value is required to prevent rollover error. Generally 1.0μF will hold the rollover error to 0.5 count. In this case a mylar type dielectric capacitor is adequate.

Auto-Zero Capacitor (CAZ):

The CAZ value has some influence on system noise. The following combination is recommended:

Application	Adequate CAZ
200.0mV Full Scale	0.47μF
2.000V Full Scale	0.047μF

It is better to use a mylar type capacitor to implement CAZ.

Oscillator Components (Rosc, Cosc):

While using RC oscillator, the Rosc (between pin 39 and pin 40) should be 100KΩ and Cosc is selected from the following equation:

$$Fosc = \frac{0.45}{Rosc.\ Cosc}$$ (Rosc in MΩ, Cosc in μF)

Reference Voltage Selection:

The analog input required to generate full scale output (2000 counts) is $V_{IN} = 2\ V_{REF}$, thus:

Required Full Scale Voltage	VREF
200.0mV	100.0mV
2.000V	1.000V

However, in many applications where an A/D converter is connected to a transducer, there may exist a non-unity scale factor between the input voltage and the digital reading. For instance, a pressure transducer output is 400mV for 2000 lb/in^2, rather than dividing the input voltage by two, the VREF should be set to 200.0mV, then permit the transducer input to be used directly.

The differential voltage reference can also be used to read a digital zero when VIN is not zero. This case is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}^- and the transducer output is connected between V_{IN}^+ and analog common. The circuit is shown in Figure 6.

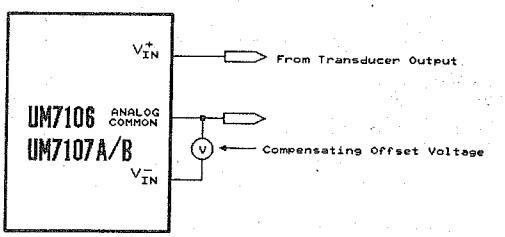

Figure 6. Circuit Used to Read a Digital Zero When VIN is not Zero.

An external reference may be added to improve temperature stability; thus, the UM7106/07A/07B devices with a lower analog common temperature drift may be used. The circuit is shown in Figure 7.

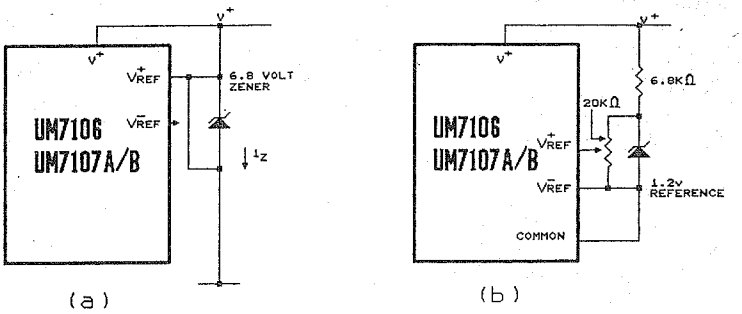

Figure 7. External Reference Voltage Circuits

Application Circuits (for reference only)

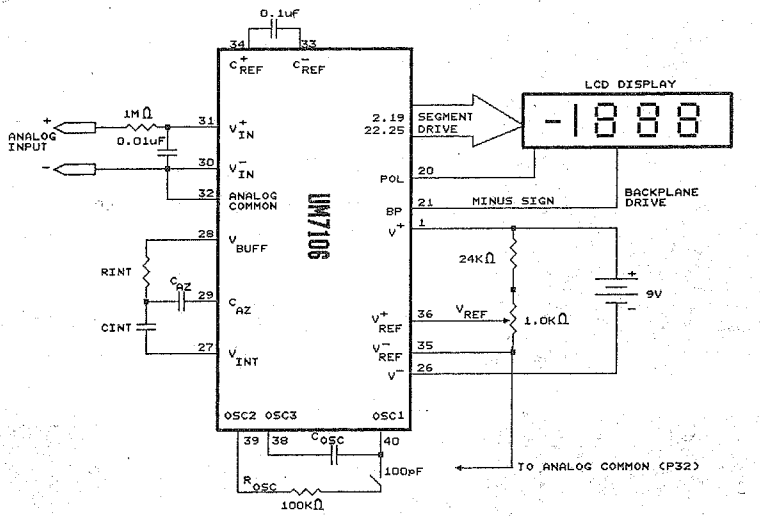

Figure 8.

Component Value	Nominal Full-Scale Voltage	
	2.000V	200.0mV
CAZ	0.047μF	0.47μF
RINT	470KΩ	47KΩ
CINT	0.22μF	0.22μF
VREF	1.000V	100.0mV

Application Circuits (continued)

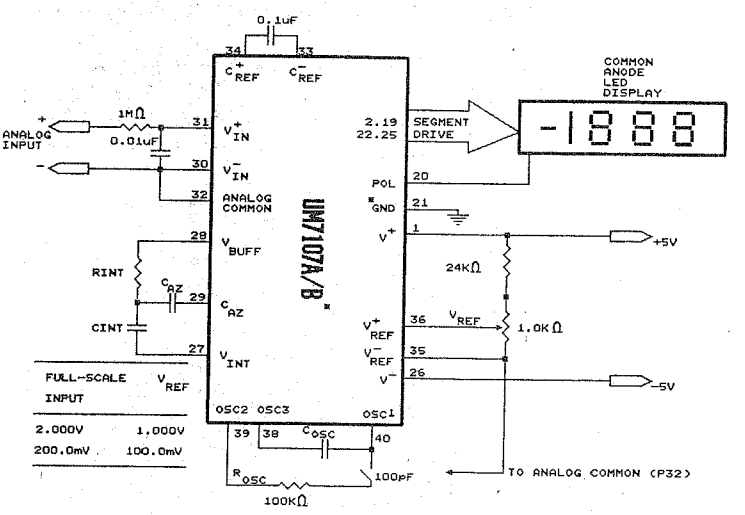

Figure 9

Component Value	Nominal Full-Scale Voltage	
	2.000V	200.0mV
CAZ	0.047μF	0.47μF
RINT	470KΩ	47KΩ
CINT	0.22μF	0.22μF
VREF	1.000V	100.0mV

* Note: For UM7107B, pin 21 must be kept floating. Place a 120 Ω resistor between V^+ and common anode LED. The digital ground of UM7107B is internally generated in order to improve PCB layout.

Ordering Information

Part No.	Package	Function
UM7106	40L DIP	LCD display
UM7107A/B	40L DIP	LED display