Data Sheet | March 13, 2006 | FN3116.9

Single 16-Channel/Differential 8-Channel, CMOS Analog Multiplexers

The DG406 and DG407 monolithic CMOS analog multiplexers are drop-in replacements for the popular DG506A and DG507A series devices. They each include an array of sixteen analog switches, a TTL and CMOS compatible digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

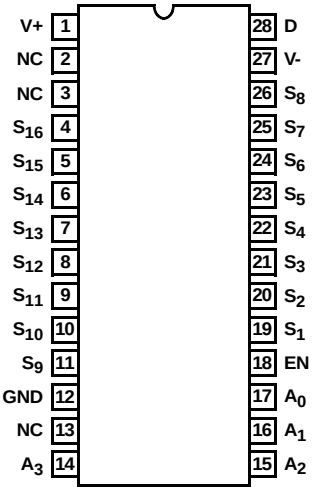
These multiplexers feature lower signal ON resistance (<100Ω) and faster transition time (t_{TRANS} < 300ns) compared to the DG506A and DG507A. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG406 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 30V_{P-P} signals when operating with ±15V power supplies.

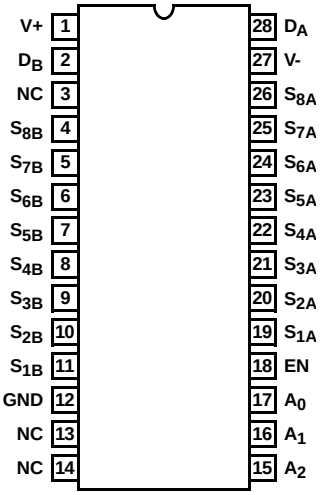
The sixteen switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range.

Pinouts

DG406 (PDIP, SOIC)
TOP VIEW



DG407 (PDIP, SOIC)
TOP VIEW



Features

- ON-Resistance (Max) 100Ω
- Low Power Consumption (P_D) . . . . . <1.2mW
- Fast Transition Time (Max) 300ns
- Low Charge Injection
- TTL, CMOS Compatible
- Single or Split Supply Operation
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Battery Operated Systems
- Data Acquisition
- Medical Instrumentation
- Hi-Rel Systems
- Communication Systems
- Automatic Test Equipment

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
DG406DJ	DG406DJ	-40 to 85	28 Ld PDIP	E28.6
DG406DJZ (See Note)	DG406DJZ	-40 to 85	28 Ld PDIP* (Pb-free)	E28.6
DG406DY	DG406DY	-40 to 85	28 Ld SOIC	M28.3
DG406DY-T	DG406DY	28 Ld SOIC Tape and Reel		M28.3
DG406DYZ (See Note)	DG406DYZ	-40 to 85	28 Ld SOIC (Pb-free)	M28.3
DG406DYZ-T (See Note)	DG406DYZ	28 Ld SOIC Tape and Reel (Pb-free)		M28.3
DG407DJ	DG407DJ	-40 to 85	28 Ld PDIP	E28.6
DG407DJZ (Note)	DG407DJZ	-40 to 85	28 Ld PDIP* (Pb-free)	E28.6
DG407DY	DG407DY	-40 to 85	28 Ld SOIC	M28.3
DG407DYZ (Note)	DG407DYZ	-40 to 85	28 Ld SOIC (Pb-free)	M28.3

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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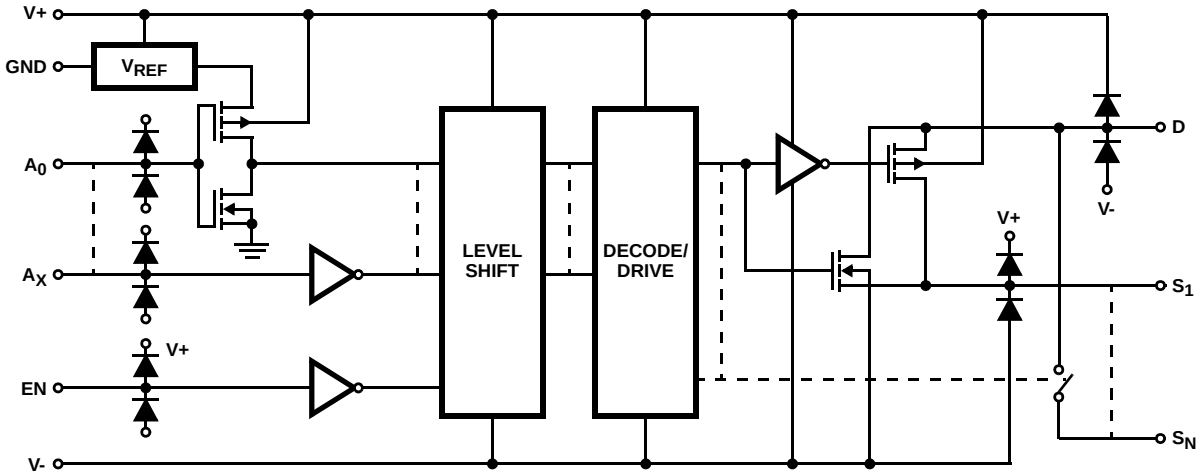
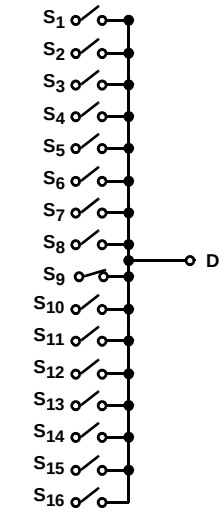
Schematic Diagram (Typical Channel)

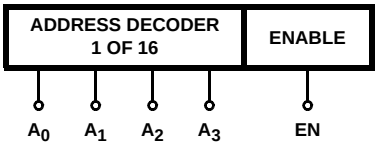


Functional Diagrams

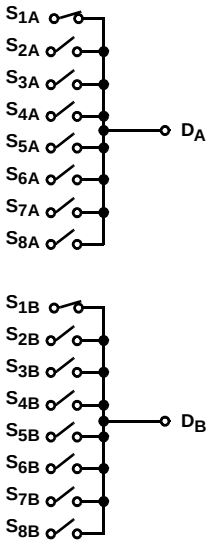
DG406



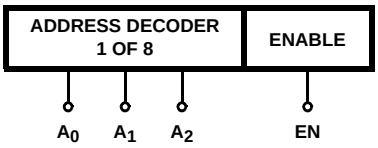
TO DECODER LOGIC CONTROLLING BOTH TIERS OF MUXING



DG407



TO DECODER LOGIC CONTROLLING BOTH TIERS OF MUXING



DG406 TRUTH TABLE

A_3	A_2	A_1	A_0	EN	ON SWITCH
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

DG407 TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic “0” = V_{AL} < 0.8V.
Logic “1” = V_{AH} > 2.4V.
X = Don’t Care.

Absolute Maximum Ratings

V+ to V- 44.0V
GND to V-. 25V
Digital Inputs, V_S, V_D (Note 1). . . . . (V-) -2V to (V+) +2V or 20mA, Whichever Occurs First
Continuous Current (Any Terminal) 30mA
Peak Current, S or D (Pulsed 1ms, 10% Duty Cycle Max) 100mA

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note1)	θ_{JA} ($^oC/W$)
PDIP Package*	60
SOIC Package	75

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range. . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(PLCC and SOIC - Lead Tips Only)
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. Signals on S_X, D_X, EN or A_X exceeding V+ or V- are clamped by internal diodes. Limit diode current to maximum current ratings.

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^oC)	(NOTE 3) MIN	(NOTE 4) TYP	(NOTE 3) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Transition Time, t_{TRANS}	(See Figure 1)	25	-	200	300	ns
		Full	-	-	400	ns
Break-Before-Make Interval, t_{OPEN}	(See Figure 3)	25	25	50	-	ns
		Full	10	-	-	ns
Enable Turn-ON Time, $t_{ON(EN)}$	(See Figure 2)	25	-	150	200	ns
		Full	-	-	400	ns
Enable Turn-OFF Time, $t_{OFF(EN)}$		25	-	70	150	ns
		Full	-	-	300	ns
Charge Injection, Q	C_L = 1nF, V_S = 0V, R_S = 0Ω	25	-	40	-	pC
OFF Isolation, OIRR	V_{EN} = 0V, R_L = 1kΩ, f = 100kHz (Note 7)	25	-	-69	-	dB
Logic Input Capacitance, C_{IN}	f = 1MHz	25	-	7	-	pF
Source OFF Capacitance, $C_{S(OFF)}$	V_{EN} = 0V, V_S = 0V, f = 1MHz	25	-	8	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$ DG406	V_{EN} = 0V, V_D = 0V, f = 1MHz	25	-	160	-	pF
DG407		25	-	80	-	pF
Drain ON Capacitance, $C_{D(ON)}$ DG406	V_{EN} = 5V, V_D = 0V, f = 1MHz	25	-	180	-	pF
DG407		25	-	90	-	pF
DIGITAL INPUT CHARACTERISTICS						
Logic High Input Voltage, V_{INH}		Full	2.4	-	-	V
Logic Low Input Voltage, V_{INL}		Full	-	-	0.8	V
Logic High Input Current, I_{AH}	V_A = 2.4V, 15V	Full	-1	-	1	µA
Logic Low Input Current, I_{AL}	V_{EN} = 0V, 2.4V, V_A = 0V	Full	-1	-	1	µA
ANALOG SWITCH CHARACTERISTICS						
Drain-Source ON Resistance, $r_{DS(ON)}$	V_D = ±10V, I_S = $\overline{+}$10mA (Note 5)	25	-	50	100	Ω
		Full	-	-	125	Ω
$r_{DS(ON)}$ Matching Between Channels, $\Delta r_{DS(ON)}$	V_D = 10V, -10V (Note 6)	25	-	5	-	%

Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^{o}C)	(NOTE 3) MIN	(NOTE 4) TYP	(NOTE 3) MAX	UNITS
Source OFF Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V, V_S = ±10V, V_D = ∓10V	25	-0.5	0.01	0.5	nA
		Full	-5	-	5	nA
Drain OFF Leakage Current, $I_{D(OFF)}$ DG406		25	-1	0.04	1	nA
		Full	-40	-	40	nA
DG407		25	-1	0.04	1	nA
		Full	-20	-	20	nA
Drain ON Leakage Current, $I_{D(ON)}$ DG406	V_S = V_D = ±10V (Note 5)	25	-1	0.04	1	nA
		Full	-40	-	40	nA
DG407		25	-1	0.04	1	nA
		Full	-20	-	20	nA
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V_{EN} = V_A = 0V or 5V (Standby)	25	-	13	30	µA
		Full	-	-	75	µA
Negative Supply Current, I-		25	-1	-0.01	-	µA
		Full	-10	-	-	µA
Positive Supply Current, I+	V_{EN} = 2.4V, V_A = 0V (Enabled)	25	-	80	100	µA
		Full	-	-	200	µA
Negative Supply Current, I-		25	-1	-0.01	-	µA
		Full	-10	-	-	µA

Electrical Specifications Single Supply Test Conditions: V+ = 12V, V- = 0V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^{o}C)	(NOTE 3) MIN	(NOTE 4) TYP	(NOTE 3) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Switching Time of Multiplexer, t_{TRANS}	V_{S1} = 8V, V_{S8} = 0V, V_{IN} = 2.4V	25	-	300	450	ns
Enable Turn-ON Time, $t_{ON(EN)}$	V_{INH} = 2.4V, V_{INL} = 0V, V_{S1} = 5V	25	-	250	600	ns
Enable Turn-OFF Time, $t_{OFF(EN)}$		25	-	150	300	ns
Charge Injection, Q	C_L = 1nF, V_S = 6V, R_S = 0Ω	25	-	20	-	pC

Electrical Specifications Single Supply Test Conditions: V+ = 12V, V- = 0V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^{O}C)	(NOTE 3) MIN	(NOTE 4) TYP	(NOTE 3) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	12	V
Drain-Source ON-Resistance, $r_{DS(ON)}$	V_D = 3V, 10V, I_S = -1mA (Note 5)	25	-	90	120	Ω
$r_{DS(ON)}$ Matching Between Channels (Note 6), $\Delta r_{DS(ON)}$		25	-	5	-	%
Source Off Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V, V_D = 10V or 0.5V, V_S = 0.5V or 10V	25	-	0.01	-	nA
Drain Off Leakage Current, $I_{D(OFF)}$						
DG406		25	-	0.04	-	nA
DG407		25	-	0.04	-	nA
Drain On Leakage Current, $I_{D(ON)}$	V_S = V_D = ±10V (Note 5)					
DG406		25	-	0.04	-	nA
DG407		25	-	0.04	-	nA
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current (I+) (Standby)	V_{EN} = 0V or 5V, V_A = 0V or 5V	25	-	13	30	µA
		Full	-	13	75	µA
Negative Supply Current (I-) (Enabled)		25	-1	-0.01	-	µA
		Full	-5	-0.01	-	µA

NOTES:

3. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
4. Typical values are for Design Aid Only, not guaranteed nor production tested.
5. Sequence each switch ON.
6. $\Delta r_{DS(ON)}$ = ($r_{DS(ON)}$(Max) - $r_{DS(ON)}$(Min)) ÷ $r_{DS(ON)}$ average.
7. Worst case isolation occurs on channel 8B due to proximity to the drain pin.

Test Circuits and Waveforms

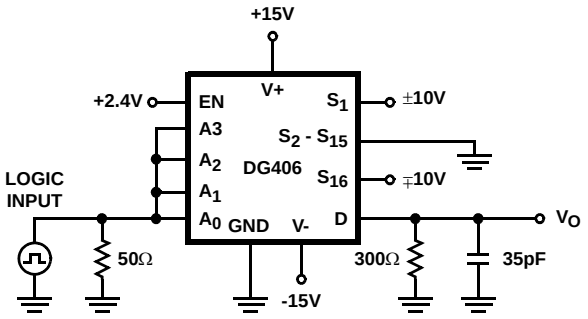


FIGURE 1A. DG406 TEST CIRCUIT

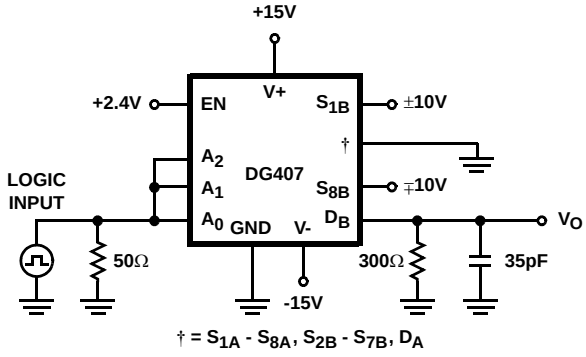


FIGURE 1B. DG407 TEST CIRCUIT

Test Circuits and Waveforms (Continued)

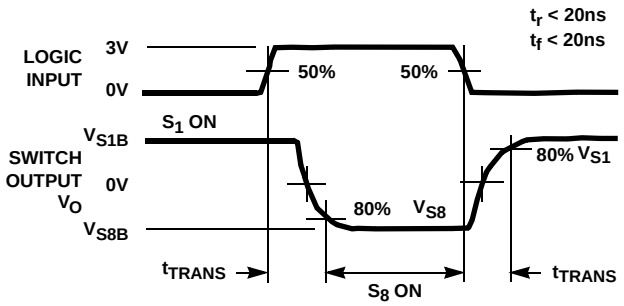


FIGURE 1C. MEASUREMENT POINTS

FIGURE 1. TRANSITION TIME

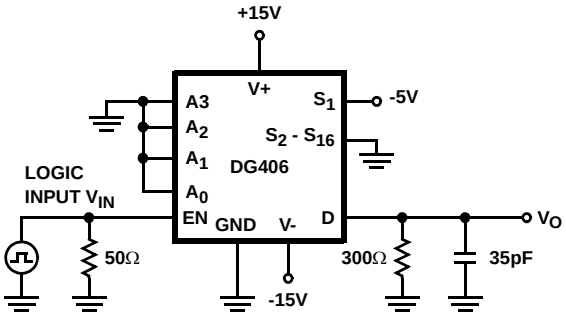


FIGURE 2A. DG406 TEST CIRCUIT

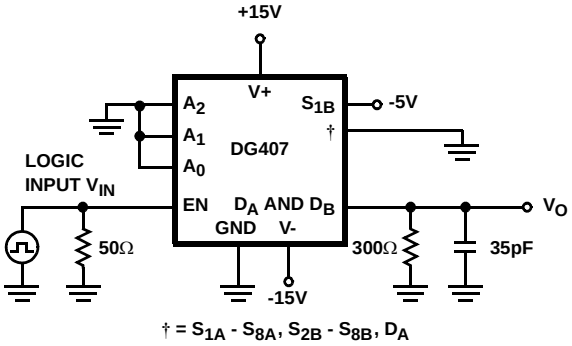


FIGURE 2B. DG407 TEST CIRCUIT

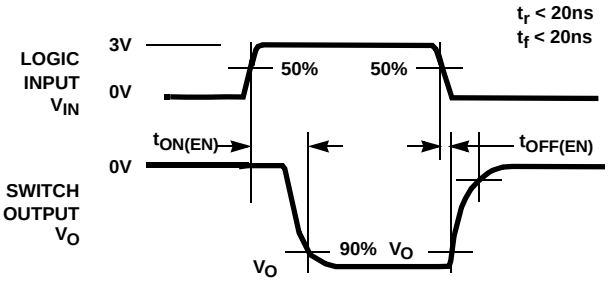


FIGURE 2C. MEASUREMENT POINTS

FIGURE 2. ENABLE SWITCHING TIMES

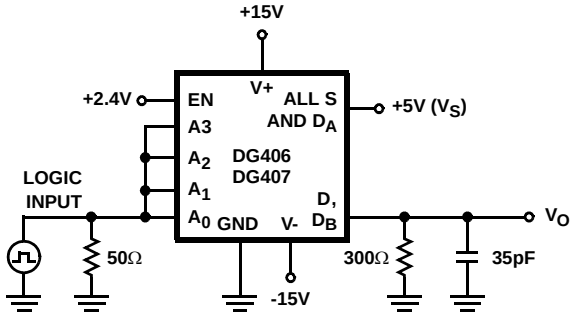


FIGURE 3A. TEST CIRCUIT

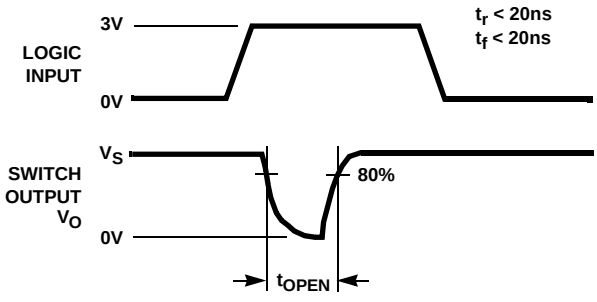


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. BREAK-BEFORE-MAKE INTERVAL

Typical Performance Curves

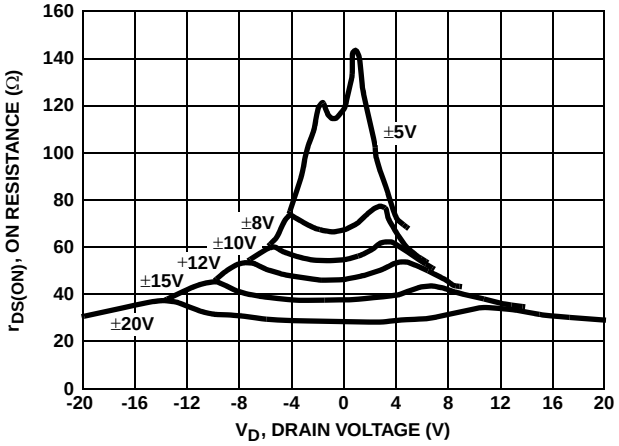


FIGURE 4. $r_{DS(ON)}$ vs V_D AND SUPPLY

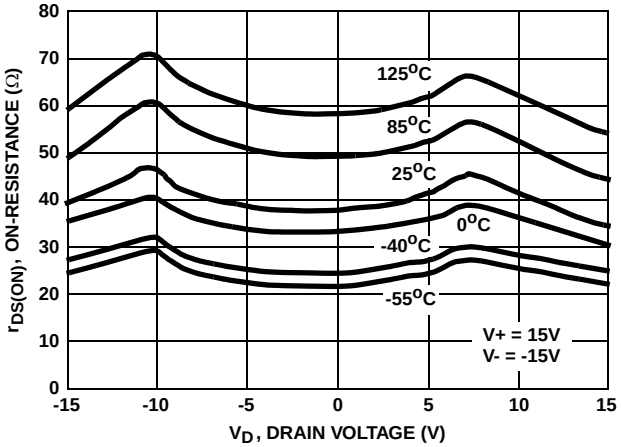


FIGURE 5. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

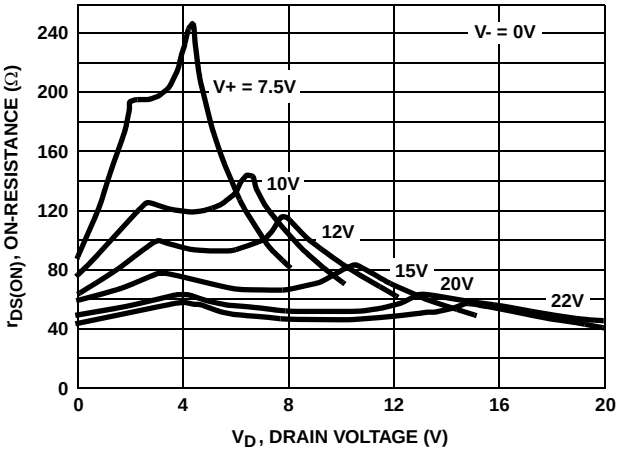


FIGURE 6. $r_{DS(ON)}$ vs V_D AND SUPPLY

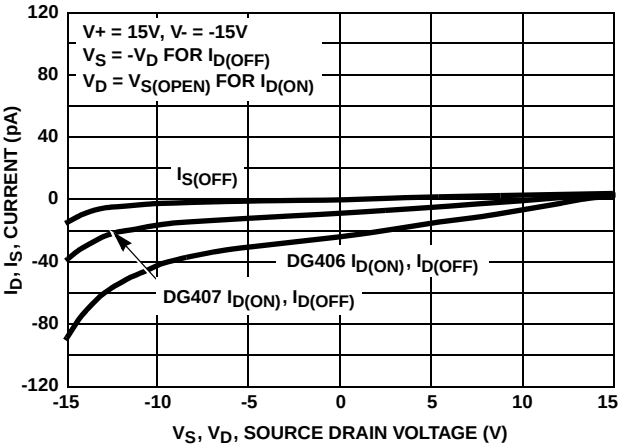


FIGURE 7. I_D, I_S LEAKAGE CURRENTS vs ANALOG VOLTAGE

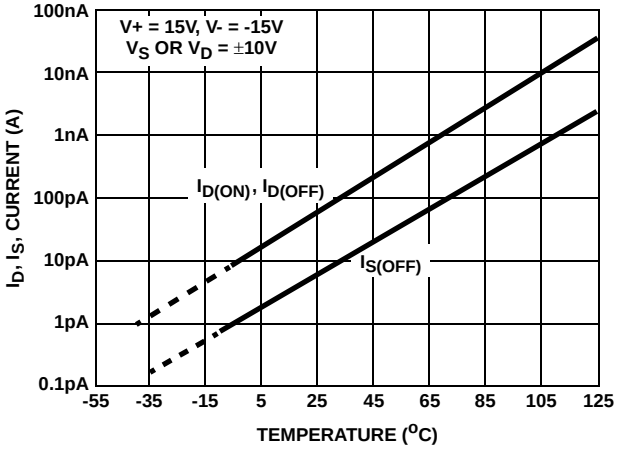


FIGURE 8. I_D, I_S LEAKAGE vs TEMPERATURE

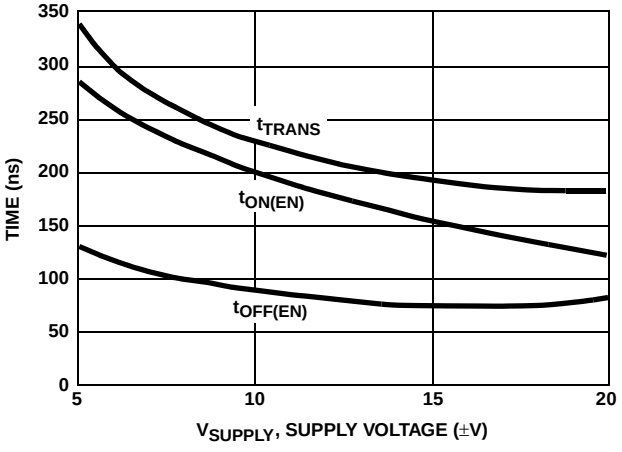


FIGURE 9. SWITCHING TIMES vs BIPOLAR SUPPLIES

Typical Performance Curves (Continued)

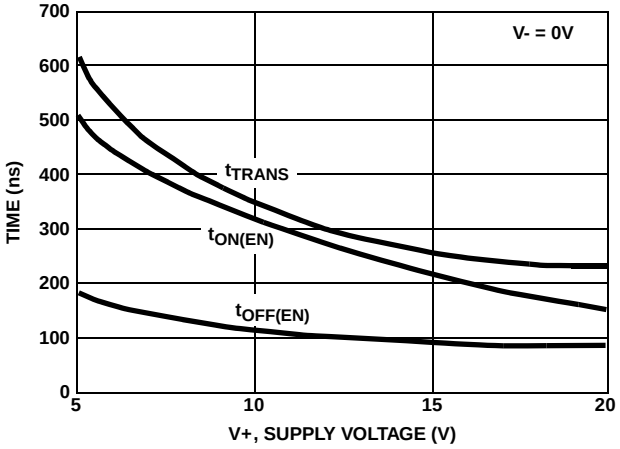


FIGURE 10. SWITCHING TIMES vs SINGLE SUPPLY

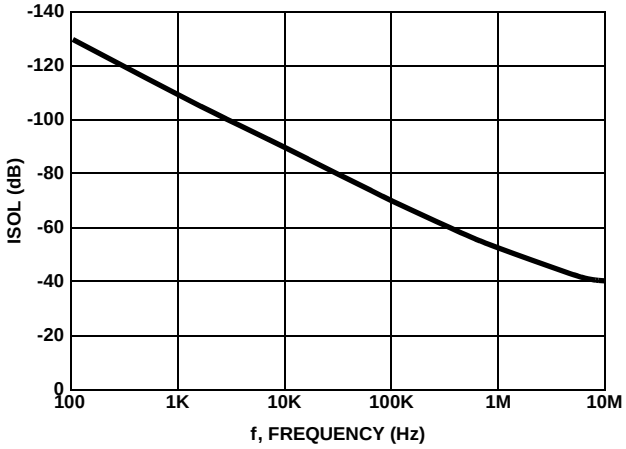


FIGURE 11. OFF ISOLATION vs FREQUENCY

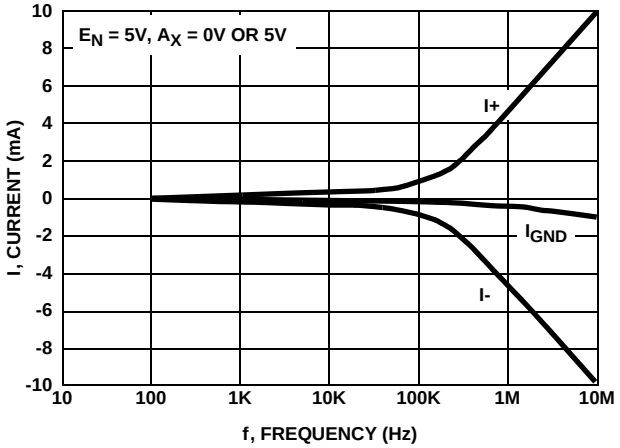


FIGURE 12. SUPPLY CURRENTS vs SWITCHING FREQUENCY

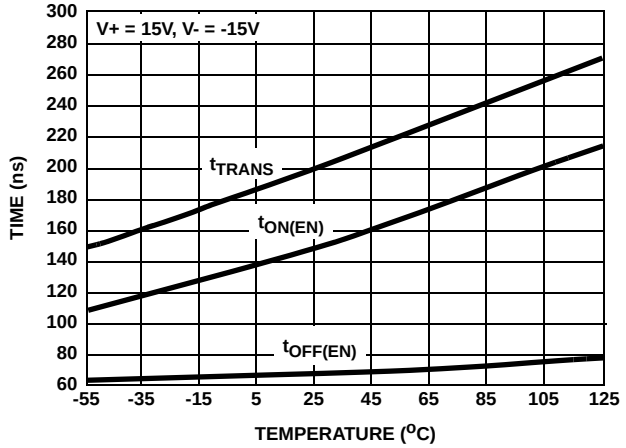


FIGURE 13. t_{ON}/t_{OFF} vs TEMPERATURE

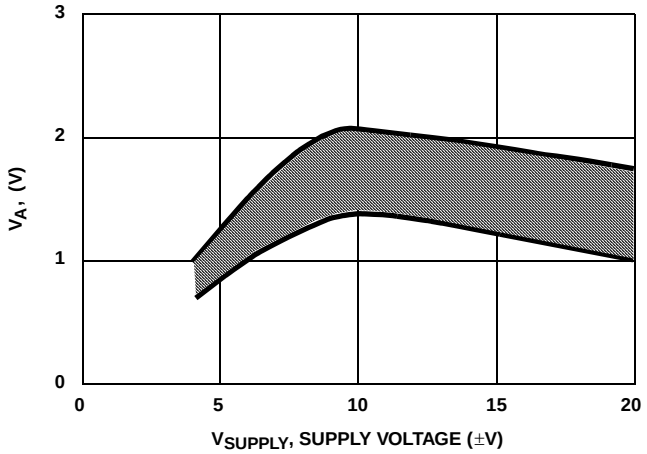


FIGURE 14. SWITCHING THRESHOLD vs SUPPLY VOLTAGE

Die Characteristics

DIE DIMENSIONS:

2490µm x 4560µm x 485µm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

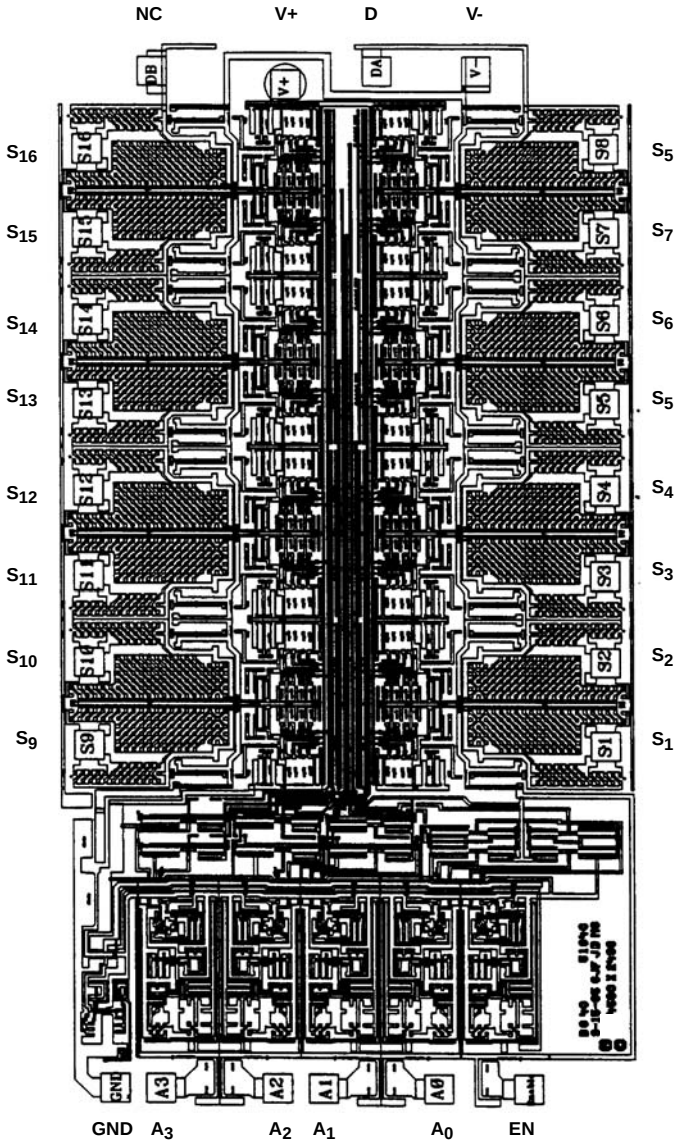
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG406



Die Characteristics

DIE DIMENSIONS:

2490µm x 4560µm x 485µm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

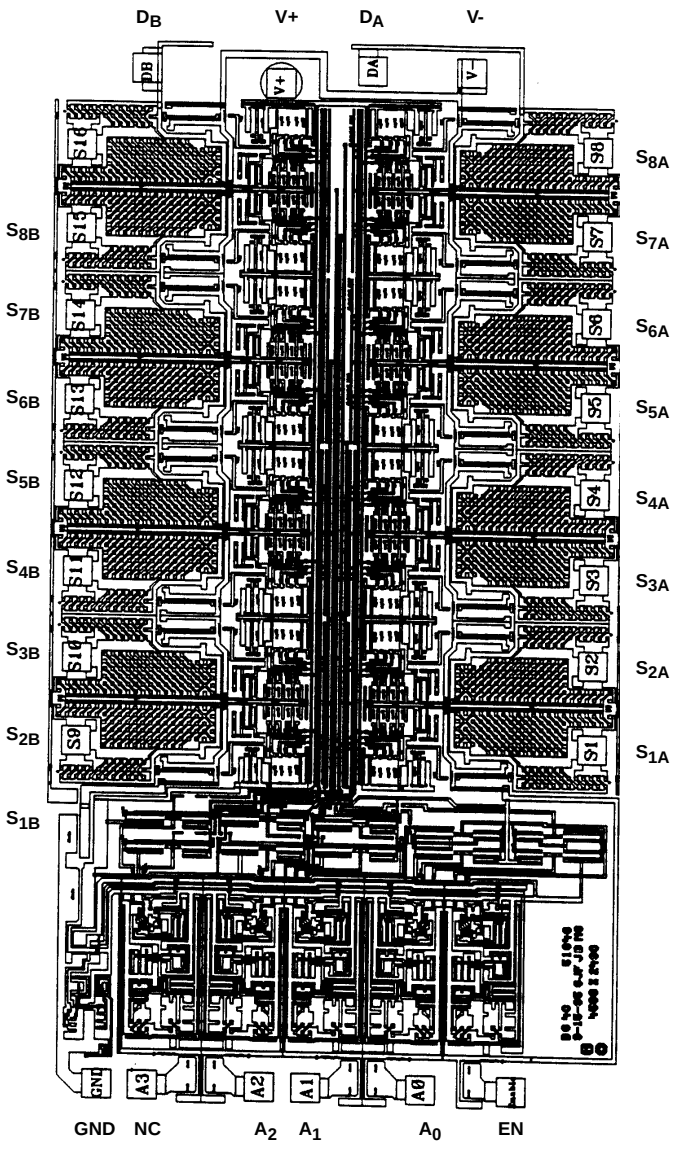
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

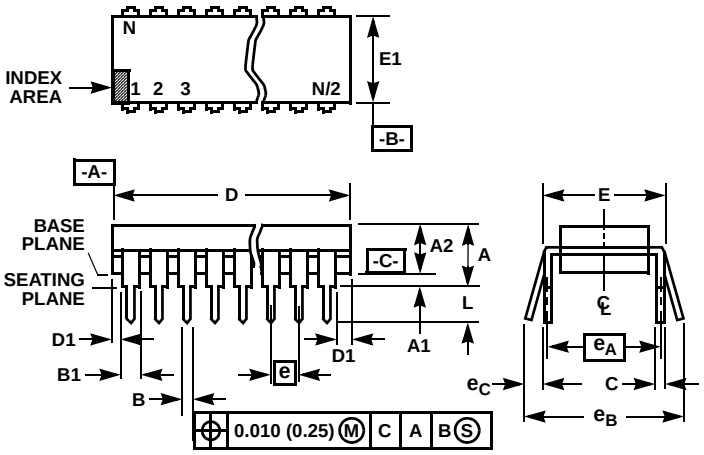
9.1×10^4 A/cm^2

Metallization Mask Layout

DG407



Dual-In-Line Plastic Packages (PDIP)



NOTES:

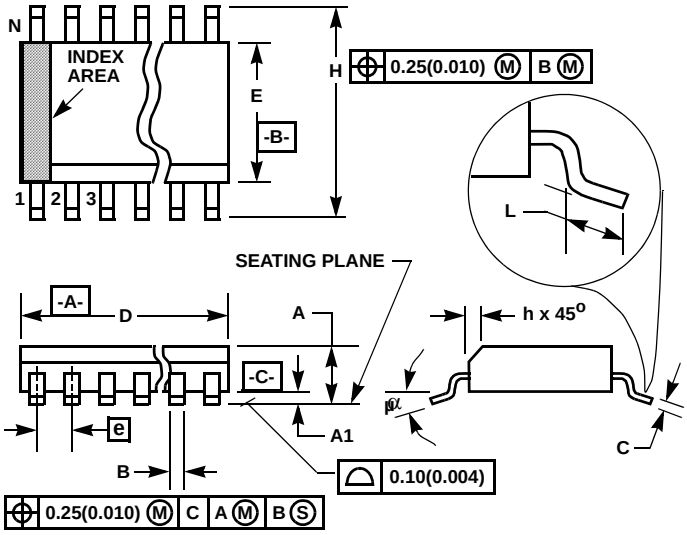
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E28.6 (JEDEC MS-011-AB ISSUE B)
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

Rev. 1 12/00

Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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19-4729; Rev 6; 3/10

Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

General Description

Maxim's redesigned DG406 and DG407 CMOS analog multiplexers now feature guaranteed matching between channels (8Ω, max) and flatness over the specified signal range (9Ω, max). These low on-resistance muxes (100Ω, max) conduct equally well in either direction and feature guaranteed low charge injection (15pC, max). In addition, these new muxes offer low input off-leakage current over temperature—less than 5nA at +85°C.

The DG406 is a 1 of 16 multiplexer/demultiplexer and the DG407 is a dual 8-channel multiplexer/demultiplexer. Both muxes operate with a +5V to +30V single supply and with ±4.5V to ±20V dual supplies. ESD protection is guaranteed to be greater than 2000V per Method 3015.7 of MIL-STD 883. These improved muxes are pin-compatible plug-in upgrades for the industry standard DG406 and DG407.

Applications

Sample-and-Hold Circuits

Test Equipment

Guidance and Control Systems

Communications Systems

Data-Acquisition Systems

Audio Signal Routing

Features

- **Pin-Compatible Plug-In Upgrade for Industry Standard DG406/DG407**
- **Guaranteed Matching Between Channels, 8Ω (max)**
- **Guaranteed On-Resistance Flatness, 9Ω (max)**
- **Guaranteed Low Charge Injection, 15pC (max)**
- **Low On-Resistance 100Ω (max)**
- **Input Leakage, 5nA (max) at +85°C**
- **Low Power Consumption, 1.25mW (max)**
- **Rail-to-Rail Signal Handling**
- **Digital Input Controls TTL/CMOS Compatible**
- **ESD Protection >2000V per Method 3015.7**

Ordering Information

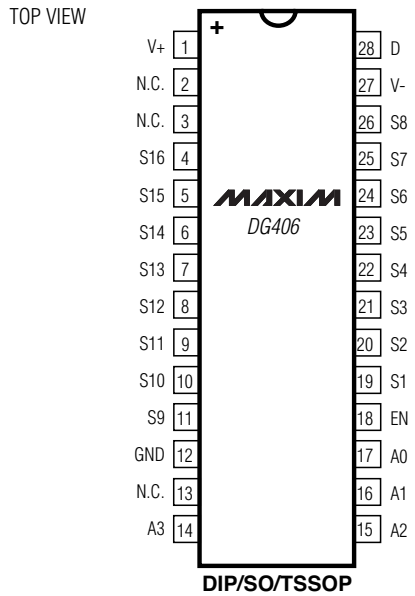
PART	TEMP RANGE	PIN-PACKAGE
DG406CJ+	0°C to +70°C	28 Plastic DIP
DG406CWI+	0°C to +70°C	28 Wide SO
DG406C/D	0°C to +70°C	Dice*
DG406DJ+	-40°C to +85°C	28 Plastic DIP
DG406EWI+	-40°C to +85°C	28 Wide SO
DG406DN+	-40°C to +85°C	28 PLCC
DG406AK+	-55°C to +125°C	28 CERDIP
DG406EUI+	-40°C to +85°C	28 TSSOP

Ordering Information continued at end of data sheet.

**Contact factory for dice specifications.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

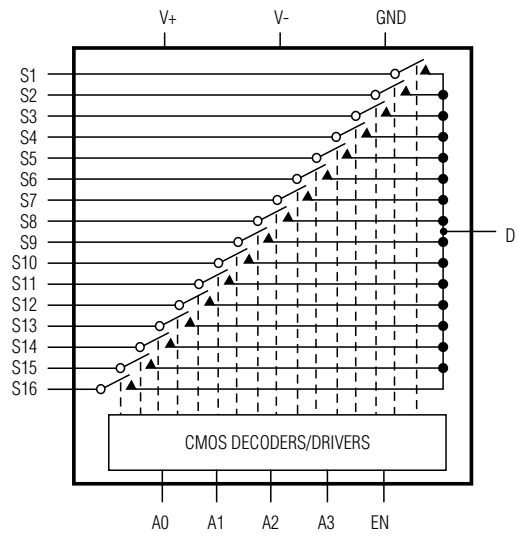
Pin Configurations



DIP/SO/TSSOP

Pin Configurations continued at end of data sheet.

Functional Diagrams



DG406 16-CHANNEL SINGLE-ENDED MULTIPLEXER

Functional Diagrams continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

(Voltage Referenced to V-)
V+ .....-0.3V, 44V
GND .....-0.3V, 25V
Digital Inputs, S, D (Note 1).....(V- - 2V) to (V+ + 2V) or 30mA (whichever occurs first)
Continuous Current (any terminal) 30mA
Peak Current, S or D
(pulsed at 1ms, 10% duty cycle max) 100mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ..727mW
28-Pin Wide SO (derate 12.50mW/°C above +70°C) ...1000mW
28-Pin PLCC (derate 10.53mW/°C above +70°C) 842mW
28-Pin CERDIP (derate 16.67mW/°C above +70°C)...1333mW
28-Pin TSSOP (derate 12.8mW/°C above +70°C) 1025mW
Operating Temperature Ranges
DG406/DG407C_ .....0°C to +70°C
DG406/DG407D_ .....-40°C to +85°C
DG406/DG407AK .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (excluding dice; soldering, 10s) .....+300°C
Soldering Temperature (reflow)
Plastic DIP, Wide SO, TSSOP .....+260°C
PLCC.....+245°C
CERDIP, Dice.....+240°C

Note 1: Signals on S_, D_, A0, A1, A2, A3, or EN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 15V, V- = -15V, V_{GND} = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP (Note 2)	MAX	UNITS
SWITCH									
Analog Signal Range	V_{ANALOG}	(Note 3)				-15		+15	V
Drain-Source On-Resistance	$R_{DS(ON)}$	I_S = -1.0mA, V_D = ±10V		T_A = +25°C			60	100	Ω
				T_A = T_{MIN} to T_{MAX}				125	
On-Resistance Matching Between Channels	$\Delta R_{DS(ON)}$	I_S = -1.0mA, V_D = ±10V (Note 4)		T_A = +25°C			1.5	8	Ω
				T_A = T_{MIN} to T_{MAX}				10	
On-Resistance Flatness	R_{FLAT}	I_S = -1.0mA, V_D = ±5V or 0V		T_A = +25°C			1.8	9	Ω
				T_A = T_{MIN} to T_{MAX}				12	
Source-Off Leakage Current (Note 5)	$I_{S(OFF)}$	V_D = +10V, V_S = ±10V, V_{EN} = 0V		T_A = +25°C		-0.5	+0.01	+0.5	nA
				T_A = T_{MIN} to T_{MAX}	C, D	-5		+5	
					A	-50		+50	
Drain-Off Leakage Current (Note 5)	$I_{D(OFF)}$	V_D = ±10V, V_S = +10V, V_{EN} = 0V	DG406	T_A = +25°C		-1	+0.02	+1	nA
				T_A = T_{MIN} to T_{MAX}	C, D	-40		+40	
					A	-200		+200	
		V_D = +10V, V_S = ±10V, V_{EN} = 0V	DG407	T_A = +25°C		-1	+0.02	+1	
				T_A = T_{MIN} to T_{MAX}	C, D	-20		+20	
					A	-100		+100	
Drain-On Leakage Current (Note 5)	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = ±10V, V_S = ±10V, sequence each switch on	DG406	T_A = +25°C		-1	+0.02	+1	nA
				T_A = T_{MIN} to T_{MAX}	C, D	-40		+40	
					A	-200		+200	
			DG407	T_A = +25°C		-1	+0.02	+1	
				T_A = T_{MIN} to T_{MAX}	C, D	-20		+20	
					A	-100		+100	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = 15V, V- = -15V, V_{GND} = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
INPUT								
Input Current with Input Voltage High	I_{AH}	V_A = 2.4V or 15V			-1.0		+1.0	µA
Input Current with Input Voltage Low	I_{AL}	V_{EN} = 0V or 2.4V, V_A = 0V			-1.0		+1.0	µA
SUPPLY								
Power-Supply Range					±4.5		±20	V
Positive Supply Current	I+	V_{EN} = V_A = 0V or 5.0V		T_A = +25°C		16	30	µA
				T_A = T_{MIN} to T_{MAX}			75	
		V_{EN} = 2.4V, $V_{A(ALL)}$ = 0V		T_A = +25°C		0.075	0.5	mA
				T_A = T_{MIN} to T_{MAX}			1	
Negative Supply Current	I-	V_{EN} = 2.4V, $V_{A(ALL)}$ = 0V		T_A = +25°C	-1		+1	µA
				T_A = T_{MIN} to T_{MAX}	-10		+10	
DYNAMIC								
Transition Time	t_{TRANS}	Figure 2		T_A = +25°C		110	300	ns
				T_A = T_{MIN} to T_{MAX}			400	
Break-Before-Make Interval	t_{OPEN}	Figure 4		T_A = +25°C	10	40		ns
Enable Turn-On Time	$t_{ON(EN)}$	Figure 3		T_A = +25°C		130	200	ns
				T_A = T_{MIN} to T_{MAX}			400	
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 3		T_A = +25°C		55	150	ns
				T_A = T_{MIN} to T_{MAX}			300	
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_S = 0V, R_S = 0Ω, Figure 5		T_A = +25°C		2	15	pC
Off-Isolation (Note 6)	V_{ISO}	V_{EN} = 0V, R_L = 1kΩ, f = 100kHz, Figure 6		T_A = +25°C		-69		dB
Crosstalk Between Channels	V_{CT}	V_{EN} = 2.4V, f = 100kHz, V_{GEN} = $1V_{P-P}$, R_L = 1kΩ, Figure 7		T_A = +25°C		-92		dB
Logic Input Capacitance	C_{IN}	f = 1MHz		T_A = +25°C		8		pF
Source-Off Capacitance	$C_{S(OFF)}$	f = 1MHz, V_{EN} = V_S = 0V, Figure 8		T_A = +25°C		8		pF
Drain-Off Capacitance	$C_{D(OFF)}$	f = 1MHz, V_{EN} = 0.8V, V_D = 0V, Figure 8	DG406	T_A = +25°C		130		pF
			DG407			65		
Drain-Source On Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$	f = 1MHz, V_{EN} = 2.4V, V_D = 0V, Figure 8	DG406	T_A = +25°C		140		pF
			DG407			70		

Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = 12V, V- = 0V, V_{GND} = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V_{ANALOG}	(Note 3)		0		12	V
Drain-Source On-Resistance	$R_{DS(ON)}$	I_S = -1.0mA V_D = 3V or 10V	T_A = +25°C		120	175	Ω
DYNAMIC							
Transition Time (Note 3)	t_{TRANS}	V_{S1} = 8V, V_{S16} = 0V, V_A = 0V, Figure 2	T_A = +25°C		130	450	ns
Enable Turn-On Time (Note 3)	$t_{ON(EN)}$	V_{AL} = 0V, V_{S1} = 5V, Figure 3	T_A = +25°C		105	600	ns
Enable Turn-Off Time (Note 3)	$t_{OFF(EN)}$	V_{AL} = 0V, V_{S1} = 5V, Figure 3	T_A = +25°C		80	300	ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_{S1} = 0V, R_S = 0Ω	T_A = +25°C		2	10	pC

Note 2: The algebraic convention where the most negative value is a minimum and the most positive value a maximum is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$. On-resistance match between channels and flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured at the extremes of the specified analog signal range.

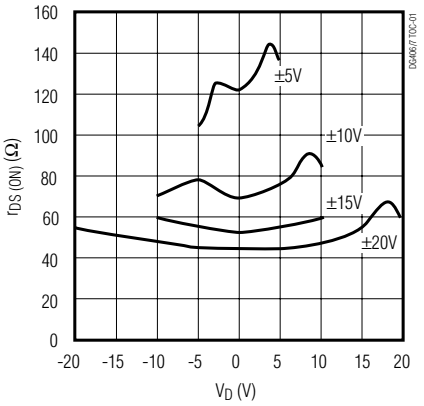
Note 5: Leakage parameters are 100% tested at the maximum-rated hot temperature and guaranteed by correlation at +25°C.

Note 6: Off-isolation = 20log V_D/V_S, where V_D = output and V_S = input to off switch.

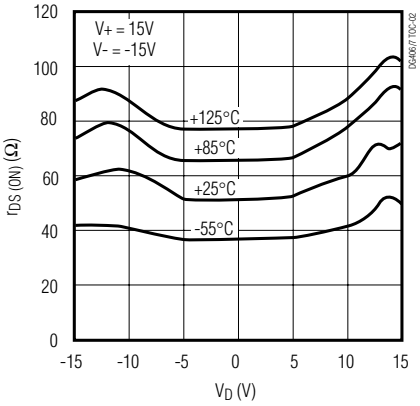
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

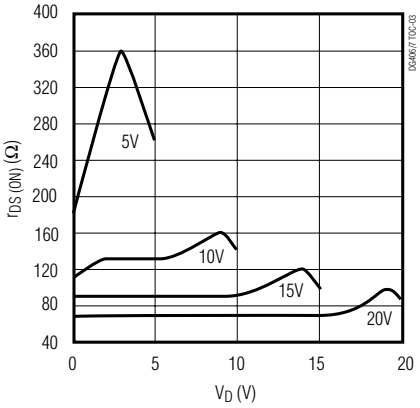
ON-RESISTANCE vs. V_D (DUAL SUPPLIES)



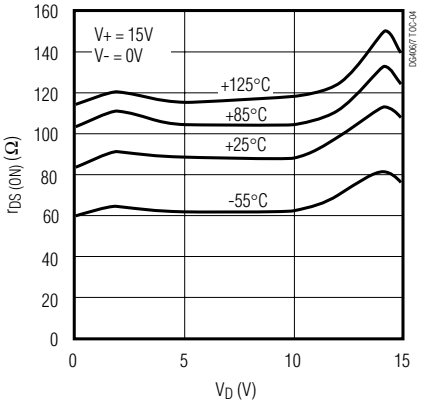
ON-RESISTANCE vs. V_D AND TEMPERATURE (DUAL SUPPLIES)



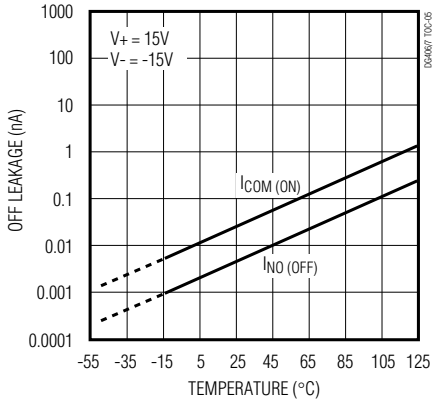
ON-RESISTANCE vs. V_D (SINGLE SUPPLY)



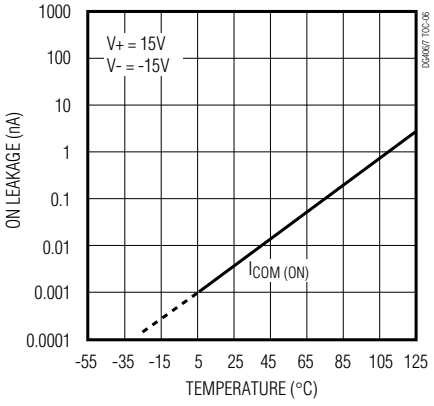
ON-RESISTANCE vs. V_D AND TEMPERATURE (SINGLE SUPPLY)



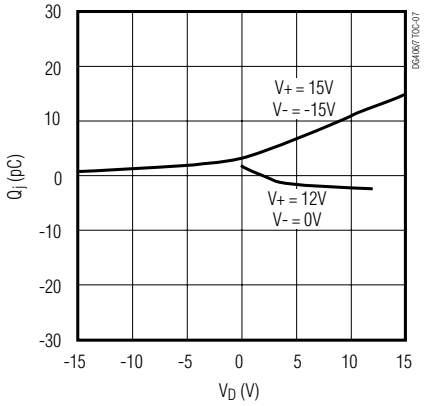
OFF LEAKAGE vs. TEMPERATURE



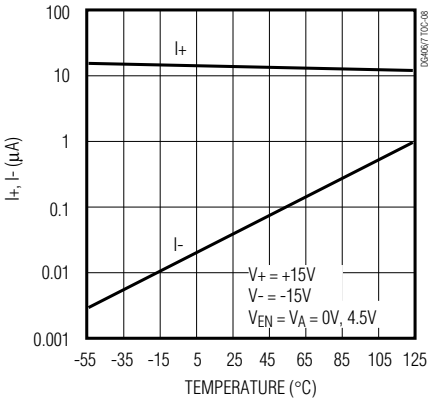
ON LEAKAGE vs. TEMPERATURE



CHARGE INJECTION vs. V_D



SUPPLY CURRENT vs. TEMPERATURE



Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

Pin Descriptions

DG406 PIN	NAME	FUNCTION
1	V+	Positive Supply Voltage Input
2, 3, 13	N.C.	No Connection. Not internally connected.
4–11	S16–S9	Bidirectional Analog Inputs
12	GND	Ground
14–17	A3–A0	Address Inputs
18	EN	Enable Inputs
19–26	S1–S8	Bidirectional Analog Inputs
27	V-	Negative Supply Voltage Input
28	D	Bidirectional Output

DG407 PIN	NAME	FUNCTION
1	V+	Positive Supply Voltage Input
2	DB	Bidirectional Output B
3, 13, 14	N.C.	No Connection. Not internally connected.
4–11	S8B–S1B	Bidirectional Analog Inputs
12	GND	Ground
15, 16, 17	A2, A1, A0	Address Inputs
18	EN	Enable Input
19–26	S1A–S8A	Bidirectional Analog Inputs
27	V-	Negative Supply Voltage Input
28	DA	Bidirectional Output A

Applications Information

Operation with Supply Voltages Other than ±15V

Using supply voltages other than ±15V reduces the analog signal range. The DG406/DG407 switches operate with ±4.5V to ±20V bipolar supplies or with a +5V to +30V single supply; connect V- to GND when operating with a single supply. Also, both device types can operate with unbalanced supplies such as +24V and -5V. The *Typical Operating Characteristics* graphs show typical on-resistance with 20V, 15V, 10V, and 5V supplies. (Switching times increase by a factor of two or more for operation at 5V.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, then V-, followed by the logic inputs and analog signals. If power-supply sequencing is not possible, add two small signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to 1V above V+ and 1V below V-, but low switch resistance and low leakage characteristics are unaffected. Device operation is unchanged, and the difference between V+ and V- should not exceed +44V.

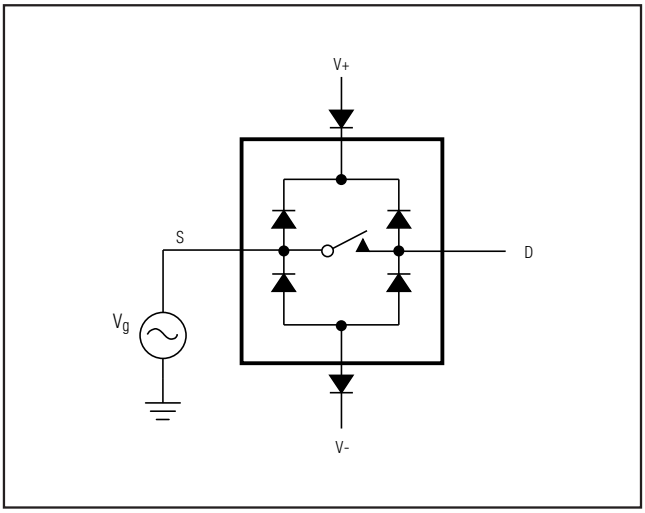


Figure 1. Overvoltage Protection Using External Blocking Diodes

Test Circuits/Timing Diagrams

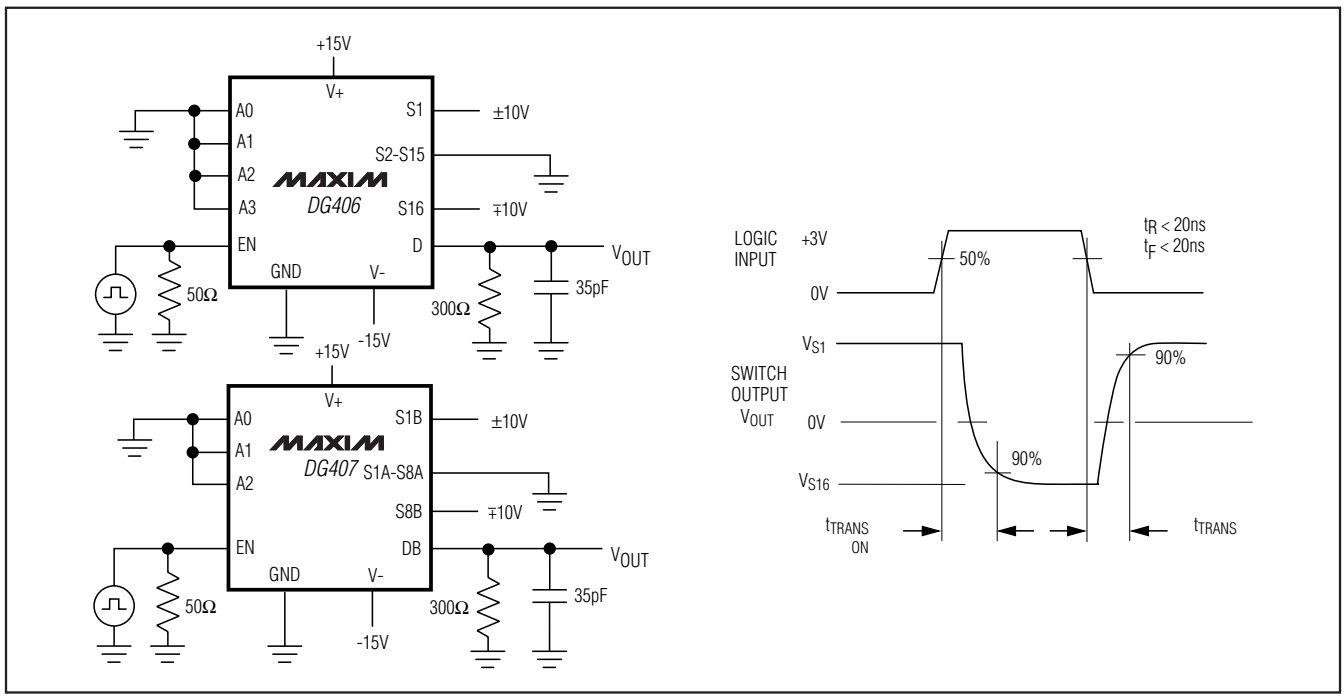


Figure 2. Transition Time

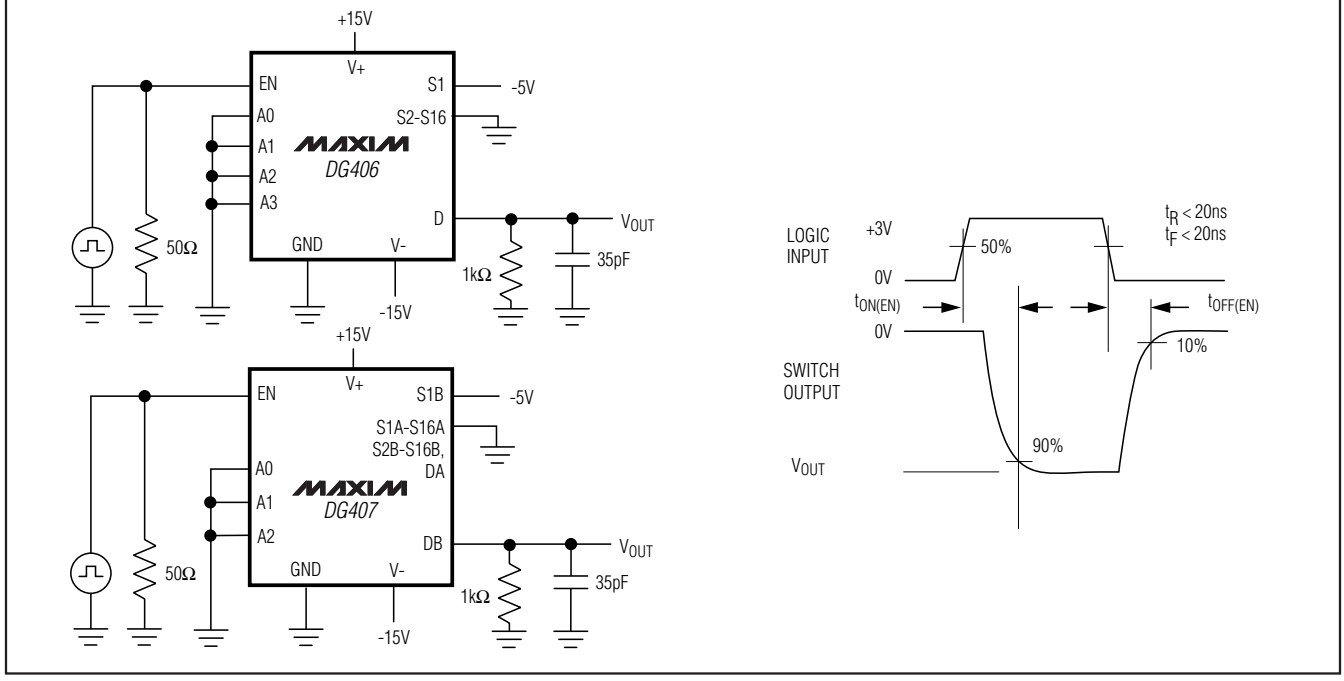


Figure 3. Enable Switching Time

Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

Test Circuits/Timing Diagrams (continued)

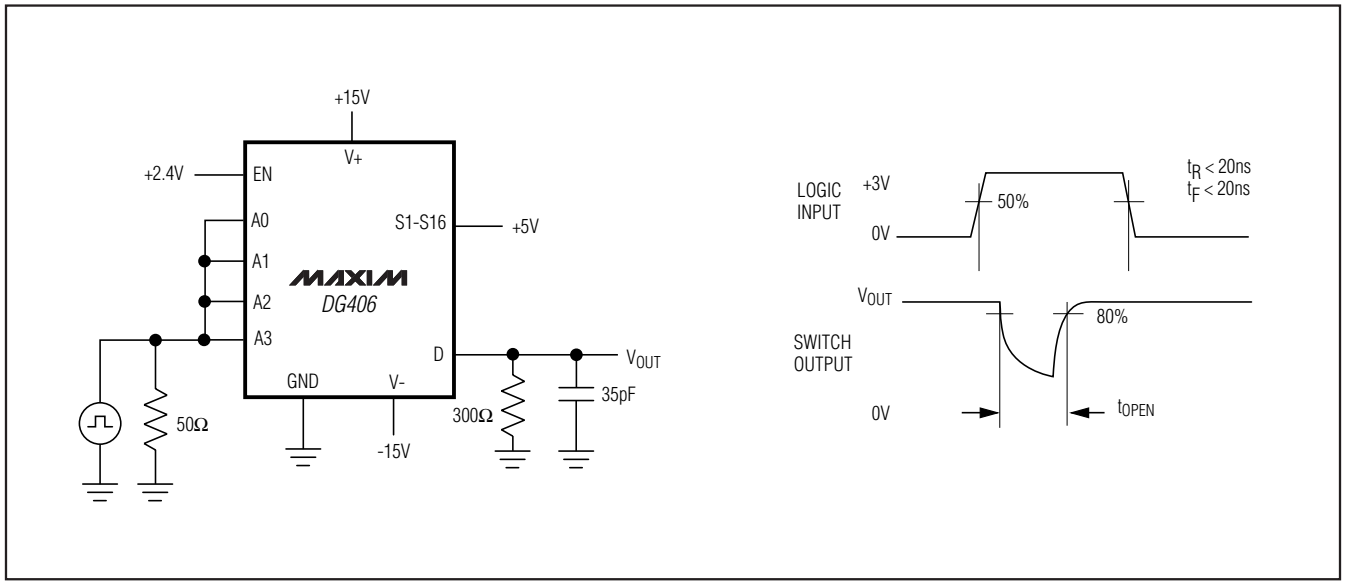


Figure 4. Break-Before-Make Interval

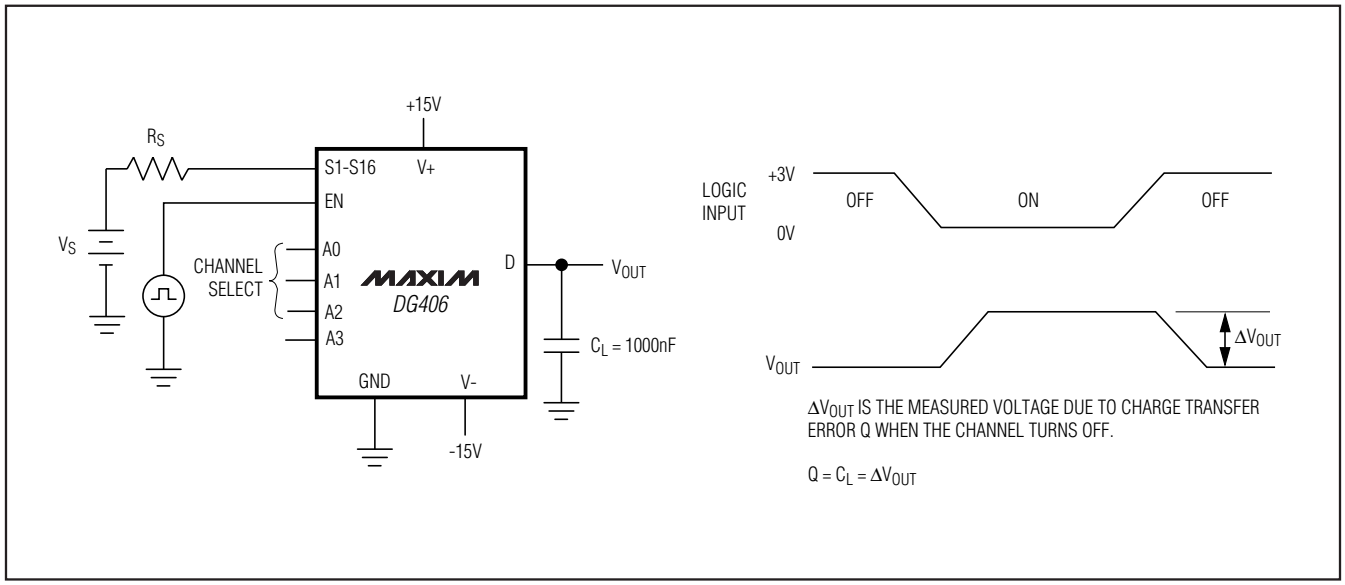


Figure 5. Charge Injection

Test Circuits/Timing Diagrams (continued)

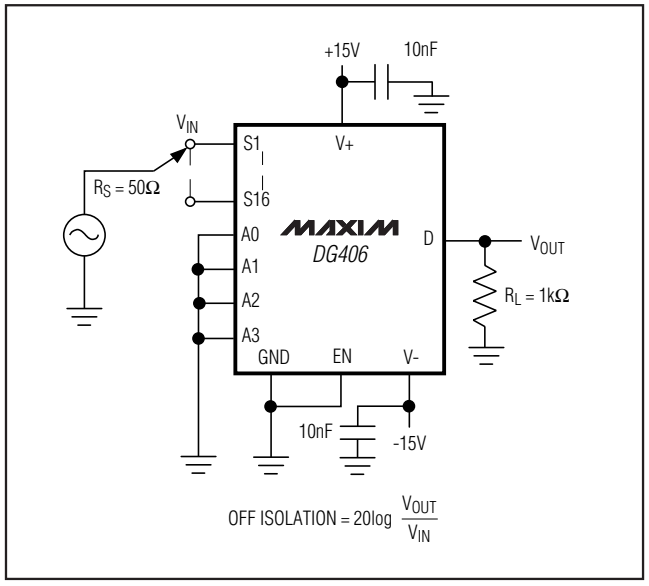


Figure 6. Off-Isolation

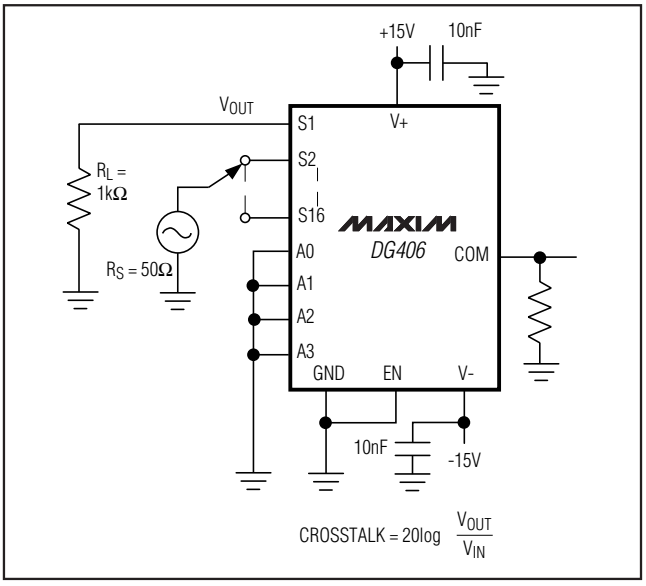


Figure 7. Crosstalk

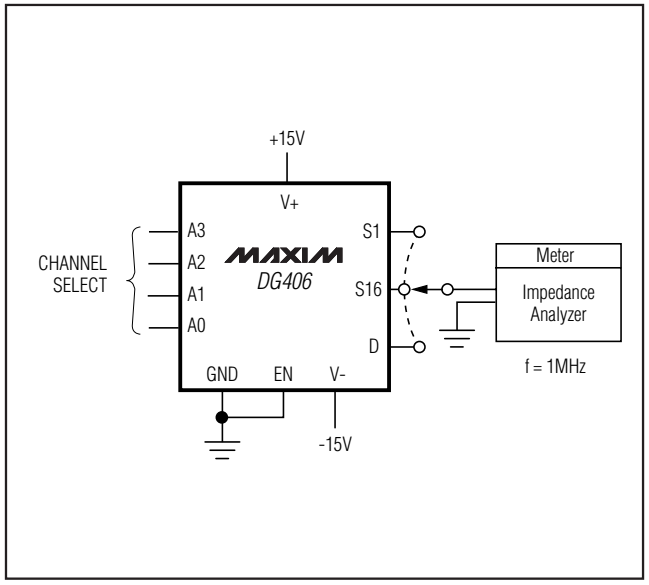
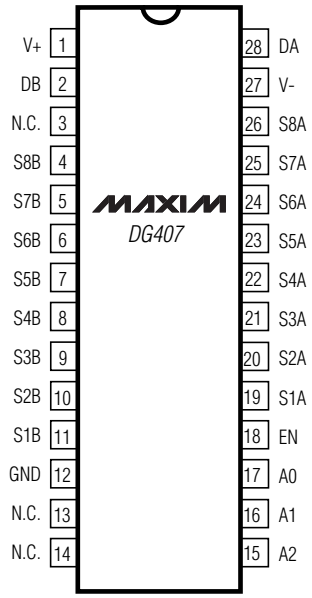


Figure 8. Source/Drain Capacitance

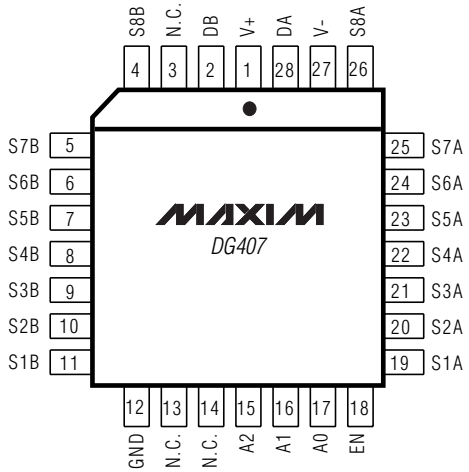
Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

_____Pin Configurations/Functional Diagrams/Truth Tables (continued)

TOP VIEW



DIP/SO



PLCC

N.C. = NO INTERNAL CONNECTION

A3	A2	A1	A0	EN	ON Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

DG406

LOGIC "0" $V_{AL} \leq 0.8V$, LOGIC "1" = $V_{AH} \geq 2.4V$

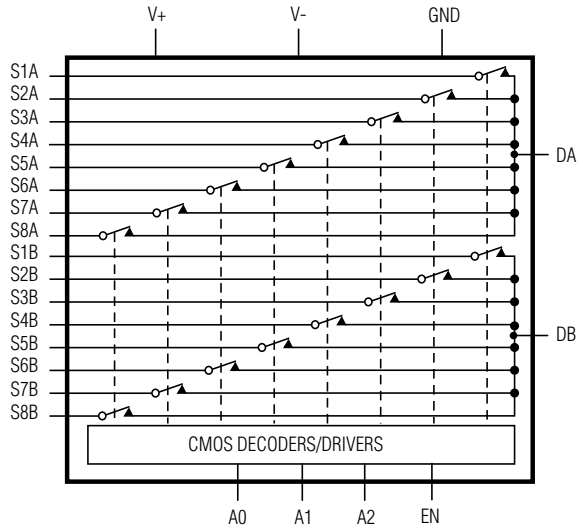
A2	A1	A0	EN	ON Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG407

LOGIC "0" $V_{AL} \leq 0.8V$, LOGIC "1" = $V_{AH} \geq 2.4V$

Improved, 16-Channel/Dual 8-Channel, High-Performance, CMOS Analog Multiplexers

__Functional Diagrams (continued)



DG407 8-CHANNEL DIFFERENTIAL MULTIPLEXER

_Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
DG407CJ+	0°C to +70°C	28 Plastic DIP
DG407CWI+	0°C to +70°C	28 Wide SO
DG407C/D+	0°C to +70°C	Dice*
DG407DJ+	-40°C to +85°C	28 Plastic DIP
DG407EWI+	-40°C to +85°C	28 Wide SO
DG407DN+	-40°C to +85°C	28 PLCC
DG407AK	-55°C to +125°C	28 CERDIP
DG407EUI+	-40°C to +85°C	28 TSSOP

**Contact factory for dice specifications.*
+Denotes a lead(Pb)-free/RoHS-compliant package.

Package Information

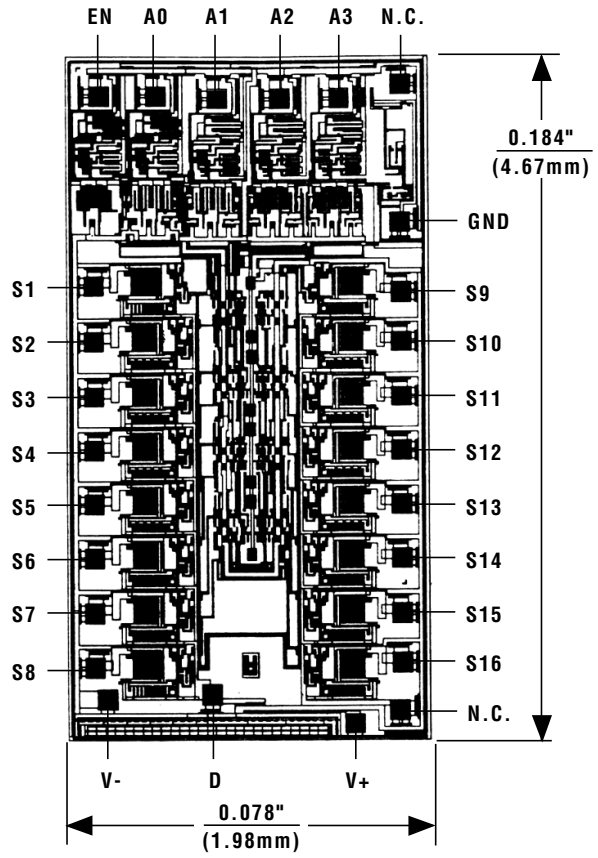
For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 PDIP	P28+3	**21-0044**
28 Wide SO	W28+6	**21-0042**
28 PLCC	Q28+4	**21-0049**
28 TSSOP	U28+2	**21-0066**
28 CERDIP	J28+2	**21-0046**

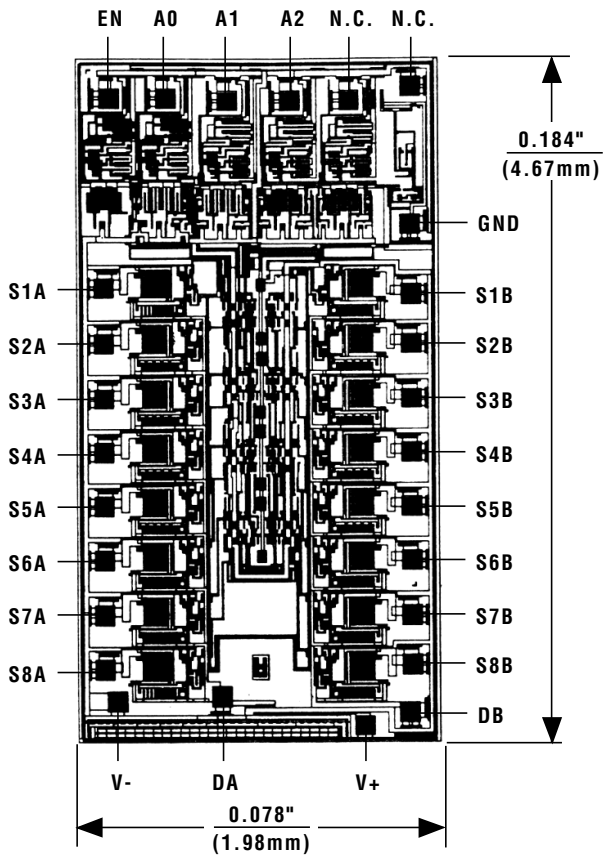
Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

Chip Topographies

DG406



DG407



N.C. = NO INTERNAL CONNECTION

SUBSTRATE IS INTERNALLY CONNECTED TO V+

SUBSTRATE IS INTERNALLY CONNECTED TO V+

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
6	3/10	Updated the minimum limit of the single supply range.	1, 6
		Added the soldering temperature of all packages to the *Absolute Maximum Ratings*.	2

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