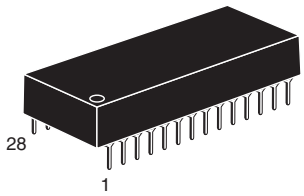
M48T35
M48T35Y

5 V, 256 Kbit (32 Kb x 8) TIMEKEEPER® SRAM

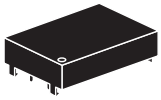
Features

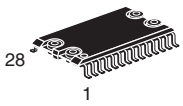
- Integrated, ultra low power SRAM, real-time clock, power-fail control circuit and battery
- BYTEWIDE™ RAM-like clock access
- BCD coded year, month, day, date, hours, minutes, and seconds
- Frequency test output for real-time clock
- Automatic power-fail chip deselect and WRITE protection
- WRITE protect voltages (V_{PFD} = power-fail deselect voltage):
  - M48T35: V_{CC} = 4.75 to 5.5 V; 4.5 V ≤ V_{PFD} ≤ 4.75 V
  - M48T35Y: V_{CC} = 4.5 to 5.5 V; 4.2 V ≤ V_{PFD} ≤ 4.5 V
- Self-contained battery and crystal in the CAPHAT™ DIP package
- SOIC package provides direct connection for a SNAPHAT® housing containing the battery and crystal
- SNAPHAT® housing (battery and crystal) is replaceable
- Pin and function compatible with JEDEC standard 32 Kb x 8 SRAMs
- RoHS compliant
  - Lead-free second level interconnect



PCDIP28
Battery/crystal
CAPHAT™

SNAPHAT®
Battery/crystal





SOH28

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1 Description

The M48T35/Y TIMEKEEPER® RAM is a 32 Kb x 8 non-volatile static RAM and real-time clock. The monolithic chip is available in two special packages to provide a highly integrated battery-backed memory and real-time clock solution.

The M48T35/Y is a non-volatile pin and function equivalent to any JEDEC standard 32 Kb x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special WRITE timing or limitations on the number of WRITEs that can be performed.

The 28-pin, 600 mil DIP CAPHAT™ houses the M48T35/Y silicon with a quartz crystal and a long life lithium button cell in a single package.

The 28-pin, 330 mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT® housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion. The SOIC and battery/crystal packages are shipped separately in plastic anti-static tubes or in tape & reel form.

For the 28-lead SOIC, the battery/crystal package (e.g., SNAPHAT) part number is “M4T28-BR12SH”.

Figure 1. Logic diagram

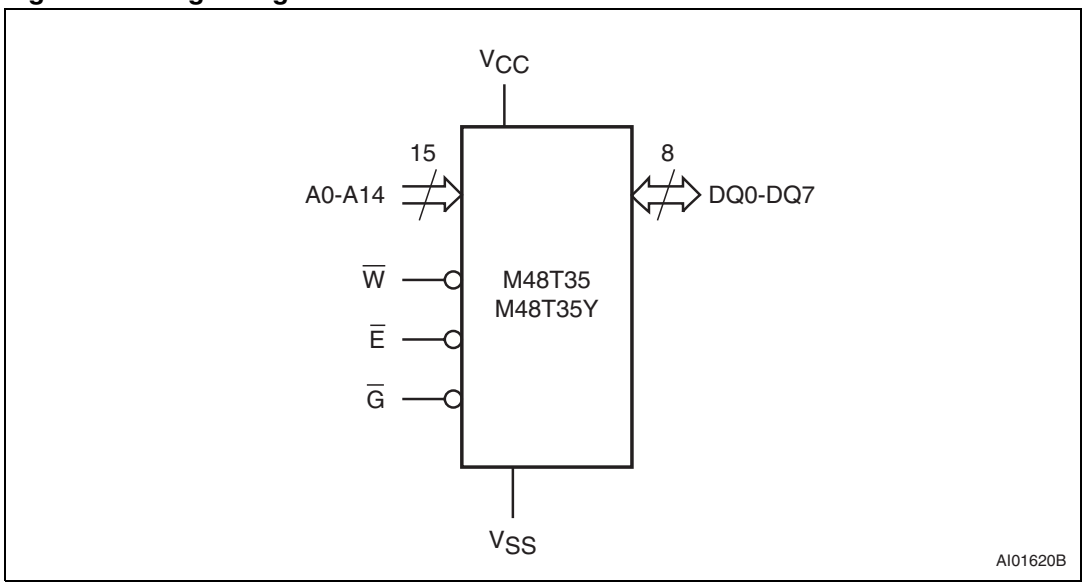


Table 1. Signal names

A0-A14	Address inputs
DQ0-DQ7	Data inputs / outputs
$\overline{E}$	Chip enable
$\overline{G}$	Output enable
$\overline{W}$	WRITE enable
V_{CC}	Supply voltage
V_{SS}	Ground

Figure 2. DIP connections

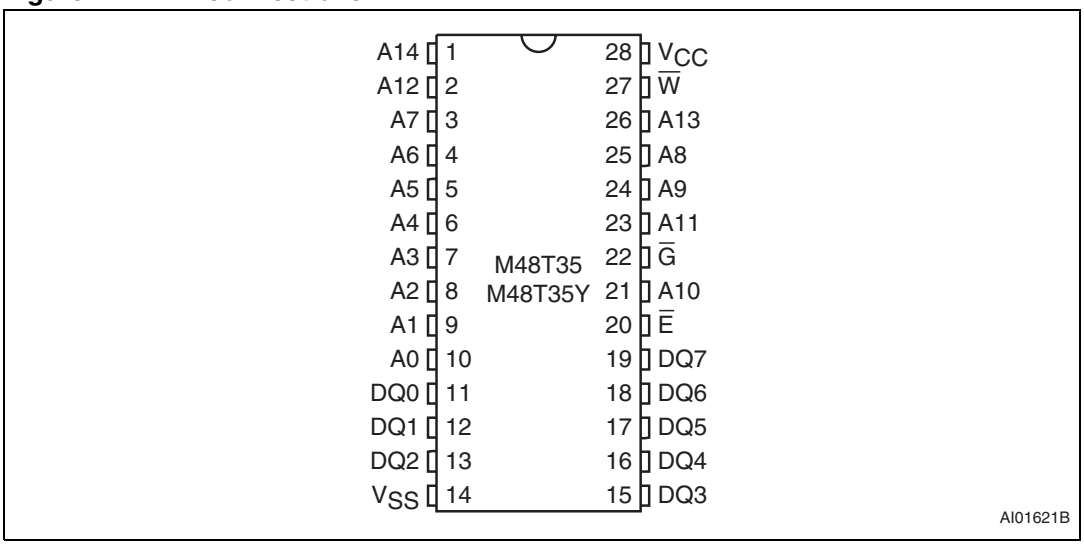


Figure 3. SOIC connections

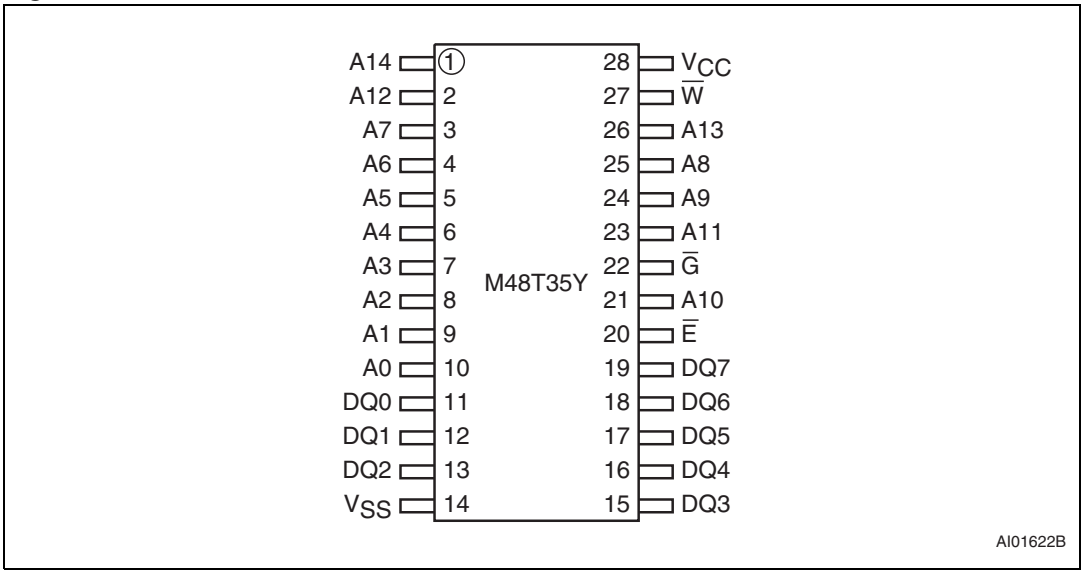
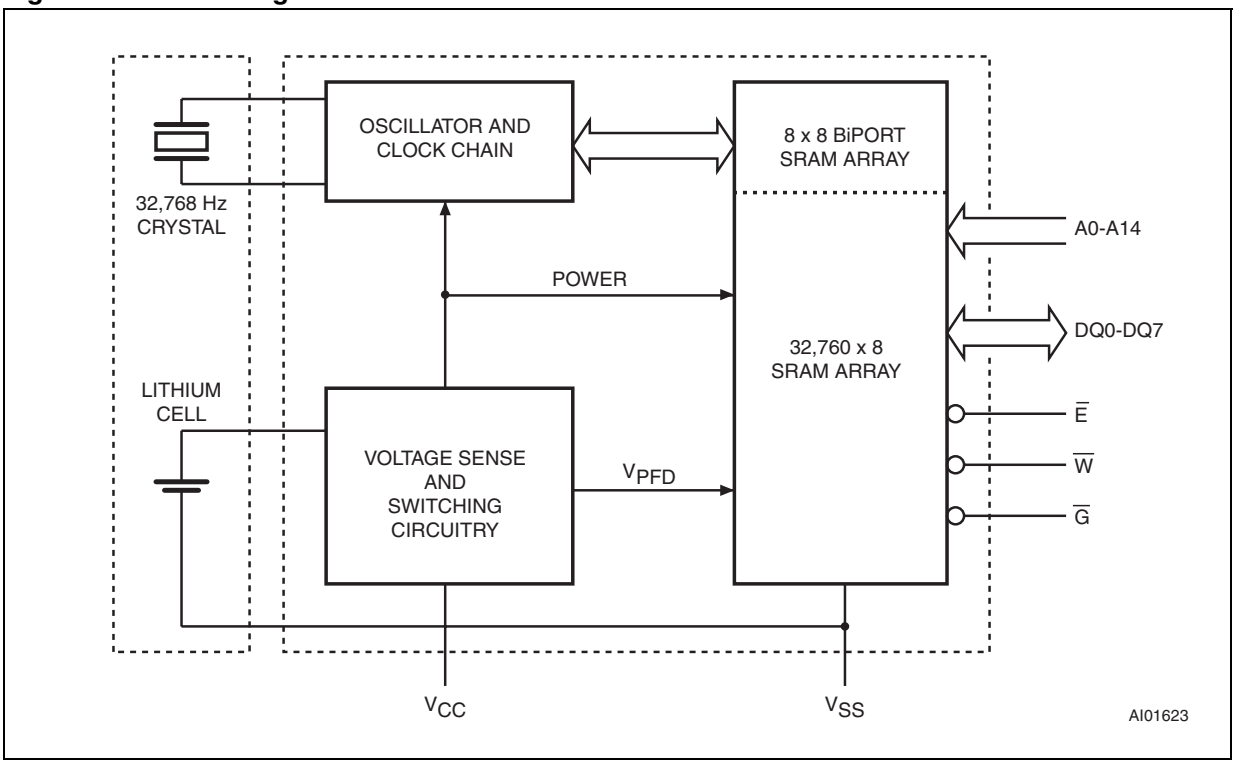


Figure 4. Block diagram



2 Operation modes

As *Figure 4 on page 7* shows, the static memory array and the quartz controlled clock oscillator of the M48T35/Y are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations to provide user accessible BYTEWIDE clock information in the bytes with addresses 7FF8h-7FFFh.

The clock locations contain the year, month, date, day, hour, minute, and second in 24-hour BCD format. Corrections for 28, 29 (leap year - valid until 2100), 30, and 31 day months are made automatically. Byte 7FF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ READ/WRITE memory cells. The M48T35/Y includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48T35/Y also has its own power-fail detect circuit. The control circuitry constantly monitors the single 5 V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below the battery backup switchover voltage (V_{SO}), the control circuitry connects the battery which maintains data and clock operation until valid power returns.

Table 2. Operating modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75 to 5.5 V or 4.5 to 5.5 V	V_{IH}	X	X	High Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)(1)	X	X	X	High Z	CMOS standby
Deselect	$\leq V_{SO}$(1)	X	X	X	High Z	Battery backup mode

1. See *Table 11 on page 20* for details.

X = V_{IH} or V_{IL}; V_{SO} = battery backup switchover voltage.

2.1 READ mode

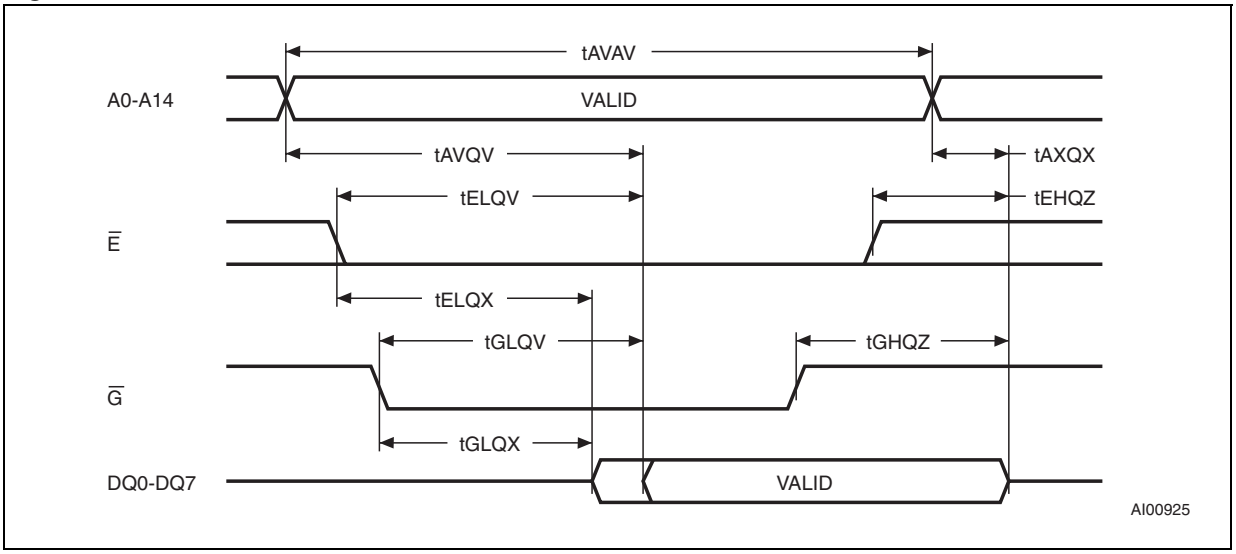
The M48T35/Y is in the READ mode whenever $\overline{W}$ (WRITE enable) is high and $\overline{E}$ (chip enable) is low. The unique address specified by the 15 address inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the data I/O pins within address access time (t_{AVQV}) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied.

If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the chip enable access time (t_{ELQV}) or output enable access time (t_{GLQV}).

The state of the eight three-state data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}.

If the address inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for output data hold time (t_{AXQX}) but will go indeterminate until the next address access.

Figure 5. READ mode AC waveforms



Note: WRITE enable ($\overline{W}$) = high.

Table 3. READ mode AC characteristics

Symbol	Parameter[1]	M48T35/Y		Unit
		Min	Max	
t_{AVAV}	READ cycle time	70		ns
t_{AVQV}	Address valid to output valid		70	ns
t_{ELQV}	Chip enable low to output valid		70	ns
t_{GLQV}	Output enable low to output valid		35	ns
t_{ELQX}[2]	Chip enable low to output transition	5		ns
t_{GLQX}[2]	Output enable low to output transition	5		ns
t_{EHQZ}[2]	Chip enable high to output Hi-Z		25	ns
t_{GHQZ}[2]	Output enable high to output Hi-Z		25	ns
t_{AXQX}	Address transition to output transition	10		ns

1. Valid for ambient operating temperature: T_A = 0 to 70 or –40 to 85 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
2. C_L = 5 pF.

2.2 WRITE mode

The M48T35/Y is in the WRITE mode whenever W and E are low. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from chip enable or t_{WHAX} from WRITE enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on W will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 6. WRITE enable controlled, WRITE AC waveform

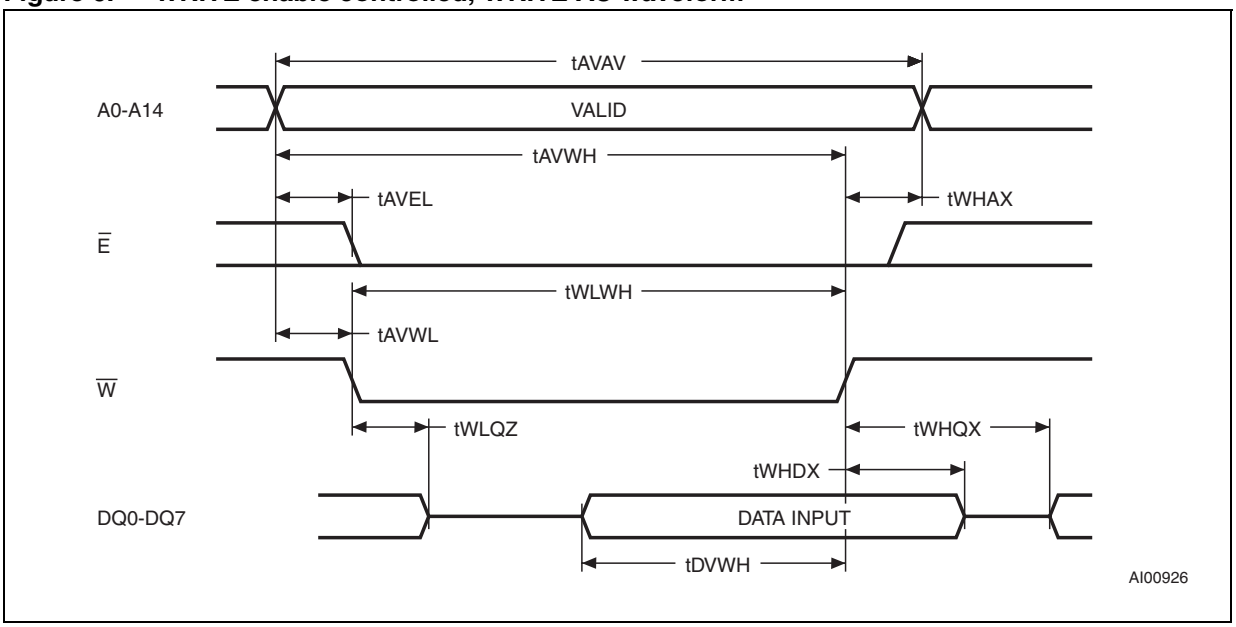


Figure 7. Chip enable controlled, WRITE AC waveforms

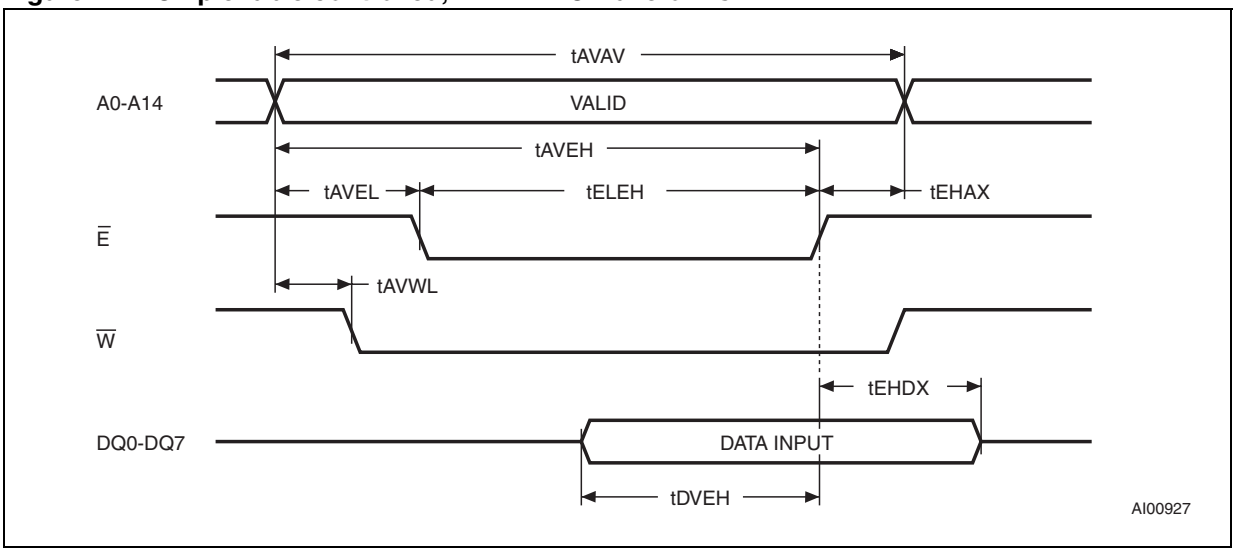


Table 4. WRITE mode AC characteristics

Symbol	Parameter[1]	M48T35/Y		Unit
		Min	Max	
t_{AVAV}	WRITE cycle time	70		ns
t_{AVWL}	Address valid to WRITE enable low	0		ns
t_{AVEL}	Address valid to chip enable low	0		ns
t_{WLWH}	WRITE enable pulse width	50		ns
t_{ELEH}	Chip enable low to chip enable high	55		ns
t_{WHAX}	WRITE enable high to address transition	0		ns
t_{EHAX}	Chip enable high to address transition	0		ns
t_{DVWH}	Input valid to WRITE enable high	30		ns
t_{DVEH}	Input valid to chip enable high	30		ns
t_{WHDX}	WRITE enable high to input transition	5		ns
t_{EHDX}	Chip enable high to input transition	5		ns
t_{WLQZ}[2][3]	WRITE enable low to output Hi-Z		25	ns
t_{AVWH}	Address valid to WRITE enable high	60		ns
t_{AVEH}	Address valid to chip enable high	60		ns
t_{WHQX}[2][3]	WRITE enable high to output transition	5		ns

1. Valid for ambient operating temperature: T_A = 0 to 70 or –40 to 85 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
2. C_L = 5 pF.
3. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

2.3 Data retention mode

With valid V_{CC} applied, the M48T35/Y operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. All outputs become high impedance, and all inputs are treated as “Don't care” (see *Figure 12 on page 19*, *Table 10*, and *Table 11 on page 20*).

Note: A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T35/Y may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48T35/Y for an accumulated period of at least 7 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues until V_{CC} reaches V_{PFD} (min) plus t_{rec} (min). $\overline{E}$ should be kept high as V_{CC} rises past V_{PFD} (min) to prevent inadvertent WRITE cycles prior to processor stabilization. Normal RAM operation can resume t_{rec} after V_{CC} exceeds V_{PFD} (max).

For more information on battery storage life refer to the application note AN1012.

3 Clock operations

3.1 Reading the clock

Updates to the TIMEKEEPER® registers (see *Table 5*) should be halted before clock data is read to prevent reading data in transition. The BiPORT™ TIMEKEEPER cells in the RAM array are only data registers and not the actual clock counters, so updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ bit, D6 in the control register 7FF8h. As long as a '1' remains in that position, updating is halted.

After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0.'

3.2 Setting the clock

Bit D7 of the control register 7FF8h is the WRITE bit. Setting the WRITE bit to a '1,' like the READ bit, halts updates to the TIMEKEEPER® registers. The user can then load them with the correct day, date, and time data in 24-hour BCD format (see *Table 5*). Resetting the WRITE bit to a '0' then transfers the values of all time registers 7FF9h-7FFFh to the actual TIMEKEEPER counters and allows normal operation to resume. The FT bit and the bits marked as '0' in *Table 5* must be written to '0' to allow for normal TIMEKEEPER and RAM operation. After the WRITE bit is reset, the next clock update will occur within one second.

See the application note AN923, “TIMEKEEPER® Rolling Into the 21st Century” for information on century rollover.

3.3 Stopping and starting the oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T35/Y is shipped from STMicroelectronics with the STOP bit set to a '1.' When reset to a '0,' the M48T35/Y oscillator starts within 1 second.

Table 5. Register map

Address	Data								Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
7FFFh	10 Years				Year				Year	00-99
7FFEh	0	0	0	10 M.	Month				Month	01-12
7FFDh	0	0	10 date		Date				Date	01-31
7FFCh	0	FT	CEB	CB	0	Day			Century/ day	00-01/01-07
7FFBh	0	0	10 hours		Hours				Hours	00-23
7FFAh	0	10 minutes			Minutes				Minutes	00-59
7FF9h	ST	10 seconds			Seconds				Seconds	00-59
7FF8h	W	R	S	Calibration					Control	

Keys:

S = SIGN bit

FT = FREQUENCY TEST bit (must be set to '0' upon power for normal operation)

R = READ bit

W = WRITE bit

ST = STOP bit

0 = Must be set to '0'

CEB = CENTURY ENABLE bit

CB = CENTURY bit

Note: When CEB is set to '1,' CB will toggle from '0' to '1' or from '1' to '0' at the turn of the century (dependent upon the initial value set).

When CEB is set to '0,' CB will not toggle. The WRITE bit does not need to be set to write to CEB.

3.4 Calibrating the clock

The M48T35/Y is driven by a quartz-controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed 35 ppm (parts per million) oscillator frequency error at 25 °C, which equates to about ±1.53 minutes per month. With the calibration bits properly set, the accuracy of each M48T35/Y improves to better than +1/–2 ppm at 25 °C.

The oscillation rate of any crystal changes with temperature (see *Figure 8 on page 15*). Most clock chips compensate for crystal frequency and temperature shift error with cumbersome “trim” capacitors. The M48T35/Y design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 9 on page 15*. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the control register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The calibration byte occupies the five lower order bits (D4-D0) in the control register 7FF8h. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is the

sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M48T35/Y may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the frequency test (FT) bit, the seventh-most significant bit in the day register is set to a '1,' and D7 of the seconds register is a '0' (oscillator running), DQ0 will toggle at 512 Hz during a READ of the seconds register. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (WR001010) to be loaded into the calibration byte for correction.

Note: Setting or changing the calibration byte does not affect the frequency test output frequency.

The FT bit MUST be reset to '0' for normal clock operations to resume. The FT bit is automatically reset on power-down.

For more information on calibration, see application note AN934, “TIMEKEEPER® Calibration.”

3.5 Century bit

Bit D5 and D4 of clock register 1FFCh contain the CENTURY ENABLE bit (CEB) and the CENTURY bit (CB). Setting CEB to a '1' will cause CB to toggle, either from a '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle.

Note: The WRITE bit must be set in order to write to the CENTURY bit.

Figure 8. Crystal accuracy across temperature

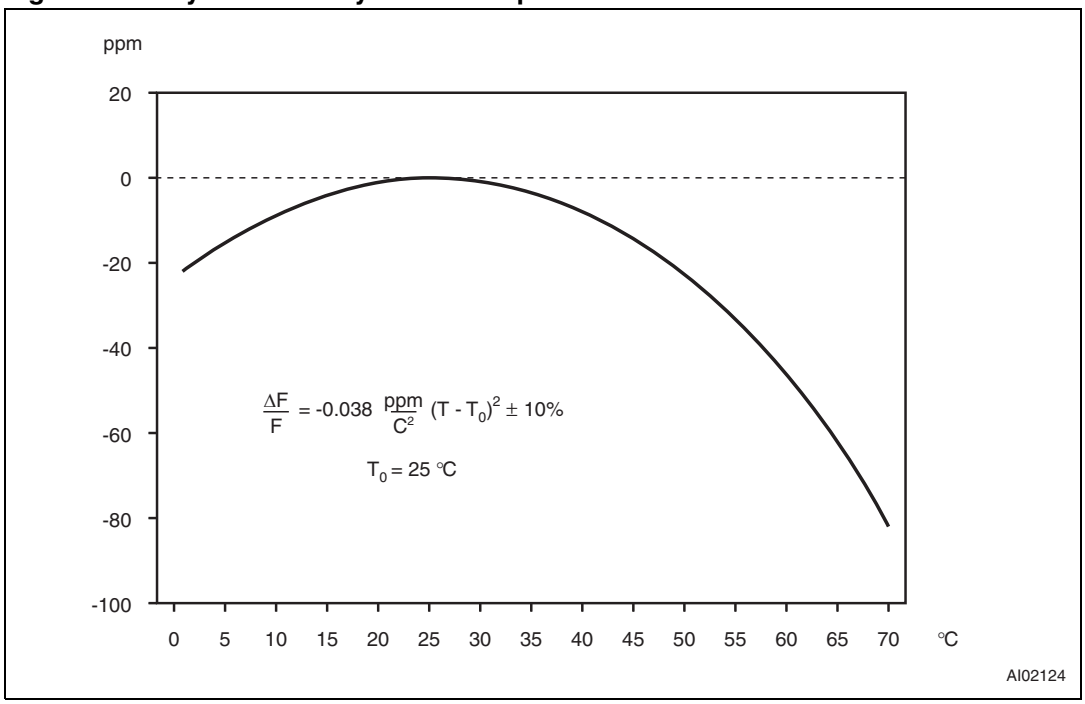
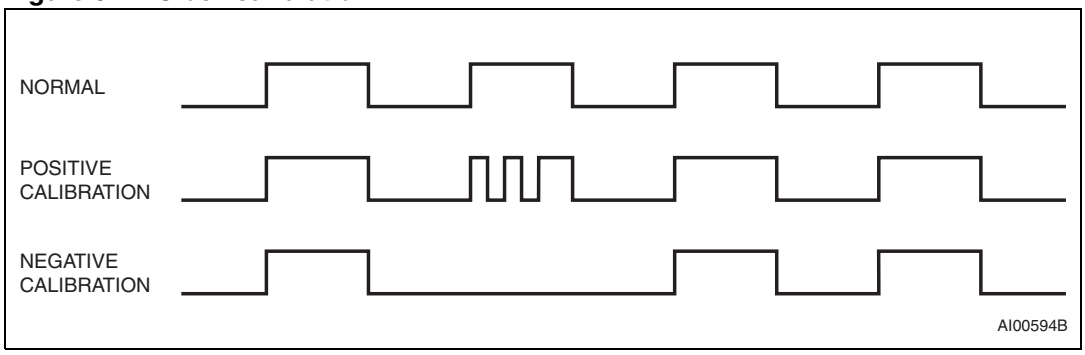


Figure 9. Clock calibration

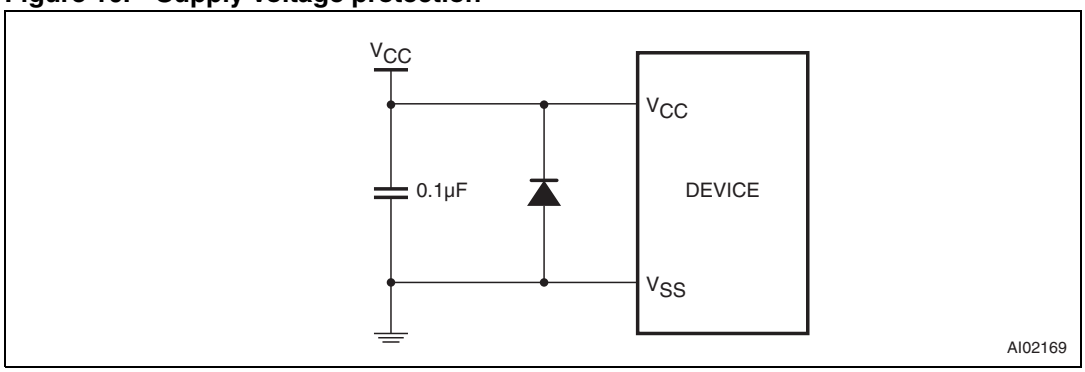


3.6 V_{CC} noise and negative going transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A bypass capacitor value of 0.1 µF (as shown in *Figure 10*) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommended to connect a Schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Figure 10. Supply voltage protection



4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

Symbol	Parameter		Value	Unit
T_A	Ambient operating temperature	Grade 1	0 to 70	°C
		Grade 6	–40 to 85	°C
T_{STG}	Storage temperature (V_{CC} off, oscillator off)		–40 to 85	°C
T_{SLD} (1)(2)(3)	Lead solder temperature for 10 seconds		260	°C
V_{IO}	Input or output voltages	M48T35	–0.3 to 7	V
		M48T35Y	–0.3 to 7	V
V_{CC}	Supply voltage	M48T35	–0.3 to 7	V
		M48T35Y	–0.3 to 7	V
I_O	Output current		20	mA
P_D	Power dissipation		1	W

1. For DIP package, soldering temperature of the IC leads is to not exceed 260 °C for 10 seconds. Furthermore, the devices shall not be exposed to IR reflow nor preheat cycles (as performed as part of wave soldering). ST recommends the devices be hand-soldered or placed in sockets to avoid heat damage to the batteries.
2. For DIP packaged devices, ultrasonic vibrations should not be used for post-solder cleaning to avoid damaging the crystal.
3. For SOH28 package, lead-free (Pb-free) lead finish: reflow at peak temperature of 260 °C (the time above 255 °C must not exceed 30 seconds).

Caution: *Negative undershoots below –0.3 V are not allowed on any pin while in the battery backup mode.*

Caution: *Do NOT wave solder SOIC to avoid damaging SNAPHAT® sockets.*

5 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 7. Operating and AC measurement conditions

Parameter	M48T35	M48T35Y	Unit
Supply voltage (V_{CC})	4.75 to 5.5	4.5 to 5.5	V
Ambient operating temperature (T_A)	0 to 70	–40 to 85	°C
Load capacitance (C_L)	100	100	pF
Input rise and fall times	≤ 5	≤ 5	ns
Input pulse voltages	0 to 3	0 to 3	V
Input and output timing ref. voltages	1.5	1.5	V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 11. AC measurement load circuit

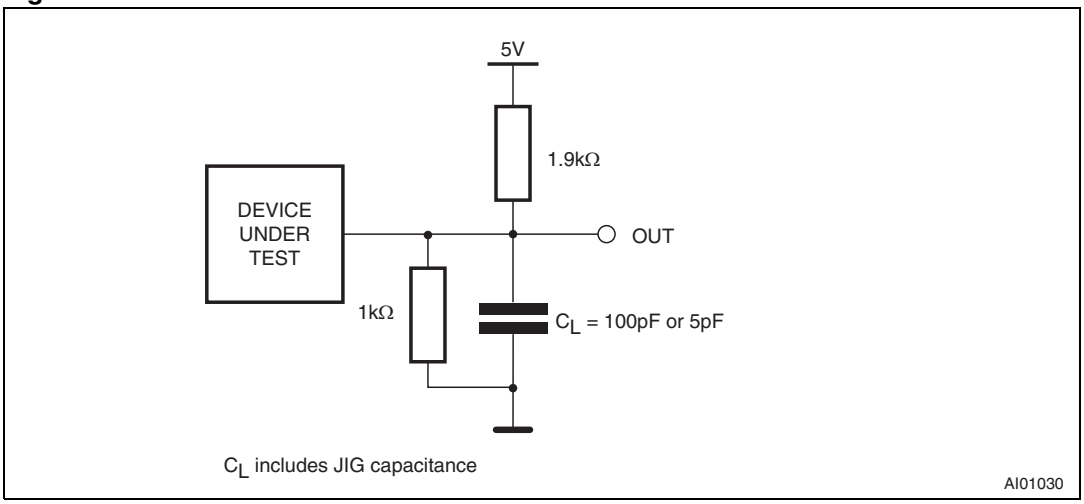


Table 8. Capacitance

Symbol	Parameter[1][2]	Min	Max	Unit
C_{IN}	Input capacitance	-	10	pF
C_{OUT}[3]	Output capacitance	-	10	pF

1. Effective capacitance measured with power supply at 5 V; sampled only, not 100% tested.
2. At 25 °C, f = 1 MHz.
3. Outputs deselected.

Table 9. DC characteristics

Symbol	Parameter	Test condition(1)	M48T35		M48T35Y		Unit
			Min	Max	Min	Max	
I_{LI}	Input leakage current	$0 V \le V_{IN} \le V_{CC}$		±1		±1	µA
I_{LO}(2)	Output leakage current	$0 V \le V_{OUT} \le V_{CC}$		±1		±1	µA
I_{CC}	Supply current	Outputs open		50		30	mA
I_{CC1}	Supply current (standby) TTL	$\overline{E} = V_{IH}$		3		3	mA
I_{CC2}	Supply current (standby) CMOS	$\overline{E} = V_{CC} - 0.2 V$		2		2	mA
V_{IL}	Input low voltage		–0.3	0.8	–0.3	0.8	V
V_{IH}	Input high voltage		2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA		0.4		0.4	V
V_{OH}	Output high voltage	I_{OH} = –1 mA	2.4		2.4		V

1. Valid for ambient operating temperature: T_A = 0 to 70 or –40 to 85 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
2. Outputs deselected.

Figure 12. Power down/up mode AC waveforms

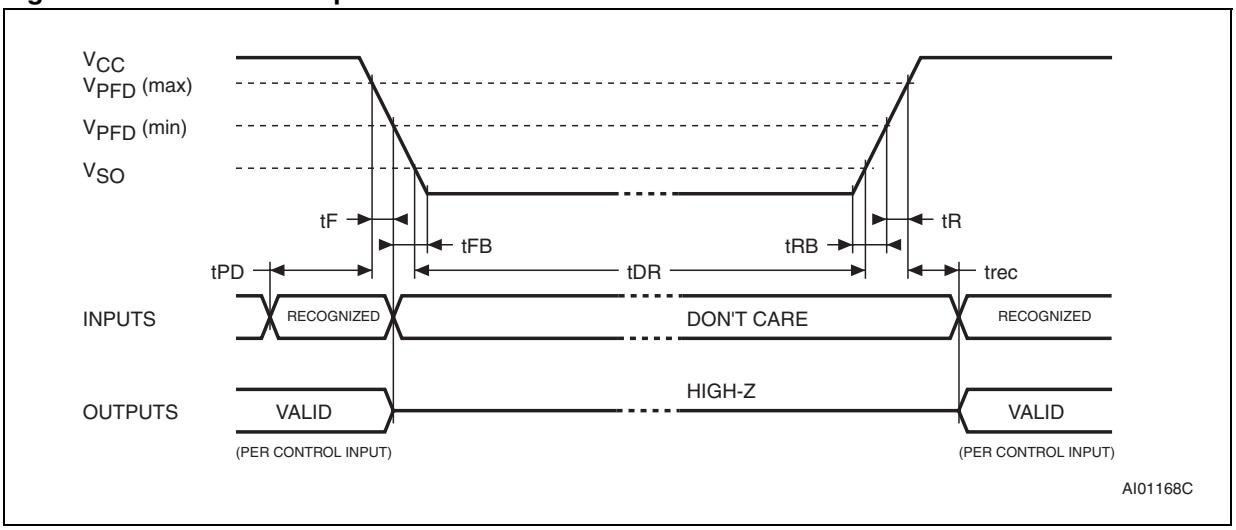


Table 10. Power down/up AC characteristics

Symbol	Parameter[1]		Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before power down		0		µs
t_F[2]	V_{PFD} (max) to V_{PFD} (min) V_{CC} fall time		300		µs
t_{FB}[3]	V_{PFD} (min) to V_{SS} V_{CC} fall time	M48T35	10		µs
		M48T35Y	10		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} rise time		10		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} rise time		1		µs
t_{rec}[4]	V_{PFD} (max) to inputs recognized		40	200	ms

1. Valid for ambient operating temperature: T_A = 0 to 70 or –40 to 85 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.
4. t_{rec} (min) = 20 ms for industrial temperature grade 6 device.

Table 11. Power down/up trip points DC characteristics

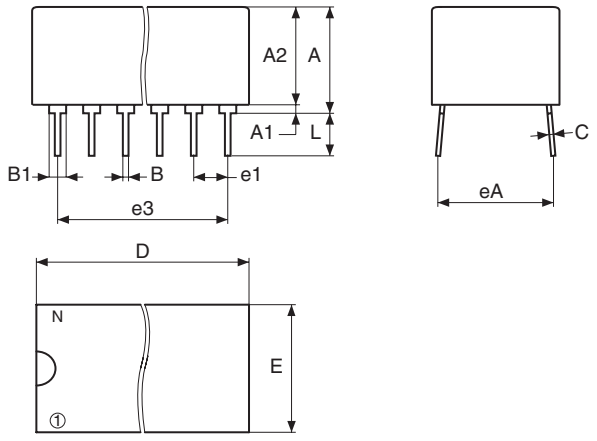
Symbol	Parameter[1][2]		Min	Typ	Max	Unit
V_{PFD}	Power-fail deselect voltage	M48T35	4.5	4.6	4.75	V
		M48T35Y	4.2	4.35	4.5	V
V_{SO}	Battery backup switchover voltage	M48T35		3.0		V
		M48T35Y		3.0		V
t_{DR}[3][5]	Expected data retention time	Grade 1	10[4]			Years
		Grade 6	10[5]			Years

1. Valid for ambient operating temperature: T_A = 0 to 70 or –40 to 85 °C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).
2. All voltages referenced to V_{SS}.
3. CAPHAT™ and M4T32-BR12SH1 SNAPHAT® only, M4T28-BR12SH1 SNAPHAT® top t_{DR} = 7 years (typ).
4. Using larger M4T32-BR12SH6 SNAPHAT® top (recommended for industrial temperature range - grade 6 device).
5. At 25 °C, V_{CC} = 0 V.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 13. PCDIP28 – 28-pin plastic DIP, battery CAPHAT™, package outline

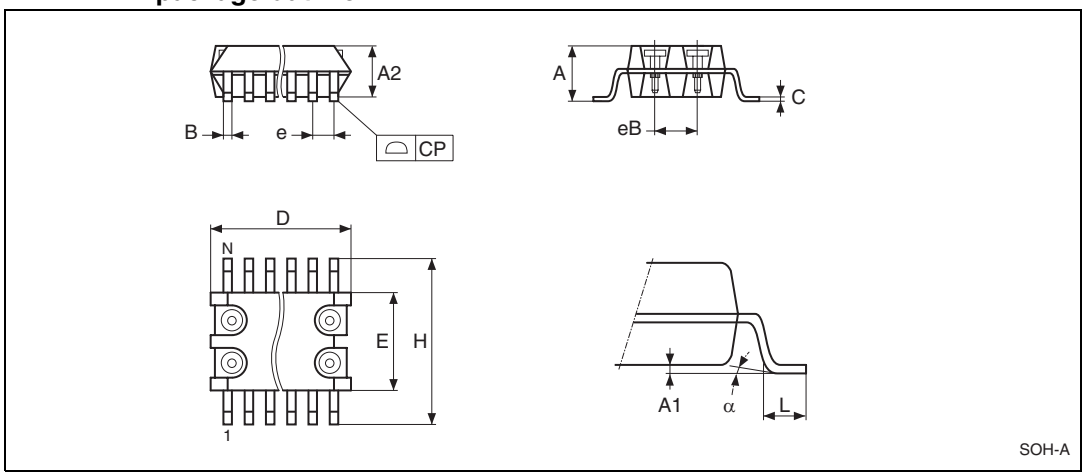


Note: Drawing is not to scale.

Table 12. PCDIP28 – 28-pin plastic DIP, battery CAPHAT™, package mech. data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3	33.02			1.3		
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

Figure 14. SOH28 – 28-lead plastic small outline, 4-socket battery SNAPHAT®, package outline

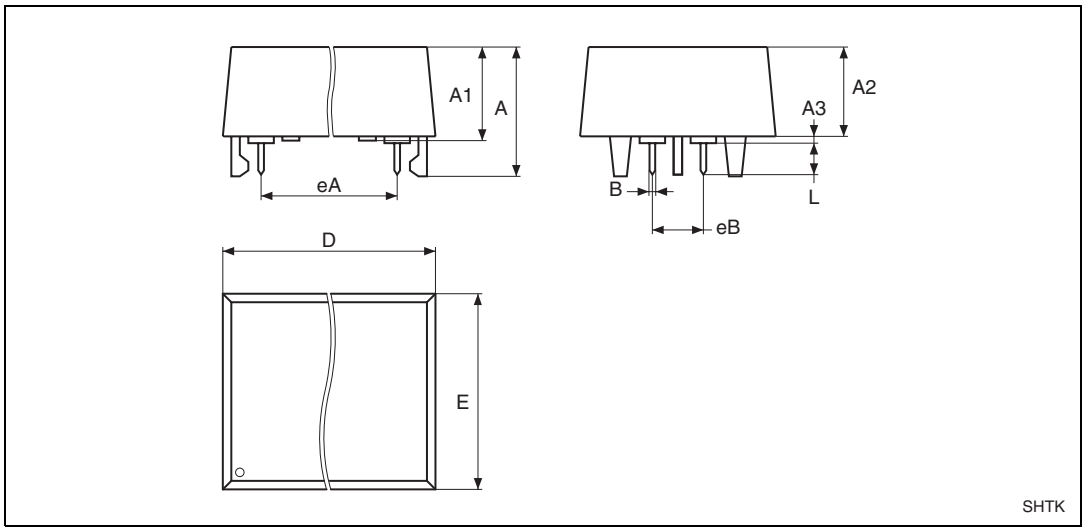


Note: Drawing is not to scale.

Table 13. SOH28 – 28-lead plastic SO, 4-socket battery SNAPHAT®, package mechanical data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
a		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

Figure 15. SH – 4-pin SNAPHAT® housing for 48 mAh battery & crystal, package outline

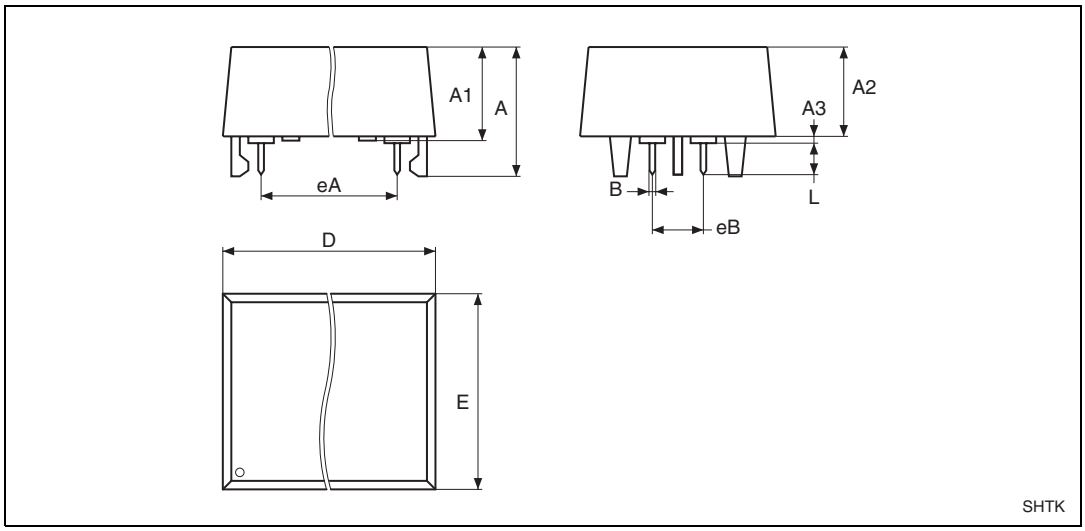


Note: Drawing is not to scale.

Table 14. SH – 4-pin SNAPHAT® housing for 48 mAh battery & crystal, package mechanical data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

Figure 16. SH – 4-pin SNAPHAT® housing for 120 mAh battery & crystal, package outline



Note: Drawing is not to scale.

Table 15. SH – 4-pin SNAPHAT® housing for 120 mAh battery & crystal, package mechanical data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54			0.415
A1		8.00	8.51		0.315	0.335
A2		7.24	8.00		0.285	0.315
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	0.710
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

7 Part numbering

Table 16. Ordering information scheme

Example: M48T 35 –70 PC 1 E

Device type

M48T

Supply voltage and write protect voltage

35(1) = V_{CC} = 4.75 to 5.5 V; V_{PFD} = 4.5 to 4.75 V

35Y(2) = V_{CC} = 4.5 to 5.5 V; V_{PFD} = 4.2 to 4.5 V

Speed

–70 = 70 ns

Package

PC = PCDIP28

MH(3) = SOH28

Temperature range

1 = 0 to 70 °C

6(4) = –40 to 85 °C

Shipping method

For SOH28:

E = ECOPACK® package, tubes

F = ECOPACK® package, tape & reel

For PCDIP28:

blank = ECOPACK® package, tubes

1. The M48T35 part is offered only in the PCDIP28 (i.e. CAPHAT™) package.
2. The M48T35Y is available only in the SOH28 (i.e. SNAPHAT SOIC) package.
3. The SOIC package (SOH28) requires the SNAPHAT® battery package which is ordered separately under the part number “M4TXX-BR12SH” (see *Table 17 on page 25*).
4. Temperature grade 6 (–40 to +85 °C) devices are not for new design. Contact ST sales office for availability.

Caution: Do not place the SNAPHAT battery package “M4TXX-BR12SH” in conductive foam as it will drain the lithium button-cell battery.

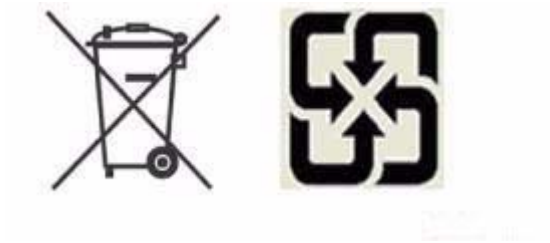
For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

Table 17. SNAPHAT® battery table

Part number	Description	Package
M4T28-BR12SH	Lithium battery (48 mAh) SNAPHAT®	SH
M4T32-BR12SH	Lithium battery (120 mAh) SNAPHAT®	SH

8 Environmental information

Figure 17. Recycling symbols



This product contains a non-rechargeable lithium (lithium carbon monofluoride chemistry) button cell battery fully encapsulated in the final product.

Recycle or dispose of batteries in accordance with the battery manufacturer's instructions and local/national disposal and recycling regulations.

9 Revision history

Table 18. Document revision history

Date	Revision	Changes
Nov-1999	1	First issue
07-Feb-2000	1.1	t_{DR} description changed (*Table 9*)
04-Jun-2001	2	Reformatted; temp/voltage info. added to tables (*Table 8*, *9*, *3*, *4*, *10*, *11*); add century bit text
31-Jul-2001	2.1	Formatting changes based on latest document reviews
06-Mar-2002	2.2	Add PMDIP packaging option, which is “Not for New Design” (NND) (*Table 16*)
20-May-2002	2.3	Modify reflow time and temperature footnotes (*Table 6*)
26-Jun-2002	2.4	Add footnote to table (*Table 11*)
31-Mar-2003	3	v2.2 template applied; data retention condition updated (*Table 11*)
10-Dec-2003	4	Reformatted; update DC characteristics (*Table 9*)
31-Mar-2004	5	Reformatted; update Pb-free package information (*Table 6*, *16*)
05-Dec-2005	6	Updated template, lead-free text, and remove footnote (*Table 9*, *16*)
01-Aug-2007	7	Reformatted; added lead-free second level interconnect information to cover page and *Section 6: Package mechanical data*.
12-Feb-2009	8	Updated *Table 6*; text in *Section 6: Package mechanical data*; added *Section 8: Environmental information*; minor formatting changes.
08-Sep-2010	9	Reformatted document; updated *Section 4*, *Table 12*, *16*; removed PMDIP28 package.
07-Jun-2011	10	Updated footnote *1* of *Table 6: Absolute maximum ratings*; updated *Section 8: Environmental information*.

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AN926
APPLICATION NOTE

Brand Traceability with for NVRAM Products

INTRODUCTION

To ensure traceability to specific assembly and test operations, ST clearly brands a date code on every device, as well as an encapsulation code on CAPHAT™ products. STMicroelectronics is implementing a new marking and traceability scheme due to the sizes of the packages as well as increases in the number of fabrication, assembly, and test sites.

The devices are marked with a trace code which provides for tracking the exact versions. The current device marking formats for our package options are shown in Figures 1 to Figure 8., page 4.

Table 1. Current Packages and Marking Information

Package Type	Figure	Marking Information
QFN	1	1-digit Year, 2-digit Work Week
8-Lead SOIC and TSSOP	2	1-character Assembly Site, 1-digit Year, 2-digit Work Week
16-Lead SOIC	3	2-digit Assembly Site, 1-digit Year, 2-digit Work Week
SOT	4	3-digit Part Number, 1-digit Work Week
24-/28-Pin CAPHAT™, 24-/44-Pin SOIC, 18-/28-Pin SOX, and 32-/36-Pin Hybrid	5	2-digit Assembly Site, 3-digit Lot Number, 2-digit Wafer Fab Site
		3-character Country of Origin, 2-digit Test Site, 1-digit Year, 2-digit Work Week
CAPHAT™ Encapsulation	6	Assembly, Test Temperature, Julian Date, Sequential Lot ID
SNAPHAT®	7	2-digit Assembly Site, 3-digit Lot Number
		3-character Country of Origin, 2-digit Test Site, 1-digit Year, 2-digit Work Week
Shipping Box Traceability	8	2-digit Assembly Site, 1-digit Year, 2-digit Work Week, 3-digit Lot Number

TABLE OF CONTENTS

NEW MARKING ILLUSTRATIONS

Figure 1. QFN Package Date Code

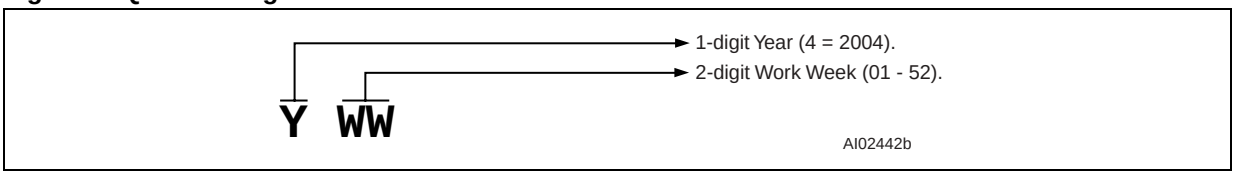


Figure 2. 8-Lead SOIC and TSSOP Date and Assembly Site Code

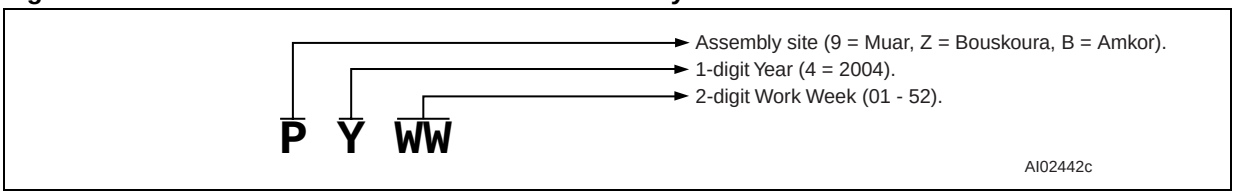


Figure 3. 16-Lead SOIC Date and Assembly Site Code

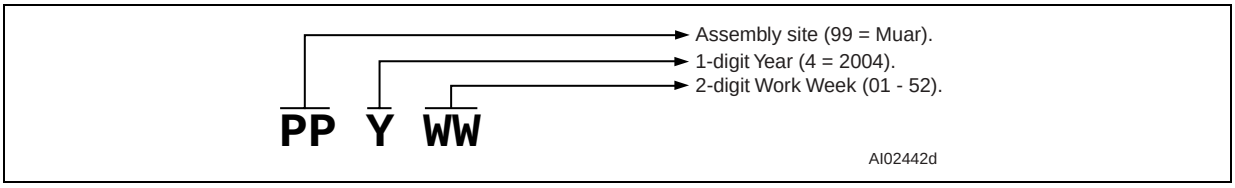


Figure 4. SOT Date and Part Number Code

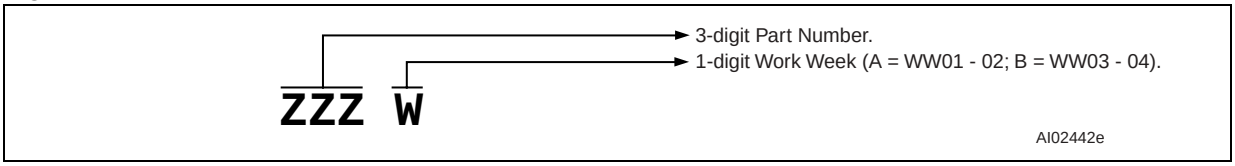


Figure 5. 24-/28-Pin CAPHAT™, 24-/44-Pin SOIC, 18-/28-Pin SOX, and 32-/36-Pin Hybrid Code

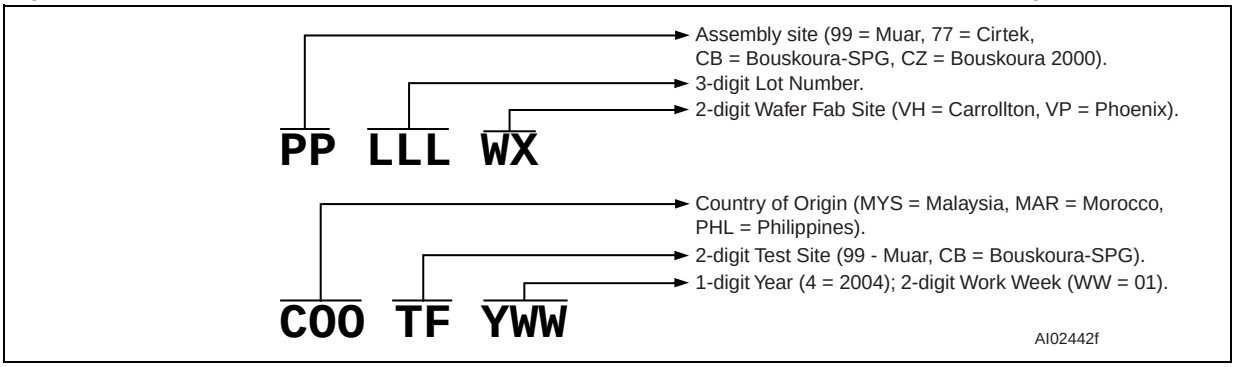
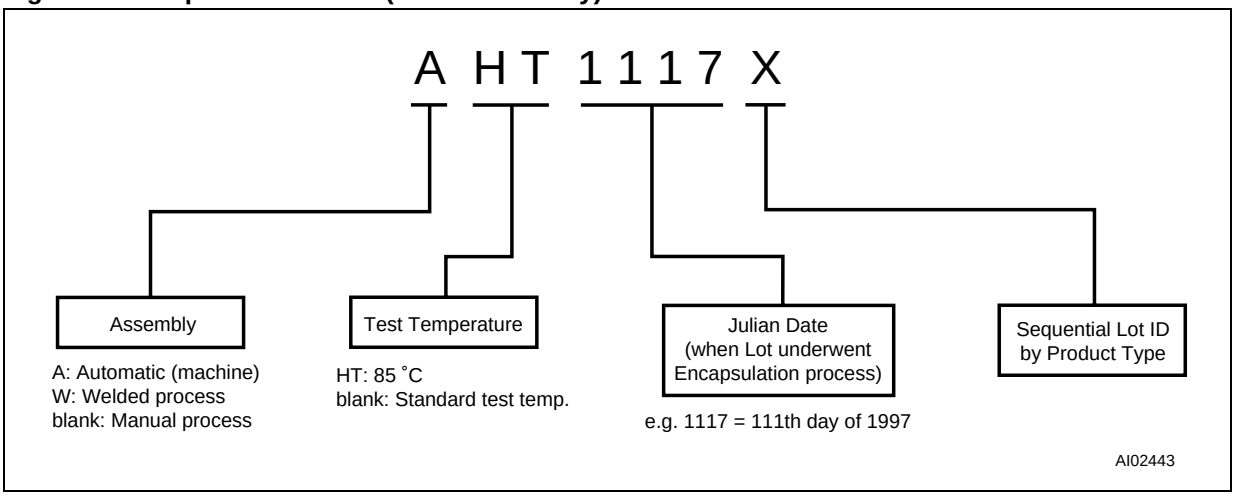


Figure 6. Encapsulation Code (CAPHAT™ only)



Note: The 5- to 8-character encapsulation code (CAPHAT™ only; Figure 6) is positioned at the end of the device and is placed perpendicularly to the date code. It summarizes details of the encapsulation process.

Figure 7. SNAPHAT®

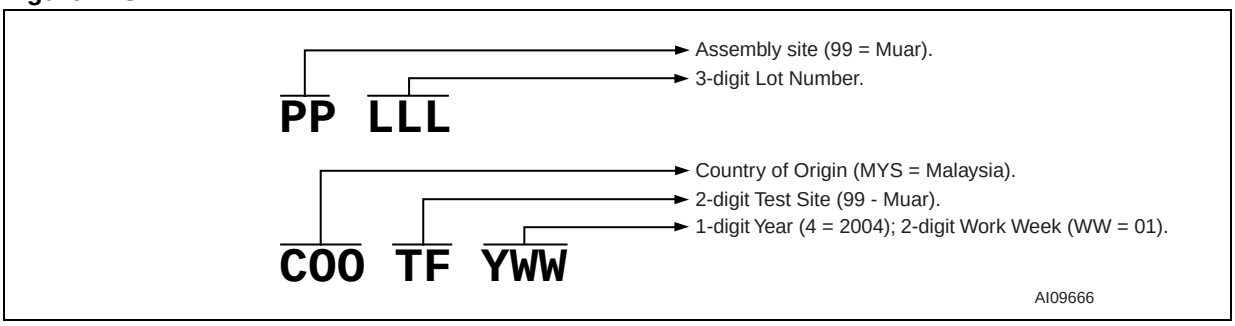
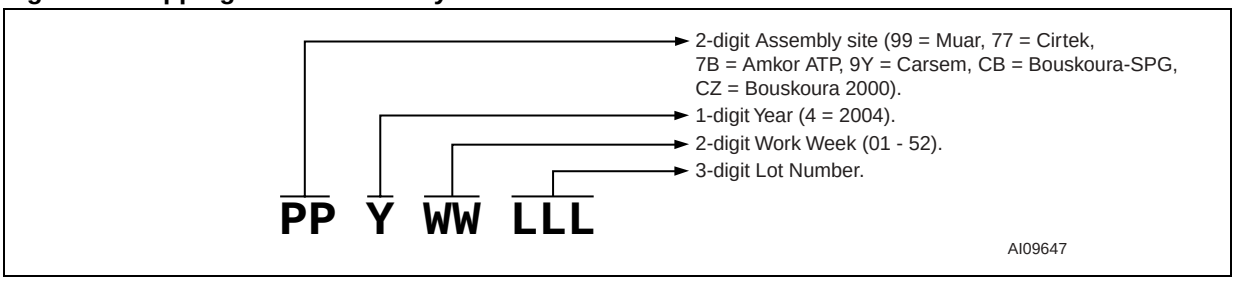


Figure 8. Shipping Box Traceability Date Code Format



PREVIOUS (OBSOLETE) MARKING INFORMATION

The 9-character date code (Figure 9) is positioned at the top of the label, beside the ST logo. This presents a complete facility identification, as well as a final-test time-line of the device's manufacturing process.

The 7-character code (SOIC only; Figure 10) is positioned in the bottom line closest to Pin 1 on the device. It represents the lots' overall fabrication history.

Figure 9. Date Code

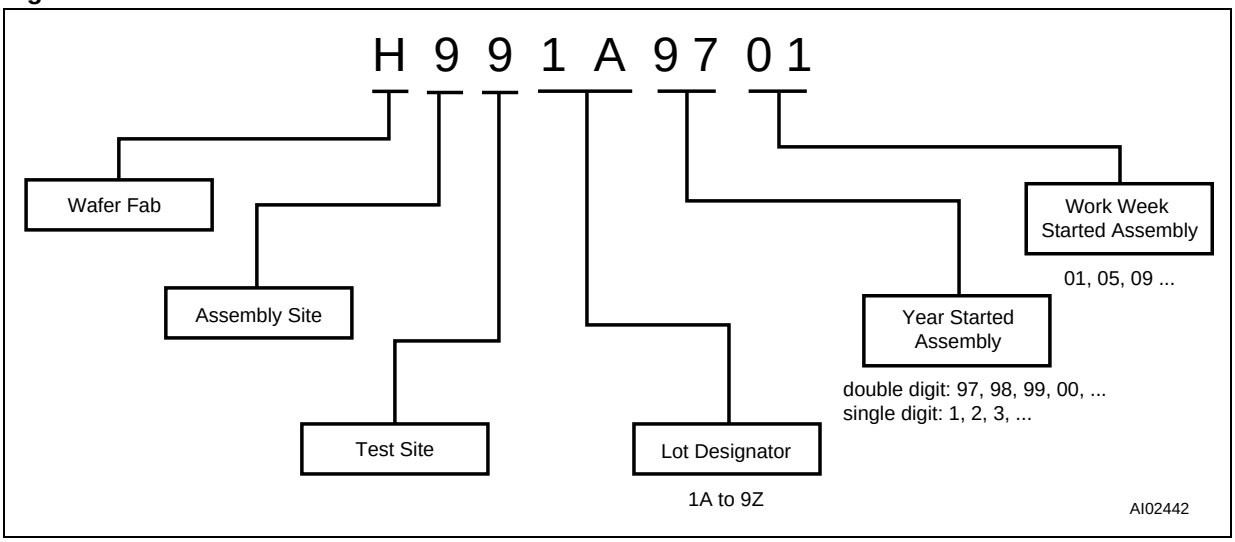


Figure 10. Fab Lot Number

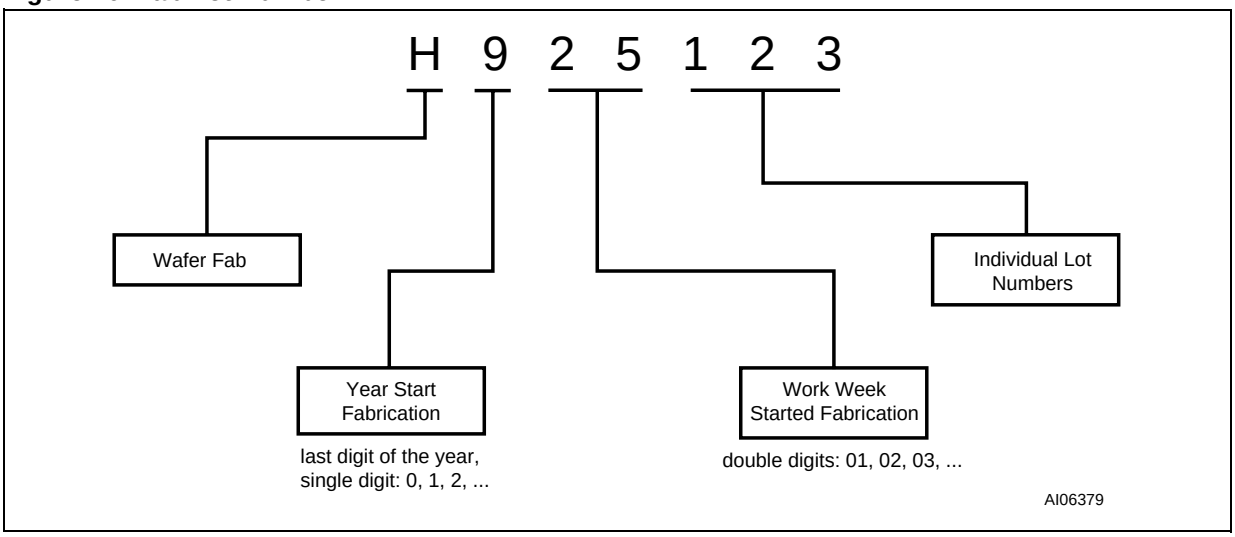
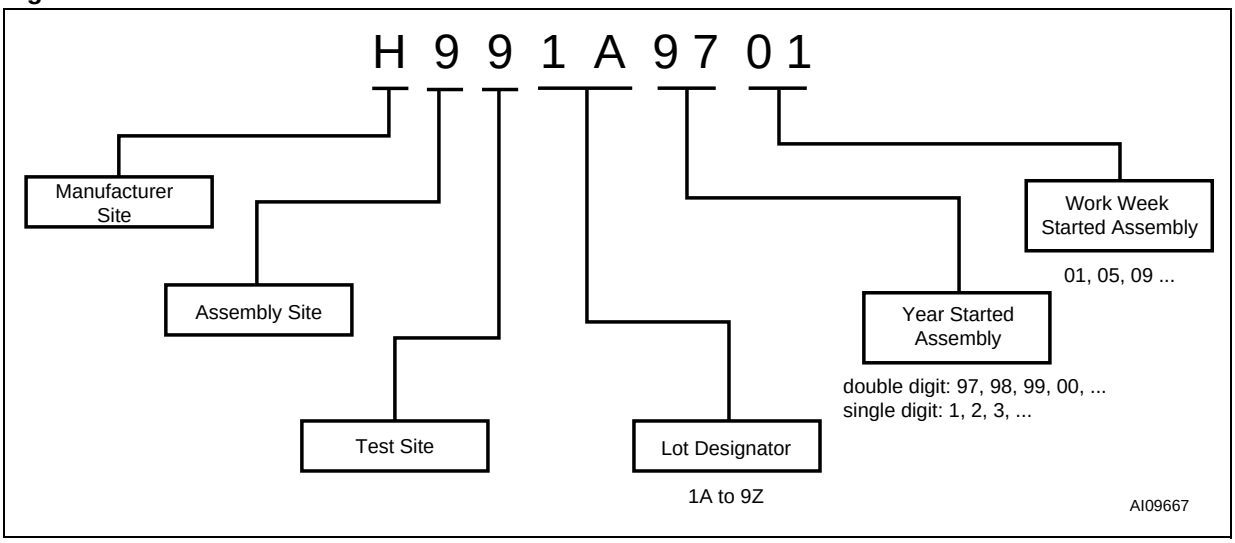


Figure 11. SNAPHAT®



REVISION HISTORY

Table 2. Document Revision History

Date	Version	Revision Details
February 2002	1.0	First Issue
26-Jul-02	1.1	Updated date code (Figure 1)
03-Feb-03	1.2	Updated date code, fab lot number (Figure 1, 10)
14-Mar-03	1.3	Clarify lot number terminology (Figure 10)
02-Jul-04	2.0	Reformatted; marking formats updated (Figure 1, 2, 3, 4, 5, 8)
26-Aug-04	3.0	Updated (Figure 5, 7, 11; Table 1)

If you have any questions or suggestions concerning the matters raised in this document, please send them to the following electronic mail addresses:

ask.memory@st.com (*for general enquiries*)

Please remember to include your name, company, location, telephone number and fax number.

PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MPG/SR/2003004

MATERIAL CHANGE FOR ALL ST ZEROPOWER AND TIMEKEEPER NVRAMS IN DIP24 AND DIP28 CAPHAT PACKAGES

WHAT IS THE CHANGE?

STMicroelectronics is implementing our new ECOPACK® Lead-free plating on all 24-lead and 28-lead CAPHAT™ DIP packaged ZEROPOWER® and TIMEKEEPER® NVRAM devices. These devices will convert from Tin-Lead to pure Tin-plated leadframes.

Note: Here, the term “Lead-free” means free of the element, Lead.

The following devices are affected:

M48T02-70PC1	M48T08-100PC1	M48T58-70PC1	M48Z02-70PC1	M48Z35-70PC1
M48T02-150PC1	M48T08-150PC1	M48T58Y-70PC1	M48Z02-150PC1	M48Z35Y-70PC1
M48T02-200PC1			M48Z02-150PC6	M48Z35AV-10PC1
	M48T18-100PC1	M48T59Y-70PC1	M48Z02-200PC1	
M48T12-70PC1	M48T18-150PC1	M48T59Y-70PC1D		M48Z58-70PC1
M48T12-150PC1		M48T59Y-70PC1DM	M48Z12-70PC1	M48Z58Y-70PC1
M48T12-200PC1	M48T35-70PC1	M48T59Y-70PC1DS	M48Z12-150PC1	M48Z58Y-70PC6
	M48T35Y-70PC1		M48Z12-200PC1	
	M48T35AV-10PC1	M48T86PC1		
			M48Z08-100PC1	
			M48Z18-100PC1	

For new system designs and qualifications, it is recommended that the Lead-free versions of these products be used.

WHY?

These changes are being implemented to make the devices more environmentally friendly.

WHEN?

Production parts could begin shipping as soon as April 1, 2004. Samples are available now. Qualification reports are available for each product family.

Once ST commences production of these Lead-free parts, it will cease production of the versions containing Lead, so customers are strongly encouraged to qualify the Lead-free parts in a timely manner.

Any last time orders for Leaded products needs to placed by Jan 31, 2004.

HOW WILL THE CHANGE BE QUALIFIED?

Qualification is being done according to STMicroelectronics Corporate procedure.

IMPACT ESTIMATION AT USER'S SIDE

These changes should have no impact because the plating technologies used are compatible with both Leaded and Lead-free assembly processes.

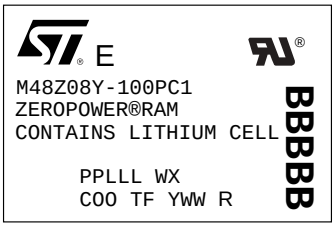
ABOUT TRACEABILITY

The Lead-free parts can be identified in three ways: The letter E (as in ECOPACK®) will appear in the brand. Furthermore, the trace code can be used to determine the time and place of manufacture, and hence the material content. Finally, the Lead-free parts will be labeled in a new format as shown in Figure 1, Figure 2, and Figure 3.

The full trace code per ST's new standard will be shown on the end of the inner bulk box (i.e. box inside shipping carton) as shown in Figure 3.

Figure 1. Lead-free Devices in the CAPHAT™ Package

The Lead-free parts will be labeled with the following format:



- The first row includes the ST logo and the Underwriter's Laboratories logo. At the lower right corner of the ST logo is the letter "E" (as in ECOPACK). Lead-free parts can be identified by the letter "E."
- The second row of text is the salestype (part number).
- The third row is the device family.(1)
- The fourth row identifies it as having a battery.(1,2)

Note: 1. The last two rows comprise the trace code, formatted as in Figure 2 and Figure 3, page 2.
2. The rotated text on the right ("BBBBB") is the battery trace code.

Figure 2. Assembly Site Trace Code (Row 5)

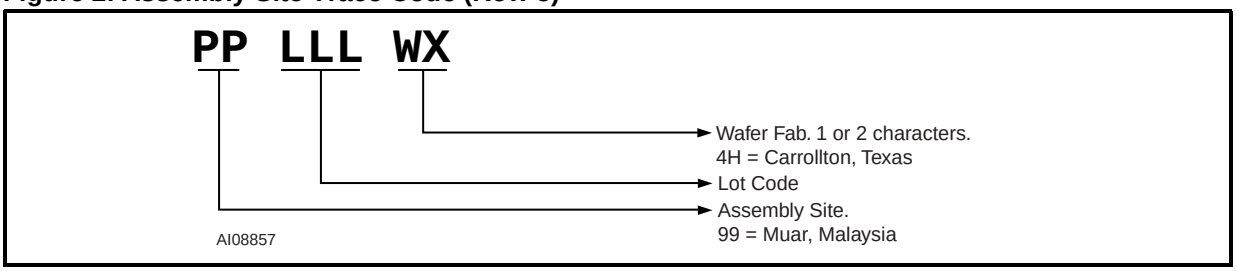


Figure 3. Country of Origin Trace Code (Row 6)

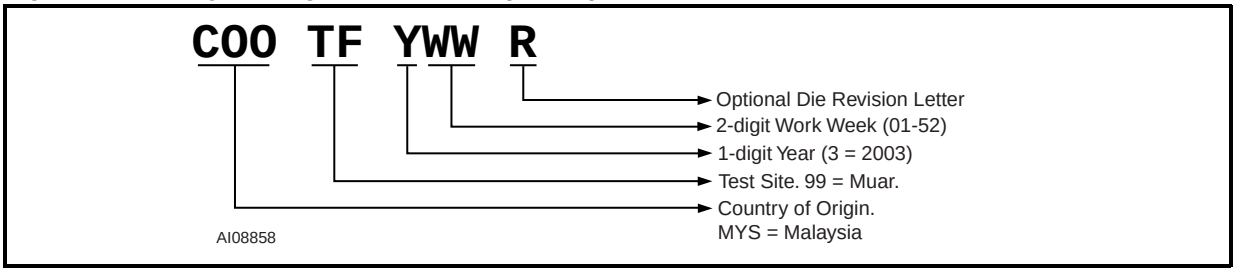
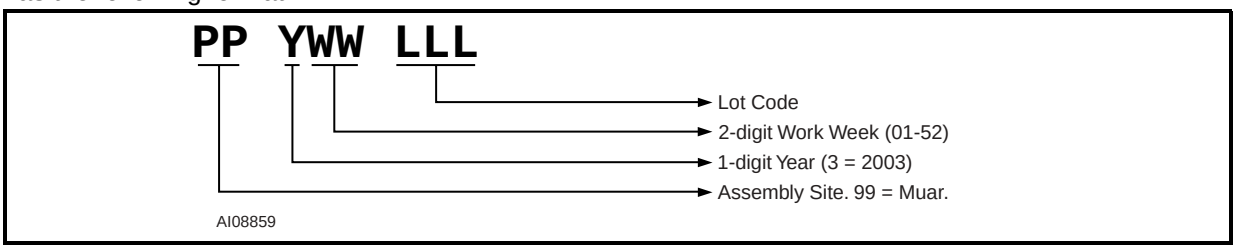


Figure 4. ECOPACK® Label

The inner bulk box will also have an ECOPACK® symbol (indicating Lead-free) on the label which is comprised of a green four-leaf clover and an IC package inserted into the text as shown in Figure 4:

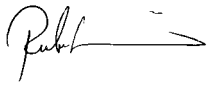
Figure 5. Inner Bulk Box Labeling

The trace code is also contained on the label on the inner bulk box (i.e. box inside shipping carton), and has the following format:



APPENDIX A. PRODUCT / PROCESS CHANGE NOTIFICATION

Ref: MPG/SR/2003004

Sales Type / Product Family:	See attached list.
Customer:	All those using any of the devices listed.
Type of Change:	New Lead-free package
Reason for Change:	To make the devices more environmentally friendly
Description of Change:	New Lead-free package
Forecasted Date of Change:	April 1, 2004
Availability Date of Samples for Customer:	October 1, 2003
Forecasted Date for Internal STMicroelectronics Change Qualification Report Availability:	Now
Marking to Identify Changed Product, e.g. Date Code Change:	See attached.
Description of the Qualification Program:	According to ST Corporate Procedure
Product Line(s) and/or Part Number(s):	See attached list.
Manufacturing Location(s):	Wafer Fabrication: Carrollton, USA Assembly Location: Muar, Malaysia Test Location: Muar, Malaysia
Forecasted Date of Shipment:	April 1, 2004
Division Product Management:	R. SONNINO 
Group Q. A. Manager:	A. PANCHIERI 
Date:	October 2nd, 2003

Customer Acknowledgment of Receipt — Ref: MPG/SR/2003004

Please sign and return to STMicroelectronics Sales Office

❑ Qualification Plan Denied	Name:
❑ Qualification Plan Approved	Title:
	Company:
❑ Change Denied	Date:
❑ Change Approved	Signature:

Corporate Quality Procedure SOP271Rev. G

REVISION HISTORY

Table 1. Document Revision History

Date	Rev. #	Revision Details
October, 2003	1.0	First Issue

CONTACT INFORMATION

If you have any questions or suggestions concerning the matters raised in this document, please send them to the following electronic mail addresses:

apps.nvram@st.com (for application support)

ask.memory@st.com (for general inquiries)

Please remember to include your name, company, location, telephone number, and fax number.

PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MPG/SR/2003005

MATERIAL CHANGE FOR ST SERIAL REAL-TIME CLOCKS AND NVRAM SUPERVISORS IN EMBEDDED CRYSTAL PACKAGES

WHAT IS THE CHANGE?

STMicroelectronics is implementing our new ECOPACK® Lead-free plating on all 28-lead, embedded crystal SOIC (Cirtek, SOX28) packaged Serial Real-Time Clock and NVRAM Supervisor devices. These devices will convert from Tin-Lead to pure Tin-plated leadframes.

Additionally, these devices will have the internal crystal connections welded instead of soldered.

Note: Here, the term “Lead-free” means free of the element, Lead.

The following devices are affected:

M41ST85WMX6	M41ST87YMX6	M41ST95WMX6	M41T81MX6
M41ST85WMX6TR	M41ST87YMX6TR	M41ST95WMX6TR	M41T81MX6TR
M41ST85YMX6			
M41ST85YMX6TR			

For new system designs and qualifications, it is recommended that the Lead-free versions of these products be used.

WHY?

These changes are being implemented to make the devices more environmentally friendly.

WHEN?

Production parts could begin shipping as soon as December, 2003. Samples will be available in late October, 2003. Qualification reports are available now.

Once ST commences production of these Lead-free parts, it will cease production of the versions containing Lead, so customers are strongly encouraged to qualify the Lead-free parts in a timely manner.

HOW WILL THE CHANGE BE QUALIFIED?

Qualification is being done according to STMicroelectronics Corporate procedure.

IMPACT ESTIMATION AT USER'S SIDE

These changes should have no impact because the plating technologies used are compatible with both Leaded and Lead-free reflow processes. The JEDEC MSL is Level 3 with the industry's 260°C reflow requirement of Lead-free reflow processes.

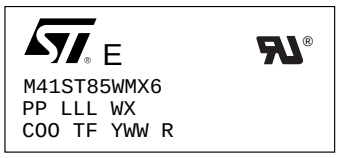
ABOUT TRACEABILITY

Lead-free parts will be marked with an “E” (representing ECOPACK®) branded onto the IC packages. The brand includes the trace code, and has the format shown in Figure 1, Figure 2, and Figure 3.

The trace code will also be shown on the end of the inner bulk box (i.e. box inside shipping carton) as shown in Figure 5.

Figure 1. Lead-free Devices in the SOX28 (Cirtek) Package

The Lead-free SOX28 parts will be labeled with the following format:



The first row includes the ST logo and the Underwriter’s Laboratories logo. At the lower right corner of the ST logo is the letter “E” (as in ECOPACK). Lead-free parts can be identified by the letter “E.”

The second row of text is the salestype (part number).

The third and fourth lines comprise the Assembly Site and Country of Origin trace codes.

Figure 2. Assembly Site Trace Code (Row 3)

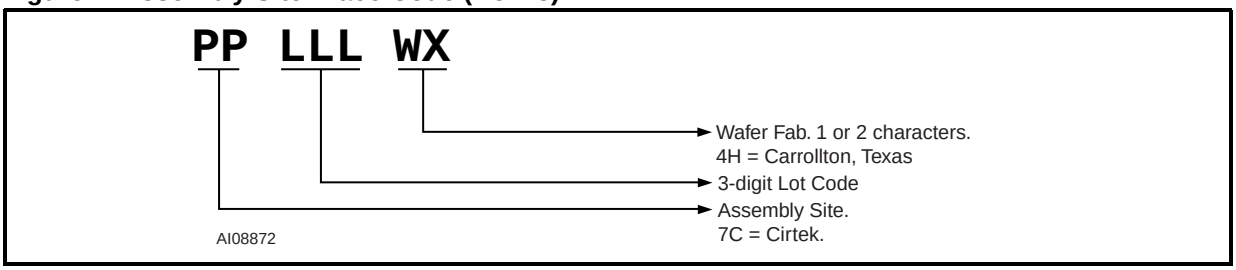


Figure 3. Country of Origin Trace Code (Row 4)

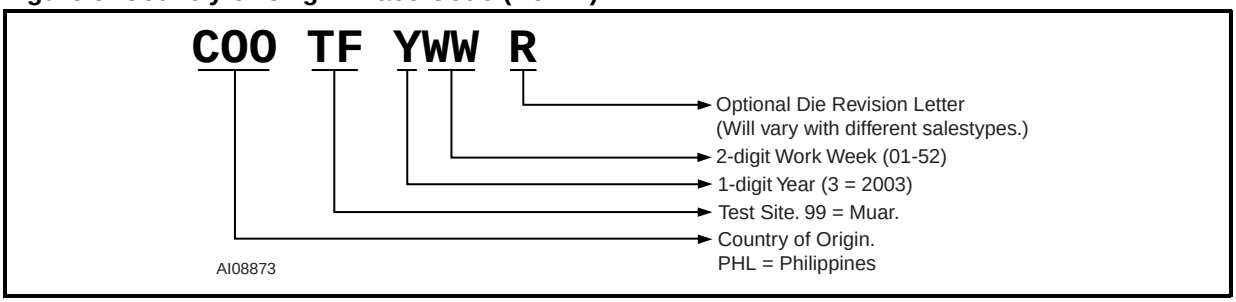
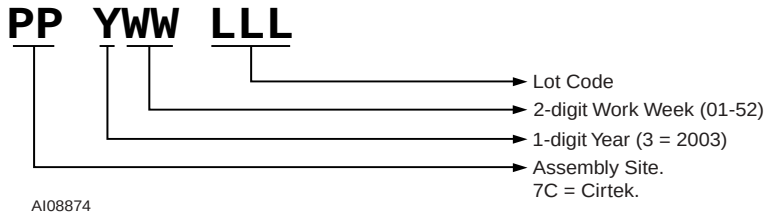


Figure 4. ECOPACK® Label

The inner bulk box will also have an ECOPACK® symbol (indicating Lead-free) on the label which is comprised of a green four-leaf clover and an IC package inserted into the text as shown in Figure 4:

Figure 5. Inner Bulk Box Labeling

The trace code is also contained on the label on the inner bulk box (i.e. box inside shipping carton), and has the following format:



APPENDIX A. PRODUCT / PROCESS CHANGE NOTIFICATION

Ref: MPG/SR/2003005

Sales Type / Product Family:	See attached list.
Customer:	All those using any of the devices listed.
Type of Change:	New Lead-free package and change to welded crystal attach process
Reason for Change:	To make the devices more environmentally friendly
Description of Change:	New Lead-free package
Forecasted Date of Change:	December, 2003
Availability Date of Samples for Customer:	October, 2003
Forecasted Date for Internal STMicroelectronics Change Qualification Report Availability:	October, 2003
Marking to Identify Changed Product, e.g. Date Code Change:	See attached.
Description of the Qualification Program:	According to ST Corporate Procedure
Product Line(s) and/or Part Number(s):	See attached list.
Manufacturing Location(s):	Wafer Fabrication: Carrollton, USA Assembly Location: Cirtek, Philippines Test Location: Muar, Malaysia
Forecasted Date of Shipment:	December, 2003
Division Product Management:	R. SONNINO
Group Q. A. Manager:	A. PANCHIERI
Date:	October 30, 2003

Customer Acknowledgment of Receipt — Ref: MPG/SR/2003005

Please sign and return to STMicroelectronics Sales Office

❑ Qualification Plan Denied	Name:
❑ Qualification Plan Approved	Title:
	Company:
❑ Change Denied	Date:
❑ Change Approved	Signature:

Corporate Quality Procedure SOP271Rev. G

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Please remember to include your name, company, location, telephone number, and fax number.

AN1011
Application note

Battery technology used in NVRAM and real-time clock (RTC) products from ST

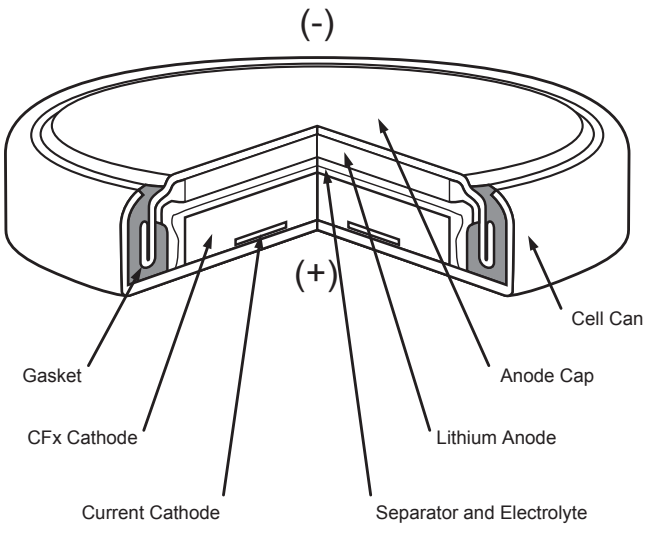
Introduction

Lithium Carbon MonoFlouride (LiCFx) batteries are used by STMicroelectronics in their ZEROPOWER® and TIMEKEEPER® NVRAM devices and in their serial real-time clock (RTC) devices. The batteries provide the backup power to maintain the static RAM arrays and to keep the oscillators running in the TIMEKEEPER and serial RTC devices.

When the discharge rates are low, these non-rechargeable lithium batteries are capable of maintaining a highly reliable voltage level for many years. Lithium batteries, therefore, are used for a variety of applications that require battery backup without need of maintenance for many years.

To be used in electronic components, these cells also need to be composed of constituents that are nontoxic, non-corrosive, and non-explosive. They also must be chemically and thermally stable before, during and after discharge. STMicroelectronics utilizes the 48 mAh BR1225X cell, and the 120 mAh BR1632 cell. The electrolyte of these cells (see *Figure 1*) is based on an organic solvent, instead of a corrosive alkaline or acidic solution found in most conventional batteries. This greatly improves the cell's leakage resistance and guards against the negative effects caused by leakage.

Figure 1. Cell cross-section



Contents

Characterization and modeling

STMicroelectronics has conducted extensive tests on these cells, a great proportion being destructive testing. Three main mechanisms of battery degradation were modeled to establish the effects under various loads, temperatures (up to 85 °C) and other environmental variables:

- Active lifetime of the cell, as a result of the consumption of the lithium anode
- Shelf life (storage lifetime) of the cell, as a result of the electrolyte drying up (evaporation)
- Self-discharge, as a result of small leakage currents inherent to the battery chemistry

The weight loss proved to be a valuable measure of electrolyte evaporation. Self-discharge is specified by the battery manufacturer to be less than 0.3% per year.

Models were then developed to predict the rate of electrolyte loss and what effect encapsulation of the cell would have. Tests on the cells, when encapsulated in the epoxy used in the SNAPHAT process, have demonstrated a significant reduction in electrolyte evaporation.

Figure 2. (A) BR1225X discharge rate (B) BR1632 discharge rate

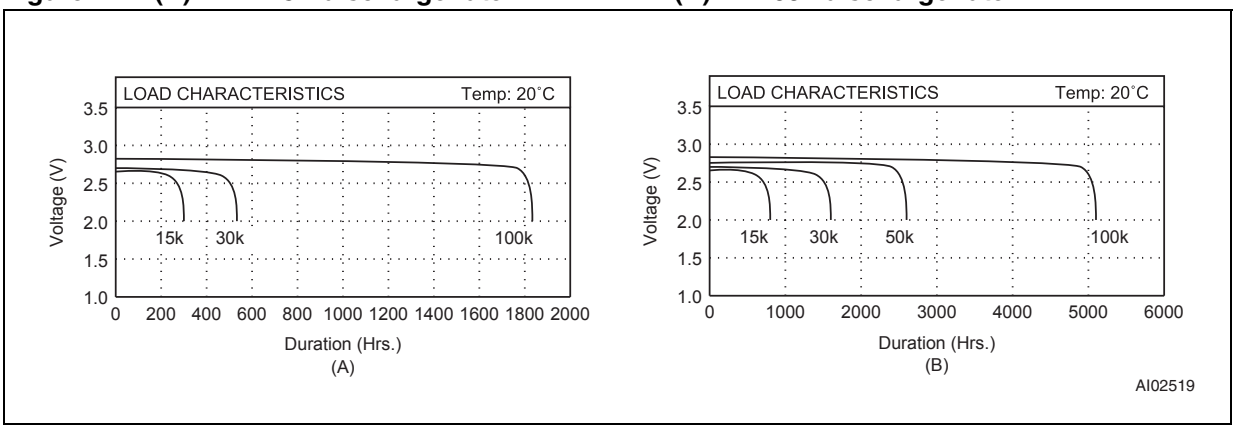


Figure 3 shows the load discharge graphs taken at 20 °C. As can be seen, both cells produce a nominal 3 V output with a flat discharge curve until the end of their effective lives, and so confirms that both are suitable for providing battery backup to low leakage CMOS SRAMs.

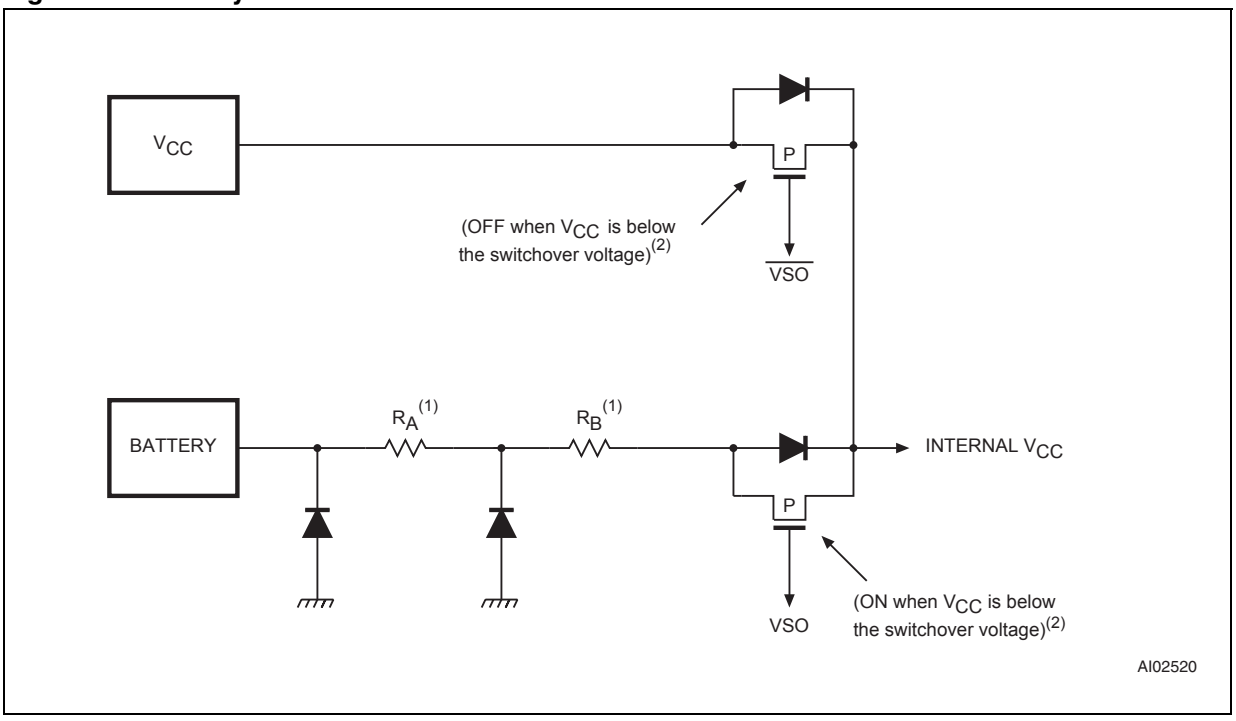
The battery lifetime of individual ZEROPOWER, TIMEKEEPER and RTC devices, as described in AN1012, is a function of the current load, the battery selected and the system duty cycle. System life, which even with 100% duty cycle can still be greater than ten years, is specified in the datasheet for each device.

UL 1950/60950 validation

All ZEROPOWER, TIMEKEEPER and RTC devices are recognized by the Underwriters Laboratory Inc. UL 1950/60950 specification. The conditions for acceptance under this include the following:

1. That the devices are intended for use as components where the replacement of the battery can be performed by the operator or a trained technician.
2. That the devices are intended for use as components in low voltage, isolated, secondary circuits; where the case temperature does not exceed 100 °C, and the voltage on any pin, relative to ground, does not exceed 7 V_{DC}.
3. That the devices are intended to be mounted on a printed wiring board, flame rated to a minimum of 94 V-1.
4. That the devices are provided with an appropriate on-chip, reverse current protection circuit. (See *Figure 3* for the circuit diagram.)

Figure 3. Battery control circuit



1. R_A is the ESD protection resistor and R_B is the battery protection resistor required by UL.
2. Depending on the device, switchover will be a function of battery voltage or set by a fixed reference.

Battery status for NVRAMs and serial RTCs

For the devices listed in *Table 1* and *2*, the battery can be internal or external to the IC package. In the external cases, the battery will either be a user-supplied battery or it may be incorporated into ST's SNAPHAT package which mates to the underlying IC as depicted in *Figure 6 on page 6*.

Figure 4 shows the CAPHAT IC package with the battery integrated with the IC. In this package, the battery is encapsulated within the device.

Figure 5 is representative of several IC packages all of which use a customer-supplied, external battery. None of these device types include the battery in the IC package.

Figure 6 on page 6 shows ST's SNAPHAT SOH28 (SOIC) package with mating SNAPHAT battery top. Here, there is no battery in the IC package. Instead, it is a separate, removable/replaceable unit stacked on top of the IC which reduces board space.

Figure 4. CAPHAT IC package

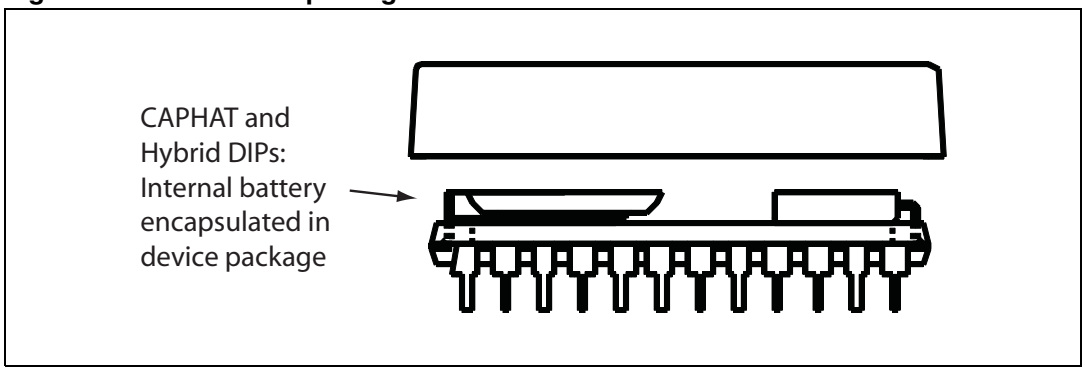


Figure 5. External battery, user supplied

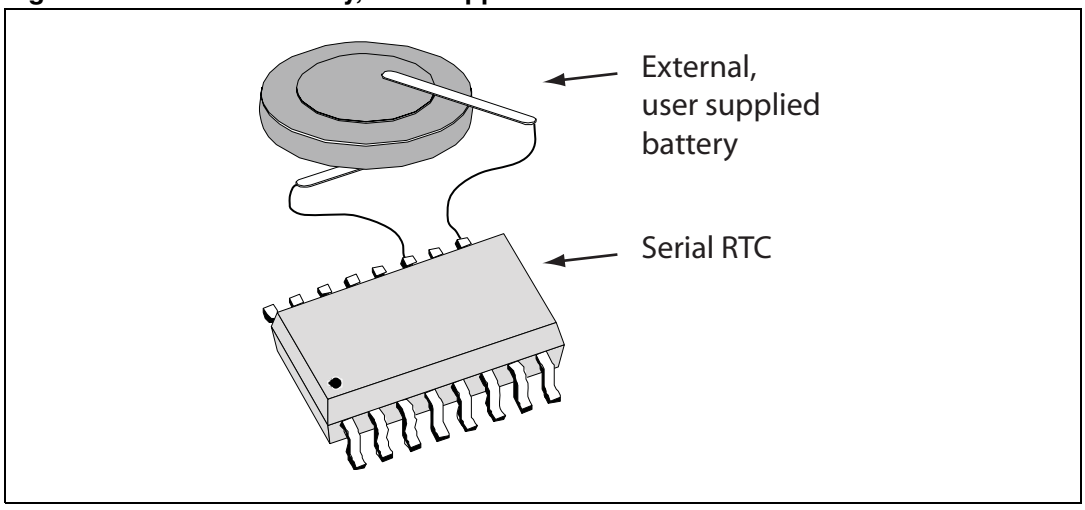


Figure 6. External battery, SNAPHAT battery top

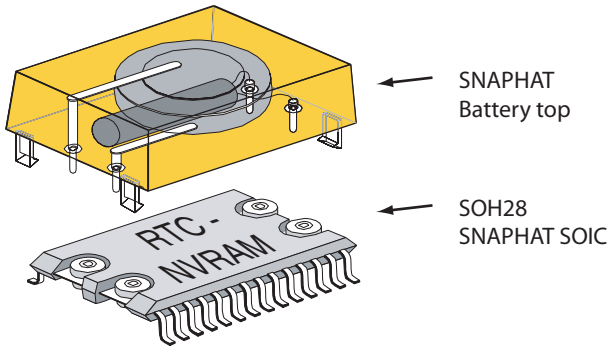


Table 1. Battery status for serial RTCs

Part number	Package	Battery status
M41ST84WMQ6E	SO-16	External, user supplied
M41ST84WMQ6F		
M41ST85WMH6E	SOH28 (330 mil)	External, SNAPHAT
M41ST85WMH6F		
M41ST85WMX6	SOX28 (300 mil)	External, user supplied
M41ST85WMX6TR		
M41ST87WMX6	SOX28 (300 mil)	External, user supplied
M41ST87WMX6TR		
M41ST87WSS6F	SSOP20	External, user supplied
M41ST87YMX6	SOX28 (300 mil)	External, user supplied
M41ST87YMX6TR		
M41ST95WMX6	SOX28 (300 mil)	External, user supplied
M41ST95WMX6TR		
M41T00AUDD1F	DFN16	External, user supplied
M41T00CAPPC1	CAPHAT DIP-24	Internal, BR1632
M41T00M6E	SO-8	External, user supplied
M41T00M6F		
M41T00SM6E	SO-8	External, user supplied
M41T00SM6F		
M41T11M6E	SO-8	External, user supplied
M41T11M6F		
M41T11MH6E	SOH28 (330 mil)	External, SNAPHAT
M41T11MH6F		
M41T56M6E	SO-8	External, user supplied
M41T56M6F		

Table 1. Battery status for serial RTCs (continued)

Part number	Package	Battery status
M41T81M6E	SO-8	External, user supplied
M41T81M6F		
M41T81SM6E	SO-8	External, user supplied
M41T81SM6F		
M41T81SMY6E	SOX18 (300 mil)	External, user supplied
M41T81SMY6F		
M41T82RM6E	SO-8	External, user supplied
M41T82RM6F		
M41T82SM6E		
M41T82SM6F		
M41T82ZM6E		
M41T82ZM6F		
M41T83RMY6E	SOX18 (300 mil)	External, user supplied
M41T83RMY6F		
M41T83RQA6F	QFN16	External, user supplied
M41T83SMY6E	SOX18 (300 mil)	External, user supplied
M41T83SMY6F		
M41T83SQA6F	QFN16	External, user supplied
M41T83ZMY6E	SOX18 (300 mil)	External, user supplied
M41T83ZMY6F		
M41T83ZQA6F	QFN16	External, user supplied
M41T93RMY6E	SOX18 (300 mil)	External, user supplied
M41T93RMY6F		
M41T93RQA6F	QFN16	External, user supplied
M41T93SMY6E	SOX18 (300 mil)	External, user supplied
M41T93SMY6F		
M41T93SQA6F	QFN16	External, user supplied
M41T93ZMY6E	SOX18 (300 mil)	External, user supplied
M41T93ZMY6F		
M41T93ZQA6F	QFN16	External, user supplied
M41T94MH6E	SOH28 (330 mil)	External, SNAPHAT
M41T94MH6F		
M41T94MQ6E	SO-16	External, user supplied
M41T94MQ6F		

Table 2. Battery status for TIMEKEEPER and ZEROPOWER NVRAMs

Part number	Package	Battery status
M40Z111MH6E	SOH28 (330 mil)	External, SNAPHAT
M40Z111MH6F		
M40Z111WMH6E		
M40Z111WMH6F		
M40Z300AVMQ6TR	SO-16	External, user supplied
M40Z300WMH6E	SOH28 (330 mil)	External, SNAPHAT
M40Z300WMH6F		
M40Z300WMQ6E	SO-16	External, user supplied
M40Z300WMQ6F		
M48T02-150PC1	CAPHAT DIP-24	Internal, BR1225
M48T02-70PC1		
M48T08-100PC1	CAPHAT DIP-28	Internal, BR1225
M48T08-150PC1		
M48T08Y-10MH1E	SOH28 (330 mil)	External, SNAPHAT
M48T08Y-10MH1F		
M48T12-150PC1	CAPHAT DIP-24	Internal, BR1225
M48T12-70PC1		
M48T128Y-70PM1	Hybrid DIP-32	Internal, BR1632
M48T129V-85PM1		
M48T129Y-70PM1		
M48T18-100PC1	CAPHAT DIP-28	Internal, BR1632
M48T18-150PC1		
M48T201V-85MH1E	SOH28 (330 mil)	External, SNAPHAT
M48T201V-85MH1F		
M48T201Y-70MH1E		
M48T201Y-70MH1F		
M48T35-70PC1	CAPHAT DIP-28	Internal, BR1632
M48T35Y-70PC1		
M48T35AV-10MH1E	SOH28 (330 mil)	External, SNAPHAT
M48T35AV-10MH1F		
M48T35AV-10PC1	CAPHAT DIP28	Internal, BR1632
M48T35Y-70MH1E	SOH28 (330 mil)	External, SNAPHAT
M48T35Y-70MH1F		

Table 2. Battery status for TIMEKEEPER and ZEROPOWER NVRAMs (continued)

Part number	Package	Battery status
M48T37V-10MH1E	SOH28 (330 mil)	External, SNAPHAT
M48T37V-10MH1F		
M48T37Y-70MH1E		
M48T37Y-70MH1F		
M48T512Y-70PM1	Hybrid DIP-32	Internal, BR1632
M48T58-70PC1	CAPHAP DIP-28	Internal, BR1225
M48T58Y-70PC1		
M48T58Y-70MH1E	SOH28 (330 mil)	External, SNAPHAT
M48T58Y-70MH1F		
M48Z02-150PC1	CAPHAP DIP-28	Internal, BR1225
M48Z02-70PC1		
M48Z08-100PC1	CAPHAP DIP-28	Internal, BR1632
M48Z12-150PC1	CAPHAP DIP-28	Internal, BR1225
M48Z12-70PC1		
M48Z128-70PM1	Hybrid DIP-32	Internal, BR1632
M48Z128Y-70PM1		
M48Z128Y-85PM1		
M48Z129V-85PM1		
M48Z18-100PC1	CAPHAP DIP-28	Internal, BR1632
M48Z2M1V-85PL1	Hybrid DIP-36	Internal, BR1632 (two)
M48Z2M1Y-70PL1		
M48Z35-70PC1	CAPHAP DIP-28	Internal, BR1225
M48Z35Y-70PC1		
M48Z35AV-10MH1E	SOH28 (330 mil)	External, SNAPHAT
M48Z35Y-70MH1E		
M48Z35Y-70MH1F		
M48Z512A-70PM1	Hybrid DIP-32	Internal, BR1632
M48Z512AV-85PM1		
M48Z512AY-70PM1		
M48Z512BV-85PM1		
M48Z58-70PC1	CAPHAP DIP-28	Internal, BR1225
M48Z58Y-70PC1		
M48Z58Y-70MH1E	SOH28 (330 mil)	External, SNAPHAT
M48Z58Y-70MH1F		

Revision history

Table 3. Document revision history

Date	Revision	Changes
Dec-1998	1	Initial release.
28-Dec-2007	2	Reformatted document; updated *UL 1950/60950 validation* and technical support URL.
02-Nov-2009	3	Updated *Introduction*; *Characterization and modeling*; *Figure 3*; reformatted document.
07-Mar-2012	4	Added *Battery status for NVRAMs and serial RTCs*, *Figure 4*, *5*, *6* *Table 1*, *2*; updated title of datasheet; minor textual updates.

AN1012
Application note

Predicting the battery life and data retention period of NVRAMs and serial RTCs

Introduction

Standard SRAM devices have the advantage, over EEPROM and Flash memory, of high write-speed when used as main memory for a processor or microcontroller. Their disadvantage is that they are volatile, and lose their contents as soon as the power supply is removed (whether this is for a prolonged period due to being turned off, or due to an unexpected glitch or loss of the power supply).

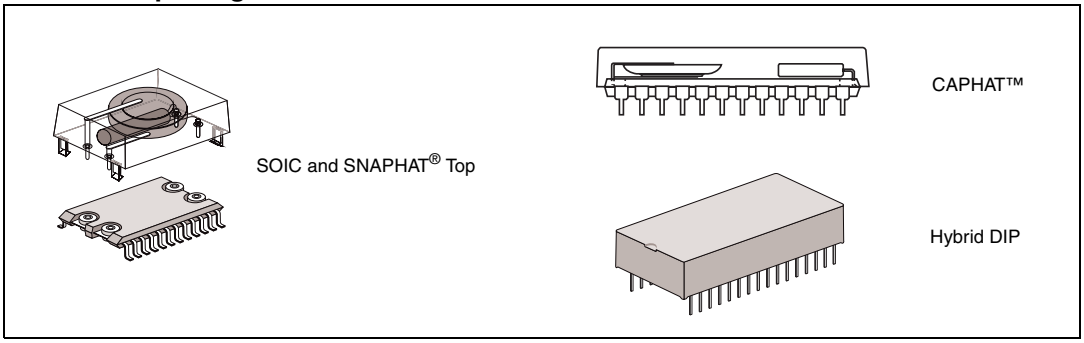
STMicroelectronics manufactures a line of non-volatile SRAMs (NVRAMs), known as ZEROPOWER® or TIMEKEEPER® NVRAMs, supervisors, and serial RTCs which offer the best of both worlds: memory devices that are non-volatile like EEPROM, yet have the fast access of SRAM. These devices consist of an array of low-power CMOS SRAM, plus a small long-life lithium power cell (along with a high-accuracy quartz crystal, in the case of the TIMEKEEPER). While the external power supply is within its specified limits, the memory behaves as standard SRAM; but as soon as the external power supply strays out of tolerance, the SRAM becomes write-protected, and its contents are preserved by a small trickle current supplied by the internal power cell.

Unlike EEPROM, where the data contents are guaranteed to be preserved for 10 years (and typically last for much longer), the contents of NVRAM will only be retained while the internal cell is able to supply sufficient current to maintain the array. This document summarizes the factors involved in predicting the battery life, and consequently data retention under various operating conditions.

Many of the ZEROPOWER, TIMEKEEPER, supervisor, and serial RTC devices are packaged in a 600 mil DIP CAPHAT™, a hybrid DIP, or a 330 mil SOIC SNAPHAT®. The SNAPHAT (shown in *Figure 1*) has a removable top that includes both the long-life lithium cell and, in the case of the TIMEKEEPER, a high-accuracy crystal.

STMicroelectronics has shipped several million SNAPHATs that have been used in a broad range of applications. From PC-based systems to high-end workstations, telecommunications, consumer, and automotive applications, these products have provided highly reliable data storage for the electronics industry.

Figure 1. Standard ZEROPOWER, TIMEKEEPER, supervisor, and serial RTC packages



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1 Process technology

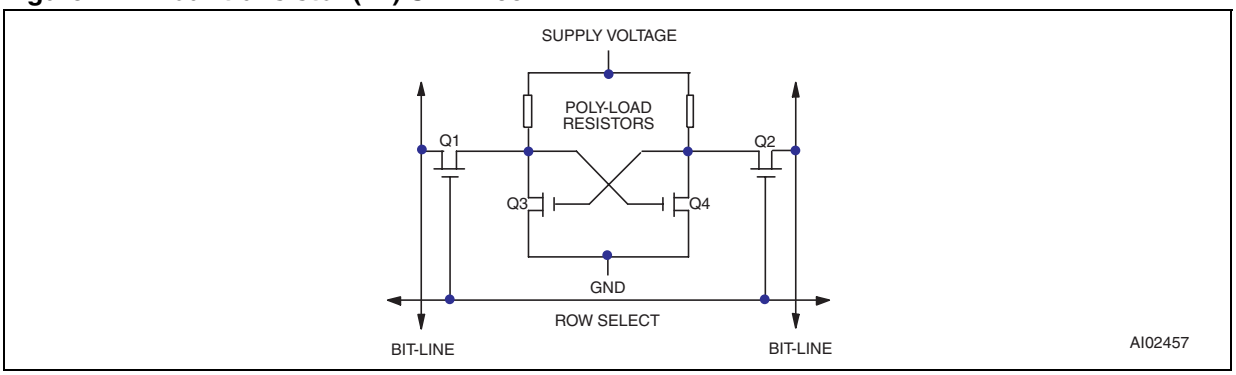
The ZEROPOWER®, TIMEKEEPER®, supervisor, and serial RTC families consist of a broad range of products that encompass various technologies. These products can be divided into six categories, as shown in *Table 1*. The SRAM array is generally based on a 6-transistor or 4-transistor cell, as indicated by the categories (6T and 4T). *Figure 2* illustrates a one-bit storage cell from a 4-transistor SRAM cell.

The hybrid devices (also known as module devices) contain individually packaged analog circuitry and SRAM. They are not covered in this document, except for the table of values for typical battery lifetimes in *Appendix A: Product data on page 25*.

Table 1. ZEROPOWER and TIMEKEEPER® product categories

Category	Devices
ZEROPOWER (4T cell)	M48Z02, M48Z12, M48Z08, M48Z18, M48Z58/Y, M48Z35/Y/AV
ZEROPOWER Hybrid	M48Z128/Y, M48Z129V, M48Z512A/AY, M48Z2M1V/Y
TIMEKEEPER (4T cell)	M48T08/Y, M48T58/Y, M48T35/Y/AV, M48T37V/Y
TIMEKEEPER Hybrid	M48T128Y, M48T129V, M48T512Y
Supervisors	M40Z111/W, M40Z300W, M48T201V/Y
Serial RTCs (6T cell)	M41T00/S, M41T11, M41T56, M41T81/S, M41T94, M41ST85W, M41ST87W

Figure 2. Four-transistor (4T) SRAM cell



The first devices, released in 1982, were based on a conventional 6T, full-CMOS, SRAM design. These were specified for low-voltage data retention, and were built to stringent manufacturing and test specifications. With data retention currents of less than 150 nA at 70 °C, these devices were designed to retain data in battery backup for at least 10 years over the full commercial temperature range.

Newer devices have since been released. They use 4T, CMOS SRAM arrays. By using two poly-R resistors in place of the pull-up transistors of full-CMOS design, the 4T cell is much smaller than the 6T equivalent. Die size is dramatically reduced because the poly-R resistors can be stacked on top of n-channel pull-down MOSFETs in the cell. This leads to a net reduction in the device costs. Although the current drawn from the lithium cell is increased, the devices have been specified to outlast the useful life of most equipment in which they are used.

2 Battery technology

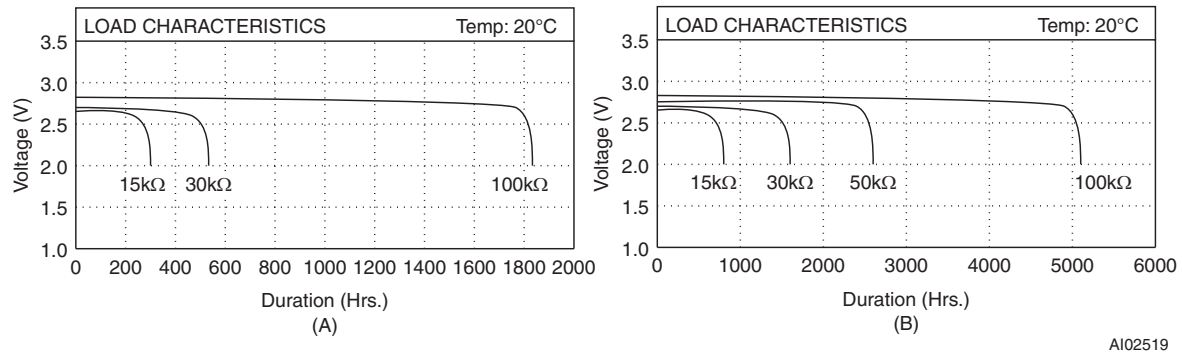
STMicroelectronics uses both the BR1225 and the BR1632 lithium button cell batteries. These have charge capacities of 48 mAh and 120 mAh, respectively. Their constituents have non-toxic and non-corrosive characteristics, and are chemically and thermally stable before, during, and after discharge. This makes these cells particularly attractive for use in electrical components.

They contain a solid carbon cathode that is pressed into a tablet of predetermined weight and height. The anode consists of high-purity lithium metal. The electrolyte is based on an organic solvent instead of the corrosive alkaline or acidic solution found in most conventional batteries. This greatly reduces the likelihood of internally-induced cell leakage, and reduces the ill effects in cases of externally-induced cell leakage. The cell is then crimp-sealed with a polypropylene grommet.

ST has conducted extensive tests on these cells, at temperatures up to 85 °C. Destructive analysis was conducted (post-stress), in order to measure such factors as weight loss and remaining charge capacity. The analysis determined that the cells were drying out, and that the weight loss was due to electrolyte evaporation. Models were developed to predict the nominal rate of electrolyte loss, and how this would be reduced by adding a second level of encapsulation. This proprietary secondary seal encapsulation, adopted by ST, has been found to provide up to a two-fold reduction of the electrolyte loss rate.

Both cells produce a nominal 2.9 V output with a flat discharge curve until the end of their effective lives, and thus confirms that both are suitable for providing battery backup to low leakage CMOS SRAMs (see *Figure 3*).

Figure 3. (A) BR1225 discharge rate and (B) BR1632 discharge rate



3 Battery backup current - predicting data retention time

A ZEROPOWER®, TIMEKEEPER®, supervisor, or serial RTC device will reach the end of its useful life for one of two reasons:

- **Capacity consumption**
  It becomes discharged, having provided current to the SRAM (and to the oscillator in the case of the TIMEKEEPER) in the battery backup mode.
- **Storage life**
  The effects of aging will have rendered the cell inoperative before the stored charge has been fully consumed by the application.

The two effects have very little influence on each other, allowing them to be treated as two independent but simultaneous mechanisms. The data retention lifetime of the device is determined by which ever failure mechanism occurs first.

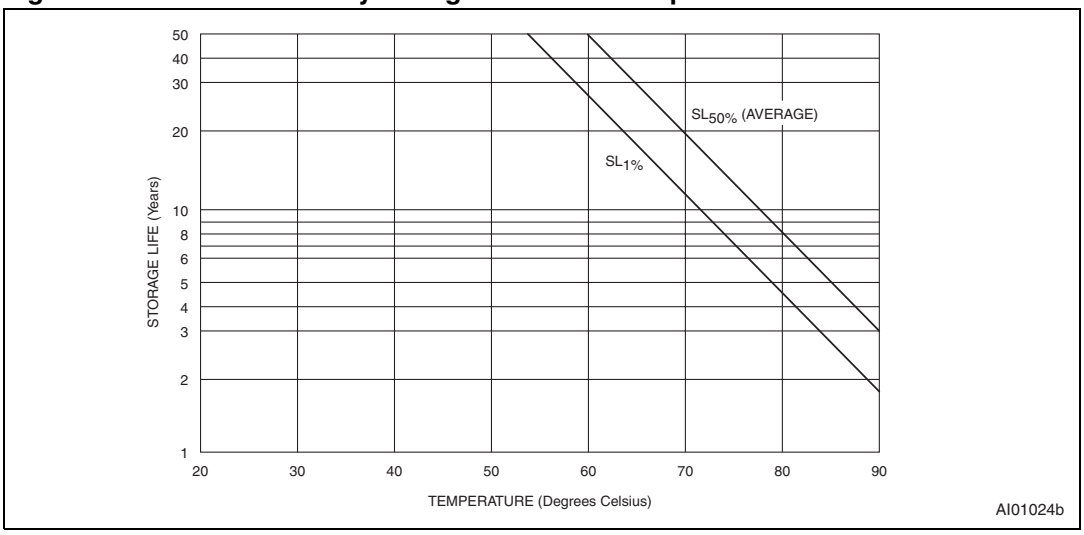
3.1 Storage life

Storage life, resulting from electrolyte evaporation, is primarily a function of temperature. *Figure 4* illustrates the predicted storage life of the BR1225 battery versus temperature. The results are derived from temperature-accelerated life test studies performed at STMicroelectronics. For the purpose of testing, a cell failure is defined as the inability of a cell, stabilized at 25 °C, to produce a 2.4 V closed-circuit voltage across a 250 kΩ load resistor.

The two lines, $SL_{1\%}$ and $SL_{50\%}$, represent different failure rate distributions for the cell's storage life. At 60 °C, for example, the $SL_{1\%}$ line indicates that the battery has a 1% chance of failure 28 years into its life, and the $SL_{50\%}$ line shows that the battery has a 50% chance of failure at the 50 year mark. The $SL_{1\%}$ line represents the practical onset of wear out, and can be considered the worst case storage life for the cell. The $SL_{50\%}$ line can be considered to be the normal, or average, life. As indicated by the curves in *Figure 4 on page 9*, storage life does not become a limiting factor to overall battery life until temperatures in excess of 60 °C to 70 °C are involved.

As an approximation, $SL_{50\%} = 14270 \times (0.91)^T$, and $SL_{1\%} = 8107 \times (0.91)^T$, when $20\ °C < T < 90\ °C$.

Figure 4. Predicted battery storage life versus temperature



3.2 Calculating storage life

Only the user can estimate predicted storage life in a given design because the ambient temperature profile is dependent upon application-controlled variables. As long as the ambient temperature is held reasonably constant, the expected storage life can be read directly from *Figure 4 on page 9*. If the battery spends an appreciable amount of time at a variety of temperatures, the following formula can be used to estimate predicted storage life:

$$\left[\left(\frac{t_1}{T}\times\frac{1}{SL_1}\right)+\left(\frac{t_2}{T}\times\frac{1}{SL_2}\right)+\ldots+\left(\frac{t_n}{T}\times\frac{1}{SL_n}\right)\right]^{-1}$$

where,

- t_i /T is the relative proportion (of the total time) during which the device is at ambient temperature TA_i;
- SL_i is the storage life at ambient temperature TA_i as illustrated in *Figure 4*; and
- T is the total time = $t_1 + t_2 + ... + t_n$.

For example, consider a battery exposed to temperatures of up to 90 °C for 600 hrs/yr, and temperatures of 60 °C or less for the remaining 8160 hrs/yr. Reading predicted $t_{1\%}$ values from *Figure 4*,

- SL_1 is about 1.8 yrs;
- SL_2 is about 28 yrs;
- T is 8760 hrs/yr;
- t_1 is 600 hrs/yr; and
- t_2 is 8160 hrs/yr.

The predicted storage life evaluates to:

$$\left[\left(\frac{600}{8760}\times\frac{1}{1.8}\right)+\left(\frac{8160}{8760}\times\frac{1}{28}\right)\right]^{-1}$$

This predicts that the storage life, in this particular case, is at least 14 years. This is, therefore, better than the normally accepted life time of 10 years.

3.3 Capacity consumption

When V_{CC} is being held by the external power supply within its specified range, the current drawn from the battery is zero. When V_{CC} falls below the battery backup switchover voltage (V_{SO}), the device goes into battery backup mode and draws all of its current from the battery.

The V_{CC} duty cycle represents the proportion of time, expressed as a percentage, that the device is supplied with power from the external supply, and therefore not drawing current from the battery.

In its battery backup mode, the array of SRAM cells can be characterized by its data retention (I_{CCDR}) current, caused primarily by the current through the Poly-R load resistors in the 4T technology, as well as also by junction leakage, sub-threshold current, and gate-to-substrate leakage. The total current is referred to as I_{BAT} (the current drawn during battery backup mode). For ZEROPOWER® devices, this is the sum of leakage currents plus the current necessary to maintain the SRAM array. For TIMEKEEPER® devices, it is the sum of the array current (including leakage) and the clock current:

$$I_{BAT} = I_{ARRAY} + I_{CLOCK}$$

Many factors need to be taken into account when calculating the I_{BAT} current, including process parameters, working temperature, and the V_{CC} duty cycle.

3.4 Calculating capacity consumption

Capacity consumption is simply calculated by:

$$\frac{\text{BatteryCapacity}}{8760 \times (1 - V_{CC}\text{DutyCycle}/100) \times I_{BAT}}$$

where:

- Battery capacity is measured in ampere-hours;
- 8760 is the constant for the number of hours there are in a year;
- V_{CC} duty cycle is measured as a percentage; and
- I_{BAT} is measured in amperes.

For the M48T35Y, a 32K x 8 TIMEKEEPER® device with a 0.048 Ah (48 mAh) M4T28-BR12SH1 battery, the typical battery current is approximately 2666 nA at 70 °C.

So, if the V_{CC} duty cycle is 50%, the predicted capacity life is:

$$\frac{0.048}{8760 \times 0.5 \times 2666 \times 10^{-9}}$$

and therefore is about 4.11 years at 70 °C.

4 4T cell devices

In moving to the newer process technologies (e.g., M48Z58 (8K x 8) device), STMicroelectronics has chosen to reduce the active current as well as decrease the die size. The STMicroelectronics HCMOS4PZ process is a 0.6 µm, double-level metal process.

In the standard SRAM memory cell, 6 transistors are formed into a pair of cross-coupled inverters. In the 4T memory cell, the top two p-channel devices are replaced by poly-silicon load resistors (poly-R). This combination allows for significant die size reduction because the poly-R structures can be stacked on top of the active n-channel devices.

There is always at least one direct path constantly leaking current to ground in each cell because of the poly-R structures in each SRAM cell. However, the value of the resistor is extremely high (about 3TΩ at 25 °C), so at a cell voltage of 3 V, this leads to a leakage current of 1 pA. Multiplying by the number of cells within the array, the array standby current can be calculated (i.e. 65.5 nA for a 65536-cell array).

The poly-R structure values are dependent on temperature, so the entire array current is very strongly temperature-dependent. *Appendix B: ZEROPOWER products on page 26* shows the expected battery lifetime of an M48Z58 device versus working temperature with a V_{CC} duty cycle of 0%.

The original specification was an expected lifetime of greater than 10 years at 25 °C but, in fact, this target is typically achieved even at 70 °C. By reducing the temperature, the expected lifetime rises to greater than 20 years (i.e., when the device is operated at 50 °C). This change is defined entirely by the temperature sensitivity of the poly-R structures within each SRAM cell.

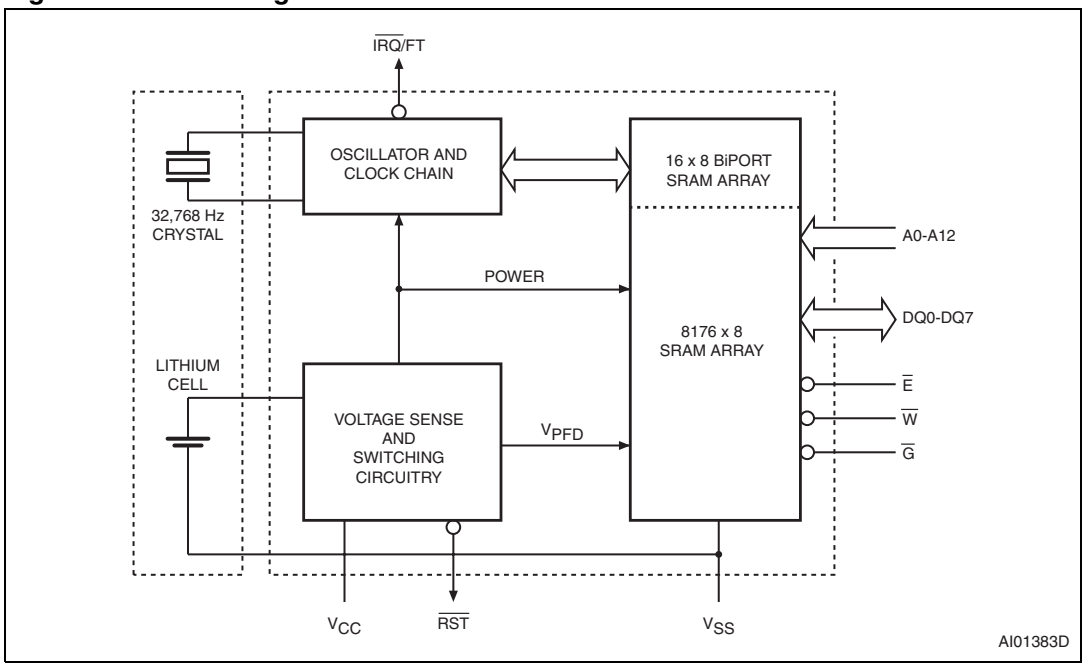
The M48Z35 also employs the STMicroelectronics HCMOS4PZ process, 4T SRAM cell technology. *Appendix B* shows the expected battery lifetime of an M48Z35 device versus working temperature with a V_{CC} duty cycle of 0%. From this we can see that expected lifetime is typically greater than 20 years when operated at 30 °C with no external V_{CC} applied, and falls to approximately 2.6 years for continuous battery backup at 70 °C. This is to be expected, due to the increased current consumption inherent in the 4T SRAM cell architecture. It should be noted that this data is based on usage of the SNAPHAT® product which includes a 48 mAh battery.

5 TIMEKEEPER products

TIMEKEEPER® products are very similar in construction and operation to ZEROPOWER® products. However, they must be evaluated separately. The current drawn is highly dependent not only on the temperature, but also on whether the oscillator is active. The main components of TIMEKEEPER devices are (see *Figure 5*):

- a CMOS RAM array;
- voltage sense and switching circuitry;
- an analog oscillator and clock chain;
- a lithium power cell; and
- a high-accuracy quartz crystal.

Figure 5. Block diagram of a TIMEKEEPER® device



5.1 TIMEKEEPER® register map

Table 2 shows a typical register map for the seconds, minutes, hours, date, day, month, and year fields. This information is stored in Binary Coded Decimal (BCD) format. These basic functions are available on all TIMEKEEPER devices. Additional features (e.g., watchdog timer, alarms, battery low flag, and a wake-up function) have additional registers allocated to them (such as those shown for the M48T37V/Y in *Table 2*). The TIMEKEEPER register locations are constructed from BiPORT™ memory cells which allow data access from two sides. The on-chip system clock connects to one side (the system side) and the user data is output to connections on the other (the user's side). At one-second intervals, clock pulses are generated by the oscillator and clock chain structure. The system side updates the new time in the TIMEKEEPER registers. Each TIMEKEEPER register location (e.g. minutes, hours, day) is then updated as necessary. When the user wants to write a new time, the "W" bit (the Write bit) of the control register is reset, causing the BiPORT cells to upload the new system time. The user accesses the TIMEKEEPER and array data by executing standard READ/WRITE cycles.

The oscillator and clock chain structure consists of a mixture of analog and digital circuitry, and account for the majority of the I_{BAT} current. *Table 3* gives conservative estimates of the currents drawn as a function of technology and working temperature.

Table 2. Typical TIMEKEEPER (M48T37V/Y) register map

Address	Data								Function	Range (in BCD format)
	D7	D6	D5	D4	D3	D2	D1	D0		
7FFFh	10 Years				Year				Year	00-99
7FFEh	0	0	0	10M	Month				Month	01-12
7FFDh	0	0	10 Date		Date				Date	01-31
7FFCh	0	FT	0	0	0	Day			Day	01-7
7FFBh	0	0	10 Hours		Hours				Hours	00-23
7FFAh	0	10 Minutes			10 Minutes				Minute	00-59
7FF9h	ST	10 Seconds			Seconds				Second	00-59
7FF8h	W	R	S	Calibration					Control	
7FF7h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watch	
7FF6h	AFE	0	ABE	0	0	0	0	0	Interrupt	
7FF5h	RPT4	0	AI 10 Date		Alarm Date				A Date	01-31
7FF4h	RPT3	0	AI 10 Hour		Alarm Hour				A Hour	00-23
7FF3h	RPT2	Alarm 10 Minutes			Alarm Minutes				A Minute	00-59
7FF2h	RPT1	Alarm 10 Seconds			Alarm Seconds				A Second	00-59
7FF1h	1000 Years				100 Years				Century	00-99
7FF0h	WDF	AF	0	BL	Z	Z	Z	Z	Flags	

Table 3. Typical I_{BAT} current for TIMEKEEPER devices

		Typical at 20°C		Typical at 70°C	
Capacity	Technology	Array	Clock	Array	Clock
64 Kbit	4T Cell	40 nA	497 nA	511 nA	619 nA

5.2 TIMEKEEPER® evolution

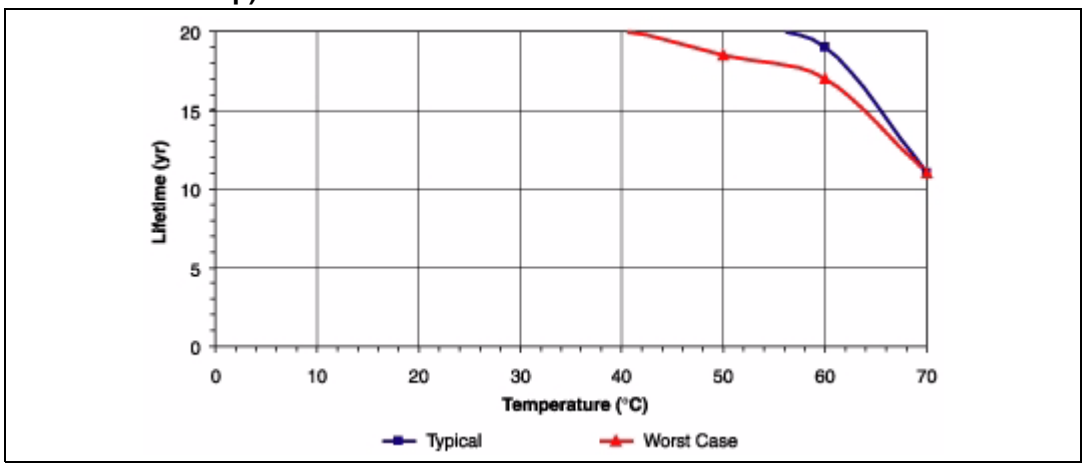
TIMEKEEPER products have seen a continuous evolutionary cycle since their initial market introduction in the 1990s.

5.2.1 M48T02 and M48T12

The first TIMEKEEPER products released were the MK48T02 and MK48T12 which offered 2K x 8 RAM and employed the STMicroelectronics 2.0 µm Spectrum™ CMOS technology. When released, these products included a BR1225 lithium cell with a specified 39 mAh capacity. This combination offered the user approximately 3.5 years of continuous battery backup life. Since that time, the devices have been moved to the 4T cell technology (HCMOS4PZ) and a CAPHAT™ package revision which includes a larger capacity lithium cell (120 mAh BR1632) capacity, and new part numbers (M48T02/12). These changes increased the expected battery life to 19 years at 60°C.

Figure 6 shows expected battery lifetime versus temperature with 100% battery backup. The data shows that by operating the devices at various temperatures, designers can expect a battery life approaching 20 years under most conditions.

Figure 6. M48T02/12 data retention lifetime vs. temperature (120 mAh, 100% battery backup)

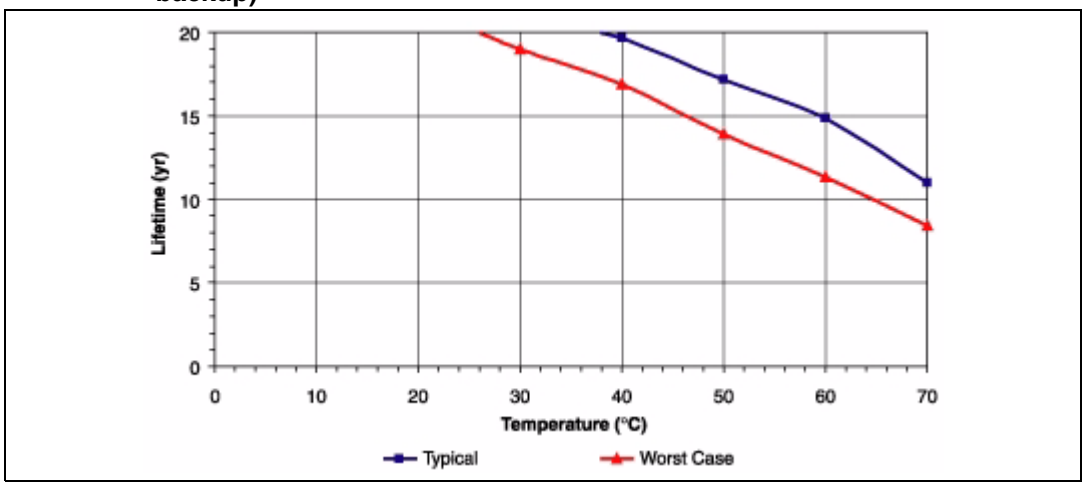


5.2.2 M48T08 and M48T18

The next TIMEKEEPER® to be released was the MK48T08/18 family, which has an 8K x 8 SRAM array. By using the more advanced 1.2 µm HCMOS3 process and refining the on-board oscillator, STMicroelectronics was able to offer a nearly three-fold increase in battery lifetime, even though the array size had increased by a factor of four. This product was later converted to the 0.6 µm, double-level metal HCMOS4PZ process for 4T SRAM cells. The battery was then upgraded to 120 mAh for the CAPHAT™ package revision (part numbers M48T08/18), which provides a battery life of at least 10 years across the commercial temperature range (0 °C to 70 °C, see *Figure 7*).

In the M48T08/18 datasheet, the battery lifetime (t_{DR}, data retention time) has been specified as 10 years or greater across the commercial temperature range (for a 0% V_{CC} duty cycle).

Figure 7. M48T08/18 data retention lifetime vs. temperature (120 mAh, 100% battery backup)



5.2.3 M48T58

The next TIMEKEEPER® product was the M48T58 which is fabricated on the 0.6 µm, double-level metal HCMOS4PZ process for 4T SRAM cells.

Table 13 on page 28, *Appendix C: TIMEKEEPER® products on page 28*, *Figure 8*, and *Figure 9 on page 16* show the extent to which the data retention of these devices is more dependent on temperature. Higher temperatures cause lower resistor values (and therefore, higher currents) because of the negative temperature coefficient of the poly-R resistors.

Data retention lifetimes typically range from 8.6 years (at 30 °C) for devices in the CAPHAT™ package, with a 48 mAh battery (see *Figure 8*), and up to 20 years (and more) for the SNAPHAT package with a 120 mAh BR1632 battery (see *Figure 9*). As always, several factors affect battery lifetime, including the V_{CC} duty cycle and temperature.

Figure 8. M48T58 data retention lifetime vs. temperature (48 mAh, 100% battery backup)

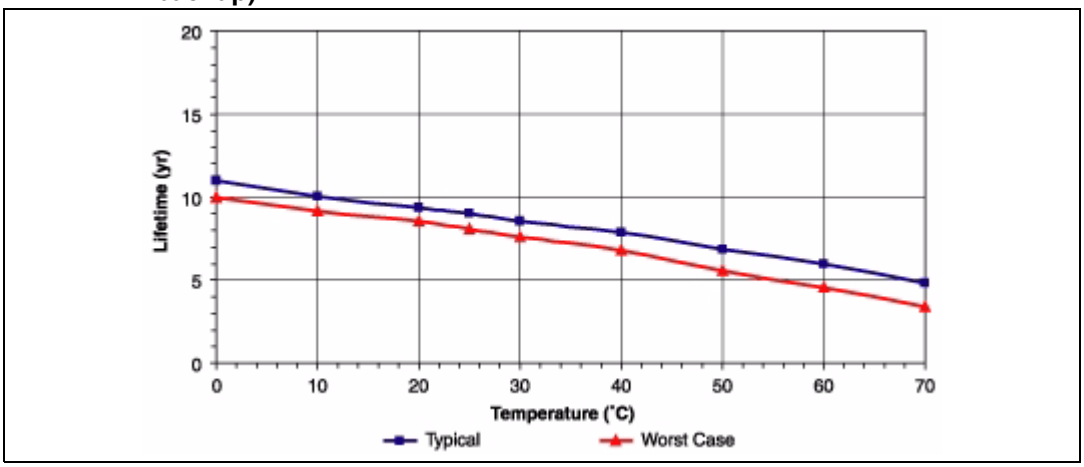
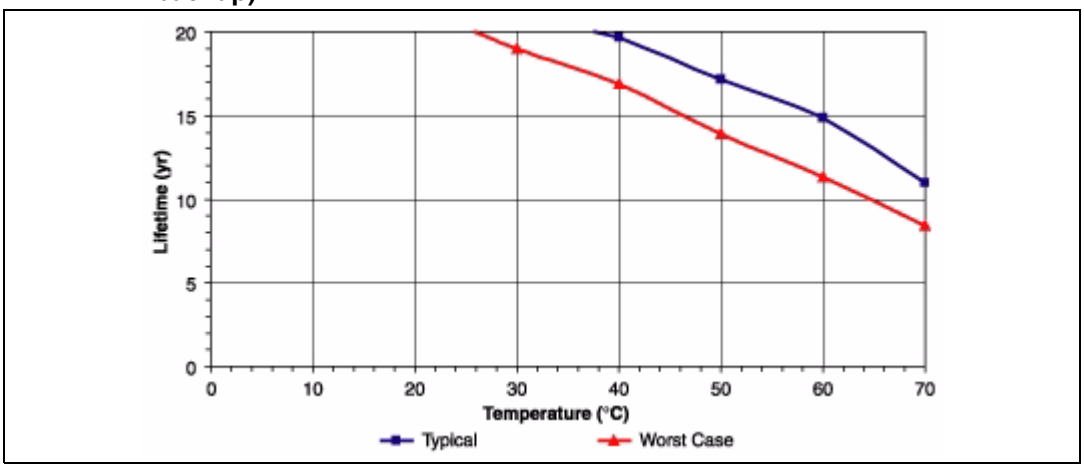


Figure 9. M48T58 data retention lifetime vs. temperature (120 mAh, 100% battery backup)



5.2.4 M48T35 and M48T37V/Y

The M48T35 and M48T37V/Y families use the same technology as the M48T58 device, but with a 32K x 8 SRAM array. *Figure 10* and *Figure 11* show the expected battery lifetime versus temperature. The expected battery lifetime (at 30 °C with no periods of valid V_{CC}) is typically 6.8 years (this assumes that a 48 mAh battery is used, see *Figure 10*). Devices in the larger M4T32-BR12SH SNAPHAT® package have a data retention lifetime of greater than twice this (almost 17 years, see *Figure 11*).

Figure 10. M48T35/37V/37Y data retention lifetime vs. temperature (48 mAh, 100% battery backup)

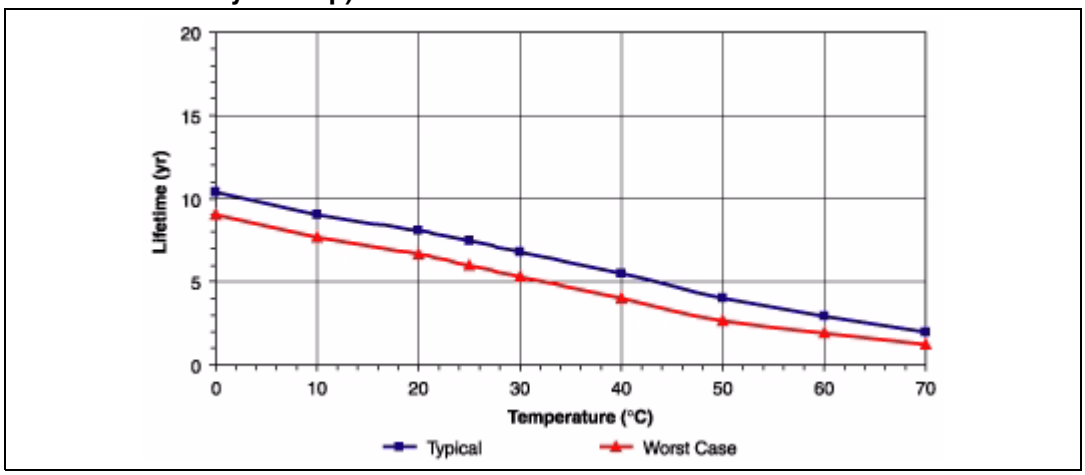
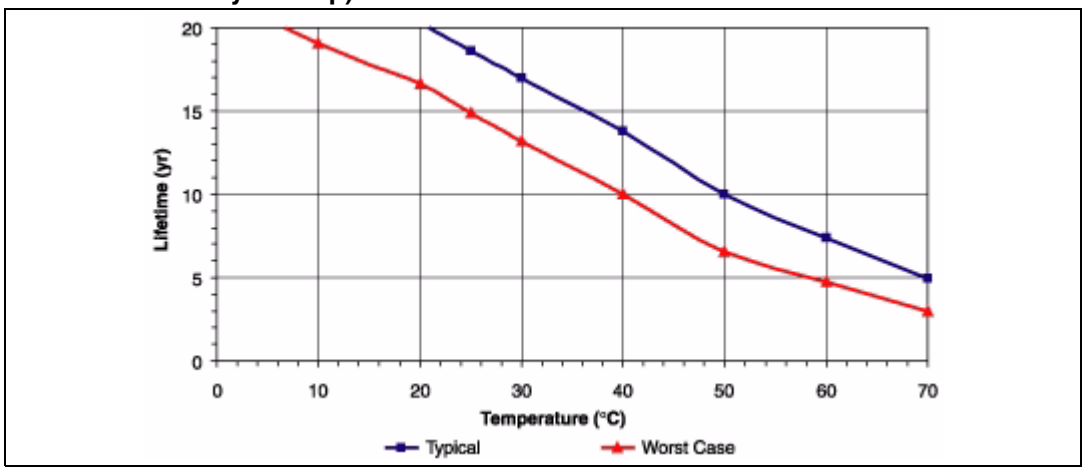


Figure 11. M48T35/37V/37Y data retention lifetime vs. temperature (120 mAh, 100% battery backup)



If data retention lifetimes greater than those shown are required, the user is advised to choose the version of the device in a SNAPHAT® package. Then, as the battery starts to reach the end of its useful life, it is possible to remove the SNAPHAT top containing the nearly expended cell and replace it with a fresh SNAPHAT top. No data will be lost during the process, provided that the board remains powered up during the operation (although some time will be lost due to the momentary removal of the 32 kHz crystal). *Table 4* shows which SNAPHAT top part numbers are available.

Table 4. SNAPHAT part numbers

Part Number	Description	Package
M4Z28-BR00SH	Li Battery (48mAh) for ZEROPOWER products and SUPERVISORS	SNAPHAT
M4Z32-BR00SH	Li Battery (120mAh) for ZEROPOWER products and SUPERVISORS	SNAPHAT
M4T28-BR12SH	Li Battery (48mAh) for TIMEKEEPER products and SUPERVISORS	SNAPHAT
M4T32-BR12SH	Li Battery (120mAh) for TIMEKEEPER products and SUPERVISORS	SNAPHAT

6 Supervisor products

STMicroelectronics also has a family of ZEROPOWER® and TIMEKEEPER® supervisor devices. Supervisors are self-contained units that allow standard low-power SRAMs to be turned into non-volatile memory devices. They monitor and provide V_{CC} input for one or more external SRAMs the same way ZEROPOWER and TIMEKEEPER products do. They use a precision voltage reference and comparator to monitor the V_{CC} input for going out-of-tolerance.

When V_{CC} becomes invalid, the supervisor's conditioned chip-enable outputs ($\overline{E}_{CON}$) are forced to their "inactive" state, thereby putting each external SRAM into its own write-protect state. During the power failure, the supervisor provides the power for the SRAM from the lithium cell within its SNAPHAT top. The supervisor switches the power source back to the V_{CC} supply as soon as the voltage returns to specified levels.

7 Choosing SRAM

Most low power SRAMs on the market today can be used with both ZEROPOWER® and TIMEKEEPER® supervisors, although there are some issues that need addressing before finally choosing which SRAM to use.

- The chip enable input, when taken inactive, must disable all the other inputs to the SRAM. This allows inputs to the external SRAMs to be treated as “Don’t care” once V_{CC} falls below V_{PFD}(min).
- The SRAM should guarantee data retention when working at V_{CC} = 2.0 volts.
- The chip-enable access time must be sufficient to meet the system needs, taking into account propagation delays on chip enable and output enable.

Most SRAMs specify a data retention current (I_{CCDR}) at 3.0 V. Manufacturers generally specify a typical condition for room temperature along with a worst case condition (generally at elevated temperatures). The system level requirements will determine the choice of which value to use. The data retention current value of the SRAMs can then be added to the I_{BAT} value of the supervisor to determine the total current requirements for data retention. The available battery capacity for the SNAPHAT® of your choice can then be divided by this current to determine the data retention period (see *Section 3.3: Capacity consumption on page 10*).

For example, the M48T201V/Y has an I_{BAT} value of 575 nA at 25 °C, and 800 nA at 70 °C. The M40Z300W has an I_{BAT} value of 5 nA at 25 °C, and 100 nA at 70 °C. *Table 5* indicates typical data retention lifetimes for the M40Z300W ZEROPOWER supervisor when it is used with a number of commercially available 1 Mbit and 4 Mbit SRAMs. *Table 6 on page 21* shows the same kind of information for the M48T201V/Y TIMEKEEPER supervisors.

Table 5. M40Z300W (120mAh SNAPHAT) data retention life vs. SRAM type

Size (Mbit)	Product		I_{BAT} (SRAM) (nA)		I_{BAT} (Total) (nA)		Lifetime in years(1)	
			25°C	70°C	25°C	70°C	25°C	70°C
1	Hynix	HY628100BLLT1-55	1000	10000	1005	10100	13.6	1.4
		HY62V8100BLLT1-70(2)	1000	10000	1005	10100	13.6	1.4
	Renesas	M5M51008DVP-55H	500	10000	505	10100	> 20	1.4
		M5M5V108DVP-70H(2)	1000	10000	1005	10100	13.6	1.4
4	Renesas	R1LP0408CSB-5SC	800	8000	805	8100	17.0	1.7
		R1LV0408CSB-5SC(2)	500	8000	805	8100	> 20	1.7
8	Renesas	HM62V8100LTTI-5SL	500	10000	505	10100	> 20	1.4
	Samsung	K6X8008T2B-UF5500	N/A	15000	N/A	15100	N/A	0.9

1. According to the respective manufacturer’s datasheets at the time of writing.
2. 3 V device

Table 6. M48T201V/Y (120 mAh SNAPHAT) data retention life vs. SRAM type

Size (Mbit)	Product		I_{BAT} (SRAM) (nA)		I_{BAT} (Total) (nA)		Lifetime in years[1]	
			25°C	70°C	25°C	70°C	25°C	70°C
1	Hynix	HY628100BLLT1-55	1000	10000	1075	10800	8.7	1.3
		HY62V8100BLLT1-70[2]	1000	10000	1075	10800	8.7	1.3
	Renesas	M5M51008DVP-55H	500	10000	1075	10800	12.7	1.3
		M5M5V108DVP-70H[2]	1000	10000	1575	10800	8.7	1.3
4	Renesas	R1LP0408CSB-5SC	800	8000	1375	8800	10.0	1.6
		R1LV0408CSB-5SC[2]	500	8000	1075	8800	12.7	1.6
8	Renesas	HM62V8100LTTI-5SL	500	10000	1075	10800	12.7	1.3
	Samsung	K6X8008T2B-UF5500	N/A	15000	N/A	15800	N/A	0.9

1. According to the respective manufacturer's datasheets at the time of writing.
2. 3 V device

8 Industrial temperature devices

Due to ever increasing requirements for portability and operation under extreme environmental conditions, STMicroelectronics offers industrial temperature versions (–40°C to +85°C) of our serial RTC devices. This expanded operating range allows these products to perform under more extreme temperatures for applications such as:

- cell phone base stations;
- traffic control;
- portable equipment;
- land, water, and aircraft instrumentation; and
- industrial control equipment.

These products are indicated by the digit ‘6’ at the end of the sales-type. The industrial temperature TIMEKEEPER® SNAPHAT® top is also designated by the suffix “6.” Predicted data retention lifetimes are listed in *Appendix B: ZEROPOWER products on page 26* and *Appendix C: TIMEKEEPER® products on page 28*.

9 U.L. recognition and recycling

While providing innovative, leading edge products, STMicroelectronics remains committed to safety, including its products, its customers, and the environment. Each device contains reverse-charge protection circuitry, and uses safe lithium mono-fluoride batteries. All ZEROPOWER®, TIMEKEEPER, supervisor, and serial RTC components are recognized by Underwriter's Laboratory under file number E89556, and are compliant to the LL-94-VO flammability rating.

The unique SNAPHAT packaging consists of a 330 mil SOIC device and a separate, "snap-on" SNAPHAT, which includes both the lithium power cell, and in the case of TIMEKEEPER product, a high accuracy crystal. The SNAPHAT is removable and can be replaced, providing the added benefit of proper disposal or recycling that has not been available before with NVRAMs. Various companies offer recycling and safe disposal of scrap lithium cells.

10 Summary

Battery life and data retention for ZEROPOWER® and TIMEKEEPER® products are primarily functions of two factors:

- Capacity consumption, and
- Storage life of the lithium button cell battery.

Due to the fact that storage life (caused by electrolyte evaporation) has little effect at temperatures below 60 °C, the data retention of most applications will be dependent upon the I_{CCDR} of the SRAM being backed-up, as well as the V_{CC} duty cycle. This allows a fairly simple calculation (see *Section 3.4: Calculating capacity consumption on page 10*) to be used to determine the lifetime.

All ST ZEROPOWER products are able to offer at least a 10 year data retention life, typically at 40 °C. This may be increased by reducing the temperature, increasing the V_{CC} duty cycle, or in the case of the surface mount SNAPHAT® products, using the larger 120 mAh SNAPHAT top.

For the TIMEKEEPER family, battery lifetimes are also affected by the percentage of time the oscillator is in operation. Commercial devices fabricated in 4T technologies provide 7 years of continuous operation at 20 °C using the 48 mAh M4T28-BR12SH SNAPHAT top, and typically greater than 15 years with the 120 mAh M4T32-BR12SH SNAPHAT top.

The ZEROPOWER and TIMEKEEPER supervisor families allow the user to purchase commodity SRAMs at the best available market price. However, overall data retention life will be determined by the I_{CCDR} of the SRAM selected.

Appendix A Product data

Note: The symbol ">>" means, "... much greater than..."

Table 7. Data for ZEROPOWER® and TIMEKEEPER® devices

Device	Process technology	SRAM Cell	Battery type		I_{BAT} (T = 20°C) (nA)	Typical data retention lifetime(1) (years)
			SNAPHAT(2)	CAPHAT		
M48Z02/12	0.6 µm, HCMOS4PZ	4T	n/a	BR1225	9	10
M48Z08/18	0.6 µm, HCMOS4PZ	4T	BR1225	BR1225	37	10
M48Z35/Y/AV	0.6 µm, HCMOS4PZ	4T	BR1225	BR1225	148	10
M48Z58/Y	0.6 µm, HCMOS4PZ	4T	BR1225	BR1225	37	10
M48T02/12	0.6 µm, HCMOS4PZ	4T	N/A	BR1632	506	10
M48T08/18	0.6 µm, HCMOS4PZ	4T	BR1225	BR1632	535	10
M48T35/Y/AV	0.6 µm, HCMOS4PZ	4T	BR1225	BR1632	646	7/10
M48T37Y	0.6 µm, HCMOS4PZ	4T	BR1225	N/A	646	7
M48T58/Y	0.6 µm, HCMOS4PZ	4T	BR1225	BR1225	535	7

1. The data retention lifetime can be significantly increased by using the SNAPHAT (ZEROPOWER or TIMEKEEPER, as appropriate) with the higher capacity BR1632 battery.
2. The larger capacity BR1632 (120 mAh) battery is also available in the SNAPHAT package.

Table 8. Data from hybrid/module devices (V_{CC} duty cycle = 0%)

Device	Specification at T = 25°C (years)	Experimental conditions (years)		
		0°C	25°C	70°C
M48Z128/Y	10	>> 20	> 20	2.3
M48Z129V	10	>> 20	> 20	2.3
M48Z512A/AV/AY	10	>> 20	> 20	6.0
M48Z2M1V/Y	10	> 20	> 20	3.1
M48T128Y	10	> 20	16.6	2.0
M48T129V/Y	10	> 20	16.6	2.0
M48T512Y	10	> 20	19.4	4.8

Note: These devices are not recommended for new design. Please contact local ST sales office for availability.

Appendix B ZEROPOWER products

The tables in this appendix use the terms “typical” and “worst case” to indicate the “mean value at the given temperature” and “mean value plus maximum expected deviation at the given temperature.”

Note: The symbol “>>” means, “... much greater than...”

Table 9. Data from M48Z02/12 devices (available only in CAPHAT™ - BR1225, 48 mAh)

Temperature (°C)	V_{CC} duty cycle = 0%		V_{CC} duty cycle = 100%, shelf life (years)
	Typical (years)	Worst case (years)	
0	>> 20	>> 20	>> 20
10	>> 20	>> 20	>> 20
20	>> 20	>> 20	>> 20
25	>> 20	>> 20	>> 20
30	>> 20	>> 20	>> 20
40	>> 20	>> 20	>> 20
50	>> 20	>> 20	>> 20
60	> 20	> 20	> 20
70	11.0	11.0	11.0

Table 10. Data from M48Z08/18, M48Z58, and M48Z58Y devices

Temperature (°C)	CAPHAT or SNAPHAT (BR1225, 48 mAh)		SNAPHAT (BR1632, 120 mAh)		V_{CC} duty cycle = 100%, shelf life (years)
	V_{CC} duty cycle = 0%				
	Typical (years)	Worst case (years)	Typical (years)	Worst case (years)	
0	>> 20	>> 20	>> 20	>> 20	>> 20
10	>> 20	>> 20	>> 20	>> 20	>> 20
20	>> 20	>> 20	>> 20	>> 20	>> 20
25	>> 20	>> 20	>> 20	>> 20	>> 20
30	>> 20	>> 20	>> 20	>> 20	>> 20
40	>> 20	> 20	>> 20	>> 20	>> 20
50	> 20	16.4	>> 20	>> 20	>> 20
60	19.7	10.1	> 20	>20	> 20
70	11.0	5.8	11.0	11.0	11.0

Table 11. Data from M48Z35/Y/AV devices

Temperature (°C)	CAPHAT or SNAPHAT (BR1225, 48 mAh)		SNAPHAT (BR1632, 120 mAh)		V_{CC} duty cycle = 100%, shelf life (years)
	V_{CC} duty cycle = 0%				
	Typical (years)	Worst case (years)	Typical (years)	Worst case (years)	
0	>> 20	>> 20	>> 20	>> 20	>> 20
10	>> 20	> 20	>> 20	>> 20	>> 20
20	>> 20	> 20	>> 20	>> 20	>> 20
25	> 20	17.2	>> 20	>> 20	>> 20
30	> 20	12.9	>> 20	> 20	>> 20
40	14.2	7.5	> 20	18.6	>> 20
50	7.4	3.8	18.4	9.5	>> 20
60	4.5	2.5	11.3	6.2	> 20
70	2.6	1.4	6.5	3.5	11.0

Appendix C TIMEKEEPER® products

Table 12. Data from M48T02/12 devices (available only in CAPHAT™ - BR1632, 120 mAh)

Temperature (°C)	V_{CC} duty cycle = 0%		V_{CC} duty cycle = 100%, shelf life (years)
	Typical (years)	Worst case (years)	
0	> 20	> 20	>> 20
10	> 20	> 20	>> 20
20	> 20	> 20	>> 20
25	> 20	> 20	>> 20
30	> 20	> 20	>> 20
40	> 20	> 20	>> 20
50	> 20	18.5	>> 20
60	19.0	17.0	> 20
70	11.0	11.0	11.0

Table 13. Data from M48T08/Y/18 and M48T58/Y devices

Temperature (°C)	CAPHAT or SNAPHAT (BR1225, 48 mAh)		CAPHAT(1) or SNAPHAT (BR1632, 120 mAh)		V_{CC} duty cycle = 100%, shelf life (years)
	V_{CC} duty cycle = 0%				
	Typical (years)	Worst case (years)	Typical (years)	Worst case (years)	
0	11.0	10.0	> 20	> 20	>> 20
10	10.1	9.2	> 20	> 20	>> 20
20	9.4	8.5	> 20	> 20	>> 20
25	9.0	8.1	> 20	> 20	>> 20
30	8.6	7.6	> 20	19.0	>> 20
40	7.9	6.8	19.7	16.9	>> 20
50	6.9	5.6	17.1	13.9	>> 20
60	5.9	4.5	14.8	11.3	> 20
70	4.8	3.4	11.0	8.4	11.0

1. Only available in M48T08 and M48T18 CAPHAT™.

Table 14. Data from M48T35/Y/AV and M48T37V/Y devices

Temperature (°C)	SNAPHAT (BR1225, 48 mAh)		CAPHAT or SNAPHAT (BR1632, 120 mAh)		V_{CC} duty cycle = 100%, shelf life (years)
	V_{CC} duty cycle = 0%				
	Typical (years)	Worst case (years)	Typical (years)	Worst case (years)	
0	10.4	9.0	> 20	> 20	>> 20
10	9.0	7.6	> 20	19.1	>> 20
20	8.1	6.7	> 20	16.6	>> 20
25	7.4	6.0	18.6	14.9	>> 20
30	6.8	5.3	16.9	13.2	>> 20
40	5.5	4.0	13.8	10.0	>> 20
50	4.0	2.6	10.0	6.6	>> 20
60	2.9	1.9	7.4	4.8	> 20
70	2.0	1.2	5.0	3.0	11.0

Appendix D Serial RTC products

Table 15. Data from M41T56/94, M41ST85W, M41ST87W/Y, and M41ST95W ind. temp. (MH6) devices

Temperature (°C)	SNAPHAT (BR1632, 120 mAh)	V_{CC} duty cycle = 100%, shelf life (years)
	V_{CC} duty cycle = 0%	
	Typical (years)	
–40	> 20	>> 20
–30	> 20	>> 20
–20	> 20	>> 20
–10	> 20	>> 20
0	> 20	>> 20
10	> 20	>> 20
20	> 20	>> 20
25	> 20	>> 20
30	> 20	>> 20
40	> 20	>> 20
50	> 20	>> 20
60	> 20	> 20
70	11.0	11.0
80	4.3	4.3
85	2.7	2.7

Table 16. Data from M41T00/S, M41T11, and M41T81/S industrial temperature (MH6) devices

Temperature (°C)	SNAPHAT (BR1632, 120 mAh) V_{CC} duty cycle = 0% Typical (years)	V_{CC} duty cycle = 100%, shelf life (years)
–40	> 20	>> 20
–30	> 20	>> 20
–20	> 20	>> 20
–10	> 20	>> 20
0	> 20	>> 20
10	> 20	>> 20
20	> 20	>> 20
25	> 20	>> 20
30	> 20	>> 20
40	> 20	>> 20
50	> 20	>> 20
60	> 20	> 20
70	11.0	11.0
80	4.3	4.3
85	2.7	2.7

11 Revision history

Table 17. Document revision history

Date	Revision	Changes
13-Oct-1998	0.0	Document written
14-Dec-1998	1.0	1st edition of ZEROPOWER and TIMEKEEPER application note book
07-Mar-2000	1.1	Data changed from that of 49 mAh and 130 mAh batteries to that of 48 mAh and 120 mAh batteries
25-Apr-2000	1.2	Controllers renamed as supervisors
26-Jun-2000	1.3	M48T35 typ data retention lifetime changed to 7/10 years (Tab-7 on p15)
08-May-2001	2.0	Reformatted, text, graphics, values updated (*Figure 6*, *7*, *8*, *10*; *Table 3*, *5*, *6*, *7*, *15*, *13*, *14*, *16*, *17*)
15-May-2001	2.1	Change trend colors to black (*Figure 6*, *7*, *8*, *10*)
31-May-2005	3.0	Update information (*Figure 1*, *6*, *7*, *8*, *9*, *10*; *Table 1*, *3*, *5*, *6*, *7*, *8*, *9*, *11*, *12*, *13*, *14*, *15*, *16*)
15-Sep-2011	4	Product updates; minor textual updates; revised document presentation.