MAXIM

3½ Digit A/D Converter

General Description

The Maxim ICL7106 and ICL7107 are monolithic analog to digital converters. They have very high input impedances and require no external display drive circuitry. On-board active components include polarity and digit drivers, segment decoders, voltage reference and a clock circuit. The ICL7106 will directly drive a non-multiplexed liquid crystal display (LCD) whereas the ICL7107 will directly drive a common anode light emitting diode (LED) display.

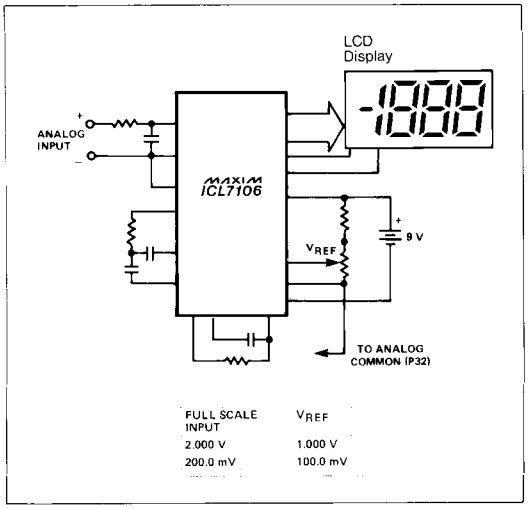
Versatility and accuracy are inherent features of these converters. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input and reference are particularly useful when making ratiometric measurements (ohms or bridge transducers). Maxim has added a zero-integrator phase to the ICL7106 and ICL7107, eliminating overrange hangover and hysteresis effects. Finally, these devices offer high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Typical Operating Circuit



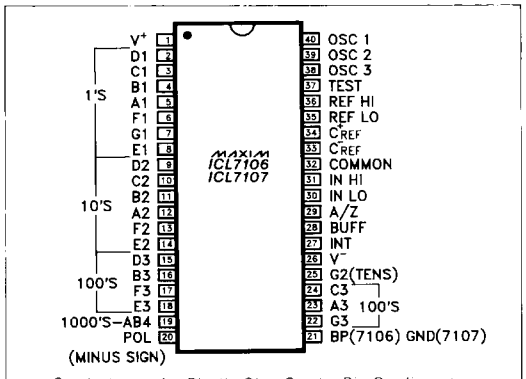
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™")**
- **Guaranteed first reading recovery from overrange**
- **On board Display Drive Capability—no external circuitry required**
  LCD-ICL7106
  LED-ICL7107
- **High Impedance CMOS Differential Inputs**
- **Low Noise (< 15μV p-p) without hysteresis or overrange hangover**
- **Clock and Reference On-Chip**
- **True Differential Reference and Input**
- **True Polarity Indication for Precision Null Applications**
- **Monolithic CMOS design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7106CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7106CJL	0°C to +70°C	40 Lead CERDIP
ICL7106CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7106C/D	0°C to +70°C	Dice
ICL7107CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7107CJL	0°C to +70°C	40 Lead CERDIP
ICL7107CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7107C/D	0°C to +70°C	Dice

Pin Configuration



See last page for Plastic Chip Carrier Pin Configuration.

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

3½ Digit A/D Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- ICL7106, V^+ to V^- 15V
- ICL7107, V^+ to GND ..... +6V
- ICL7107, V^- to GND ..... −9V

Analog Input Voltage (either input)(Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input
- ICL7106 ..... TEST to V^+
- ICL7107 ..... GND to V^+

Power Dissipation (Note 2)
- Plastic Package 1000mW

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF} V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≈ 200.0mV	−1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V. Full Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Input Leakage Current	V_{IN} = 0		1	10	pA
Zero Reading Drift	V_{IN} = 0 0° < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° < T_A < 70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0		0.8	1.8	mA
V^- supply current 7107 only			0.6	1.8	mA
Analog Common Voltage (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply		80		ppm/°C
7106 ONLY Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
7107 ONLY Segment Sinking Current (Except Pin 19) (Pin 19 only)	V^+ = 5.0V Segment voltage = 3V	5 10	8.0 16		mA mA

Note 3: Unless otherwise noted, specifications apply to both the 7106 and 7107 at T_A = 25°C, f_{CLOCK} = 48kHz. 7106 is tested in the circuit of Figure 1. 7107 is tested in the circuit of Figure 2.

Note 4: Refer to "Differential Input" discussion.

Note 5: Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

3½ Digit A/D Converter

- **Guaranteed Overload Recovery Time**
- **Significantly Improved ESD Protection (Note 7)**
- **Low Noise**
- **Key Parameters Guaranteed over Temperature**
- **Negligible Hysteresis**
- **Maxim Quality and Reliability**
- **Increased Maximum Rating for Input Current (Note 8)**

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS: Specifications below satisfy or exceed all "tested" parameters on adjacent page.
(V^+ = 9V; T_A = 25°C; f_{CLOCK} = 48kHz; test circuit - Figure 1; unless noted)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV				
	T_A = 25°C (Note 6)	−000.0	±000.0	+000.0	Digital
	0° ≤ T_A ≤ 70°C (Note 10)	**−000.0**	**±000.0**	**+000.0**	Reading
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV				
	T_A = 25°C (Note 6)	999	999/1000	1000	Digital
	0° ≤ T_A ≤ 70°C (Note 10)	**998**	**999/1000**	**1001**	Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≅ 200.0mV				
	T_A = 25°C (Note 6)	−1	±.2	+1	Counts
	0° ≤ T_A < 70°C (Note 10)		±.2		
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		50		µV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		µV
Input Leakage Current	V_{IN} = 0				
	T_A = 25°C (Note 6)		1	10	pA
	0° ≤ T_A ≤ 70°C		**20**	**200**	
Zero Reading Drift	V_{IN} = 0 0° ≤ T_A ≤ 70°C (Note 6)		0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ 70°C (Ext. Ref. 0ppm/°C) (Note 6)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0				
	T_A = 25°C		0.6	1.8	mA
	0° ≤ T_A ≤ 70°C			**2**	
V^- Supply Current (7107 only)			0.6	1.8	mA
Analog Common Voltage (with respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	25kΩ between Common & Pos. Supply		75		ppm/°C
7106 Only (Note 5) Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V
7107 Only—Segment Sinking Current	V^+ = 5.0V	5	8.0		mA
(Except Pin 19)	Segment Voltage = 3V				
(Pin 19 only)		10	16		mA
7106 Only—Test Pin Voltage	**With Respect to V^+**	**4**	**5**	**6**	**V**
Overload Recovery Time (Note 9)	**V_{IN} changing from ±10V to 0V**		**0**	**1**	**Measurement Cycles**

Note 6: Test condition is V_{IN} applied between pin IH-HI and IN-LO through a 1MΩ series resistor as shown in Figures 1 and 2.

Note 7: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

Note 8: Input voltages may exceed the supply voltage provided the input current is limited to ±1mA (This revises Note 1 on adjacent page).

Note 9: Number of measurement cycles for display to give accurate reading.

Note 10: 1MΩ resistor is removed in Figures 1 and 2.

3½ Digit A/D Converter

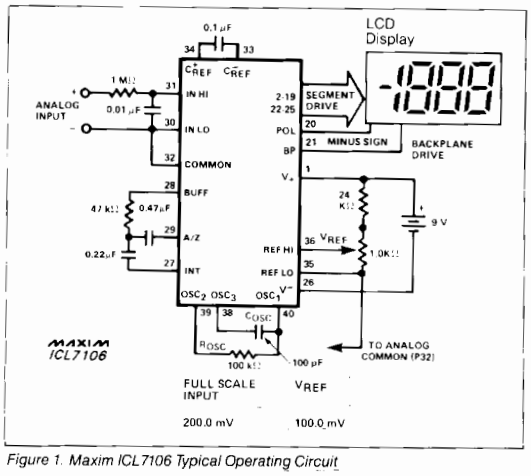


Figure 1. Maxim ICL7106 Typical Operating Circuit

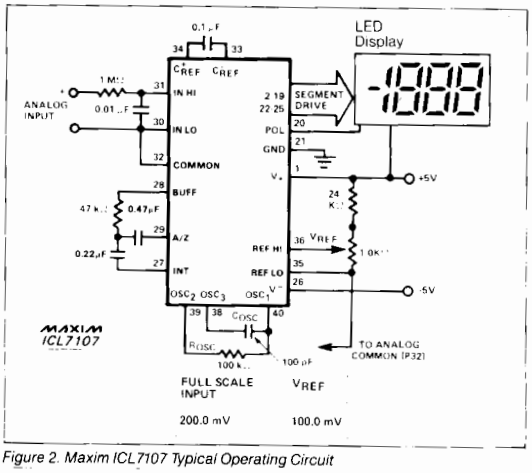


Figure 2. Maxim ICL7107 Typical Operating Circuit

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the ICL7136. Each measurement cycle is divided into four phases:

1. Auto-Zero (A-Z)
2. Signal Integrate (INT)
3. Reference De-Integrate (DI)
4. Zero Integrator (ZI)

Auto-Zero Phase

Three events occur during auto-zero. The inputs, IN-HI and IN-LO, are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. And lastly, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the comparator, buffer amplifier and integrator. The inherent noise of the system determines the A-Z accuracy.

Signal Integrate Phase

The internal input high (IN-HI) and input low (IN-LO) are connected to the external pins, the internal short is removed and the auto-zero loop is opened. The converter then integrates the differential voltage between IN-HI and IN-LO for a fixed time. This differential voltage can be within a wide common-mode range (within one volt of either supply). If, however, the input signal has no return with respect to the converter power supply, IN-LO can be tied to analog common to establish the correct common-mode voltage. The polarity of the integrated signal is determined at the end of this phase.

Reference De-Integrate

IN-HI is connected across the previously charged reference capacitor and IN-LO is internally connected to analog common. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The input signal determines the time required for the output to return to zero. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Zero Integrator Phase

Input low is shorted to analog COMMON and the reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to input high, causing the integrator output to return to zero. This phase normally lasts between 11 and 140 clock pulses but is extended to 740 clock pulses after a "heavy" overrange conversion.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a rollover voltage. This is caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. The reference capacitor can gain charge (increase voltage) if there is a large common-mode voltage. This happens during de-integration of a positive signal. In contrast, the reference capacitor will lose charge (decrease voltage) when de-integrating a negative input signal. Rollover error is caused by this difference in reference for positive or negative input voltages. This error can be held to less than half a count for the worst-case condition by selecting a reference capacitor that is large enough in comparison to the stray capacitance. (See component value selection.)

Differential Input

Differential voltages anywhere within the common-mode range of the input amplifer can be accepted by the input (specifically from 1V below the positive supply to 1.5V above the negative supply). The system has a CMRR of 86dB (typ) in this range. Care must be exercised, however, to ensure that the integrator output does not saturate, since the integrator follows the common-mode voltage. A large positive common-mode voltage with a near full-scale negative differential input voltage is a worst-case condition. When most of the integrator output swing has been used up by the positive common-mode voltage, the negative input signal drives the integrator more positive. The integrator swing can be reduced to less than the recommended 2V full-scale swing with no loss of accuracy in these critical

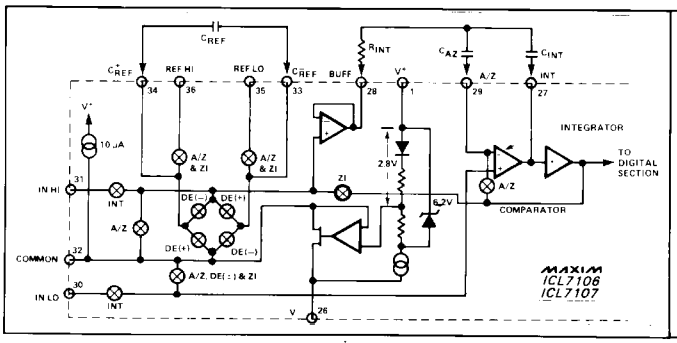


Figure 3. Analog Section of ICL7106/ICL7107

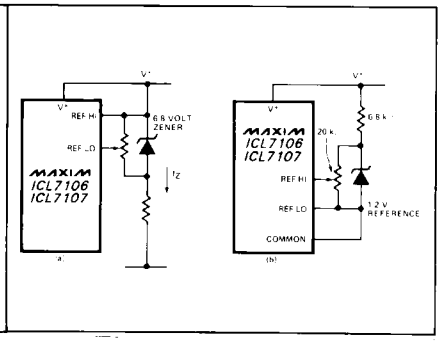


Figure 4. Using an External Reference

applications. The integrator output can swing within 0.3V of either supply without loss of linearity.

Analog Common

The primary purpose of this pin is to set the common-mode voltage for battery operation. This is useful when using the ICL7106, or for any system where the input signals are floating with respect to the power supply. A voltage of approximately 2.8V less than the positive supply is set by this pin. The analog common has some of the attributes of a reference voltage. If the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low output impedance (approximately 15Ω), a temperature coefficient of typically 80ppm/°C, and a low voltage coefficient (.001%).

The internal heating of the ICL7107 by the LED display drivers degrades the stability of Analog Common. The power dissipated by the LED display drivers changes with the displayed count, thereby changing the temperature of the die, which in turn results in a small change in the Analog Common voltage. This combination of variable power dissipation, thermal resistance, and temperature coefficient causes a 25–80μV increase in noise near full scale. Another effect of LED display driver power dissipation can be seen at the transition between a full scale reading and an overload condition. Overload is a low power dissipation condition since the three least significant digits are blanked in overload. On the other hand, a near full scale reading such as 1999 has many segments turned on and is a high power dissipation condition. The difference in power dissipation between overload and full scale may cause a ICL7107 with a negative temperature coefficient reference to cycle between overload and a near full scale display as the die alternately heats and cools. An ICL7107 with a positive TC reference will exhibit hysteresis under these conditions: once put into overload by a voltage just barely more than full scale, the voltage must be reduced by several counts before the ICL7107 will come out of overload.

None of the above problems are encountered when using an external reference. The ICL7106, with its low power dissipation, has none of these problems with either an external reference or when using Analog Common as a reference.

During auto-zero and reference integrate the internal input low is connected to Analog Common. If IN-LO is different from analog-common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. In some applications, however, IN-LO will be set at a fixed known voltage (e.g., power supply common). Whenever possible analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If convenient, REF-LO should be connected to analog common. This will remove the common-mode voltage from the reference system.

Analog Common is internally tied to an N-channel FET that can sink 30mA or more of current. This will hold the Analog Common voltage 2.8V below the positive supply (when a source is trying to pull the common line positive). There is only 10μA of source current, however, so COMMON may easily be tied to a more negative voltage, thus over-riding the internal reference.

Test

Two functions are performed by the test pin. The first is using this pin as the negative supply for externally generated segment drivers or any other annunciators the user may want to include on the LCD. This pin is coupled to the internally generated digital supply through a 500Ω resistor. This application is illustrated in Figures 5 & 6.

A lamp test is the second function. All segments will be turned on and the display should read −1888, when TEST is pulled high (V+).

Caution: In the lamp test mode, the segments have a constant dc voltage (no square wave). This can burn the LCD if left in this mode for several minutes.

3½ Digit A/D Converter

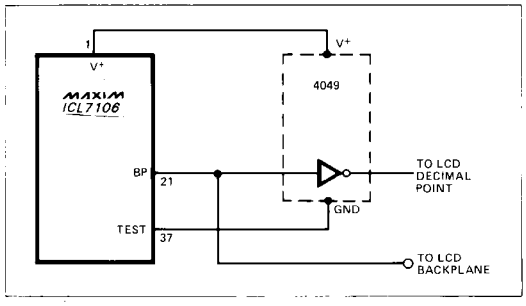


Figure 5A. Fixed Decimal Point Drivers

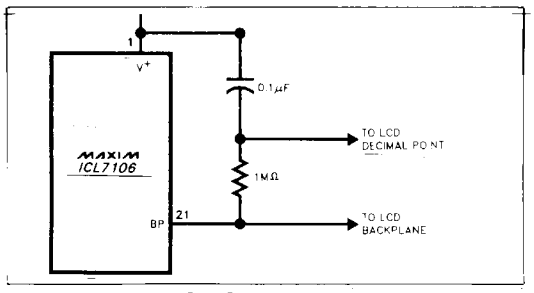


Figure 5B. Fixed Decimal Point Drivers

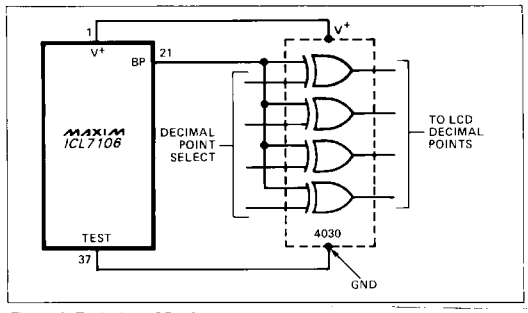


Figure 6. Exclusive "OR" Gate for Decimal Point Drive

Digital Section

The digital section for the ICL7106 and ICL7107 is illustrated in Figures 8 and 9. In Figure 8, an internal digital ground is generated from a 6V zener diode and a large P-channel source follower. This supply is made stiff to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is calculated by dividing the clock frequency by 800. For example, with a clock frequency of 48kHz (3 readings per second), the backplane will be a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude. Note that these are out-of-phase when the segment is ON and in-phase when OFF. Negligible dc voltage exists across the segments in either case.

The ICL7107 is identical to the ICL7106 except that the backplane and drivers have been replaced by N-channel segment drivers. The ICL7107 is designed to drive common anode LED's with a typical segment current of 8mA. Pin 19 (thousands digit output) sinks current from two LED segments, and has a 16mA drive capability.

The polarity indication is "on" for negative analog inputs, for both the ICL7106 and ICL7107. If desired IN-HI and IN-LO can be reversed giving a "on" for positive analog inputs.

System Timing

The clocking circuitry for the ICL7106 and ICL7107 is illustrated in Figure 7. Three approaches can be used:

1. A crystal between pins 39 and 40.
2. An external oscillator connected to pin 40.
3. An RC oscillator using all three pins.

The decade counters are driven by the clock frequency divided by four. This frequency is then further divided to form the four convert-cycle phases, namely: signal integrate (1000 counts), reference de-integrate (0 to 2000 counts), auto-zero (260 to 2989 counts) and zero integrator (11 to 740).

The signal integration should be a multiple of 60Hz to achieve a maximum rejection of 60Hz pickup. Oscillator frequencies of 30kHz, 40kHz, 48kHz, 60kHz, 80kHz, 120kHz, 240kHz, etc., should be selected. Similarly, for 50Hz rejection, oscillator frequencies of 200kHz, 100kHz, 66⅔kHz, 50kHz, 40kHz, etc., are appropriate. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

Auto-zero receives the unused portion of reference deintegrate for signals less than full-scale. A complete measurement cycle is 4,000 counts (16,000 clock pulses), independent of input voltage. As an example, an oscillator frequency of 48kHz would be used to obtain three readings per second.

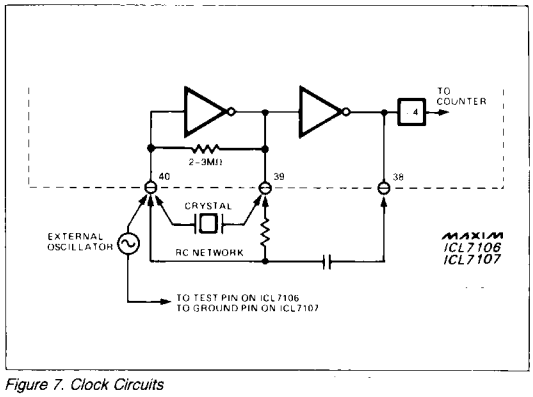


Figure 7. Clock Circuits

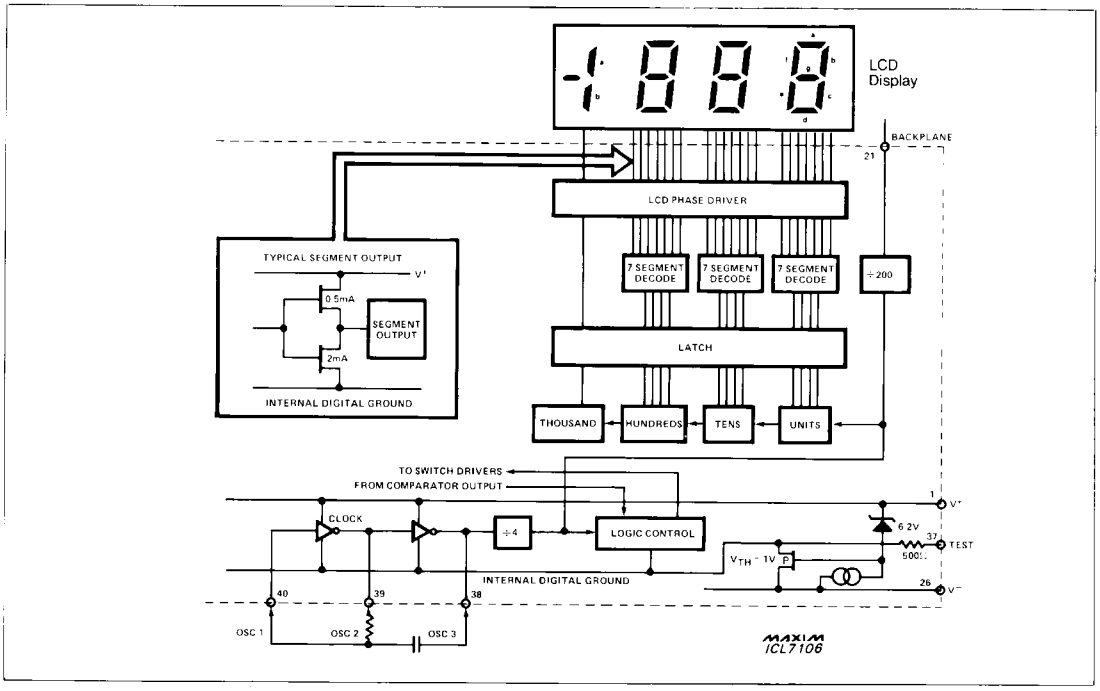


Figure 8. ICL7106 Digital Section

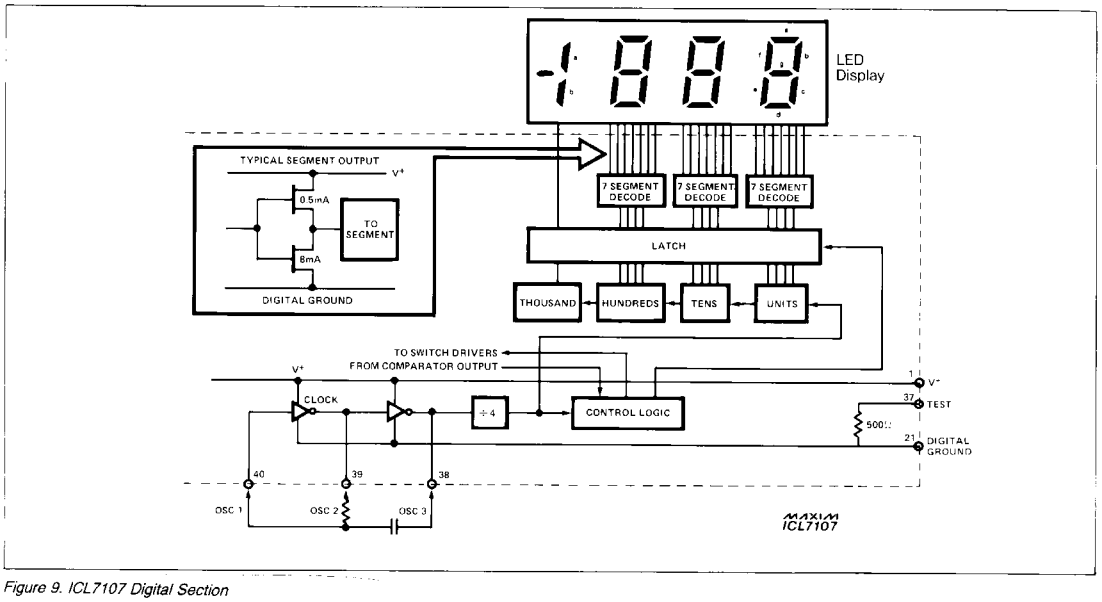


Figure 9. ICL7107 Digital Section

3½ Digit A/D Converter

Component Value Selection

Auto-Zero Capacitor

The noise of the system is influenced by the auto-zero capacitor. For the 2V scale, a 0.047μF capacitor is adequate. A capacitor size of 0.47μF is recommended for 200mV full scale where low noise operation is very important. Due to the ZI phase of Maxim's ICL7106/7, noise can be reduced by using a larger auto-zero capacitor without causing hysteresis or overrange hangover problems seen in other manufacturers' ICL7106/7 which do not have the ZI phase.

Reference Capacitor

For most applications, a 0.1μF capacitor is acceptable. However, a large value is needed to prevent rollover error where a large common-mode voltage exists (i.e., the REF-LO pin is not at analog common) and a 200mV scale is used. Generally, the roll over error will be held half a count by using a 1.0μF capacitor.

Integrating Capacitor

To ensure that the integrator will not saturate (at approximately 0.3V from either supply), an appropriate integrating capacitor must be selected. A nominal ±2V full-scale integrator swing is acceptable for the ICL7106 or ICL7107 when the analog common is used as a reference. A nominal ±3.5 to 4 volt swing is acceptable for the ICL7107 with a ±5V supply and analog common tied to supply ground. The nominal values for C_{INT} is 0.22μF for three readings per second. (48kHz clock). These values should be changed in inverse proportion to maintain the same output swing if different oscillator frequencies are used.

The integrating capacitor must have low dielectric absorption to minimize linearity errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

The integrator and the buffer amplifier both have a class A output stage with 100μA of quiescent current. 20μA of drive current can be supplied with negligible non-linearity. This resistor should be large enough to maintain the amplifiers in the linear region over the entire input voltage range. The resistor value, however, should be low enough that undue leakage requirements are not placed on the PC boards. For a 200mV scale, a 47KΩ resistor is recommended; (2V scale/470KΩ).

Oscillator Components

A 100KΩ resistor is recommended for all ranges of frequency. By using the equation f = 0.45/RC, the capacitor value can be calculated. For 48kHz clock, (3 readings/second), the oscillator capacitor plus stray capacitance should equal 100pF.

Reference Voltage

An analog input voltage of V_{IN} equal to 2 (V_{REF}) is required to generate full scale output of 2000 counts. Thus, for 2V and 200mV scales, V_{REF} should equal 1V and 100mV respectively. However, there will exist a scale factor other than unity between the input voltage and the digital reading in many applications where the A/D is connected to a transducer.

As an example, the designer may like to have a full scale reading in a weighing system when the voltage from the transducer is 0.682V. The designer should use the input voltage directly and select V_{REF} at 0.341V instead of dividing the input down to 200mV. Suitable values of the capacitor and integrating resistor would be 0.22μF and 120KΩ. This provides for a slightly quieter system and also avoids a divider network on the input. The ICL7107 can accept input signals up to ±3.5V with ±5V supplies. Another advantage of this system occurs when the digital reading of zero is desired for $V_{IN} \neq$ zero. Examples are temperature and weighing systems with variable tare. By connecting the voltage transducer between V_{IN} positive and common, and the variable (or fixed) offset voltage between common and V_{IN} negative, the offset reading can be conveniently generated.

ICL7107 Power Supplies

The ICL7107 is designed to operate from ±5V supplies. However, when a negative supply is not available it can be generated from a clock output with two diodes, two capacitors, and an inexpensive IC. Refer to Figure 10. Alternatively a −5V supply can be generated using Maxim's ICL7660 and two capacitors.

A negative supply is not required in selected applications. The conditions to use a single +5V supply are:

- An external reference is used.
- The signal is less than ±1.5V.
- The input signal can be referenced to the center of the common-mode range of the converter.

See Figure 18.

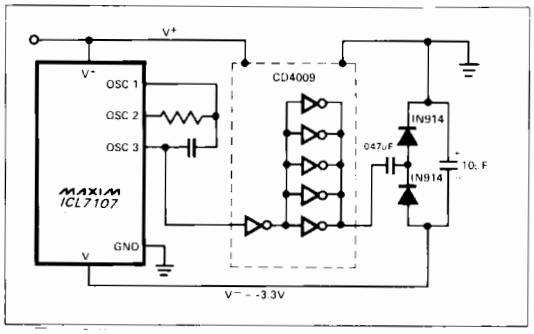


Figure 10. Generating Negative Supply from +5V

Applications Information

Heat is generated within the ICL7107 IC package due to the sinking of LED display current. Fluctuating chip temperature can cause a display to change reading if the internal voltage reference is used. By reducing the power being dissipated such variations can be reduced. The ICL7107 power dissipation is reduced by reducing the LED common anode voltage. The curve tracer illustration showing the relationship between the output current and the output voltage for typical ICL7107 is seen in Figure 11. Note that the typical ICL7107 output is 3.2V (point A), since the typical LED has 1.8V across it (8mA drive current) and its common anode is connected to + 5V. Maximum power dissipation is:

$$8.1mA \times 3.2V \times 24 \text{ segments} = 622mW$$

Once the ICL7107 output voltage is above 2V, the LED current is essentially constant as output voltage increases. Point B illustrates that reducing the output voltage by 0.7V results in 7.7mA of LED current, (only 5% reduction). The maximum power dissipation is a reduction of 26% as calculated by:

$$7.7mA \times 2.5V \times 24 \text{ segments} = 462mW$$

As illustrated in Figure 12, reduced power dissipation is easy to obtain. This can be accomplished by placing either a 5.1Ω resistor or a 1 amp diode in series with the display (but not in series with the ICL7107). Point C of Figure 18 illustrates that a resistor will reduce the ICL7107 output voltage when all 24 segments are "On". The output voltage will increase when segments are turned "Off". On the other hand, the diode will result in a relatively steady output voltage, around Point B. The resistor not only reduces the change in power dissipation as the display changes, but also limits the maximum power dissipation. This is due to the fact that as fewer segments are "On", each "On" output drops more voltage and current. The resistor circuit will change about 230mW when changing from the best case of six segments, a "111" display, to worst-case of a "1888" display. If the resistor is removed, the power dissipation change will be 470mW. The resistor, therefore, will reduce the effect of display dissipation on reference voltage drift by about 50%.

As more segments are turned off, the change in LED brightness caused by the resistor is almost unnoticeable. A diode may be used instead of the resistor if it is important to maintain a steady level of display brightness.

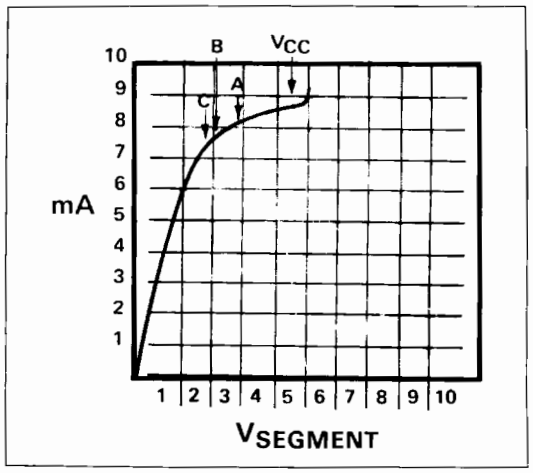


Figure 11. ICL7107 Output Current vs. Output Voltage

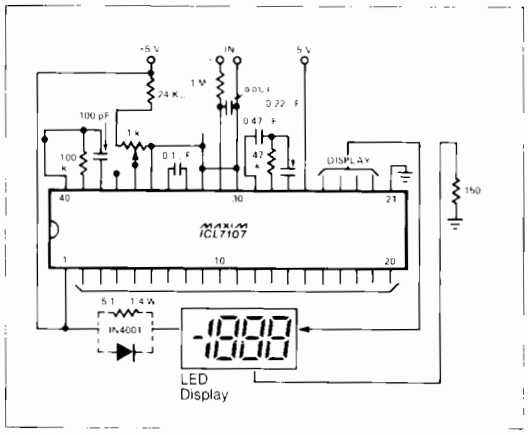


Figure 12. Diode or Resistor Limits Package Power Dissipation

3½ Digit A/D Converter

Typical Applications

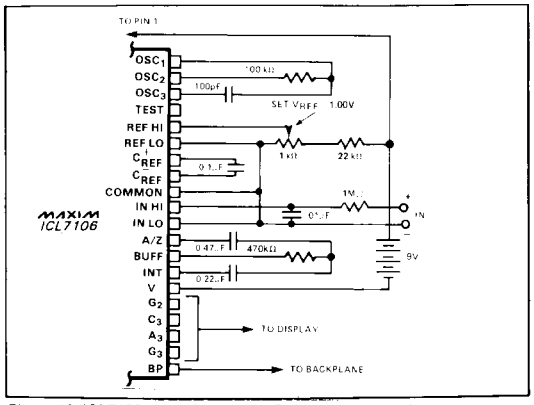


Figure 13. ICL7106 using the Internal Reference. 2V Full Scale; 3 Readings per Second.

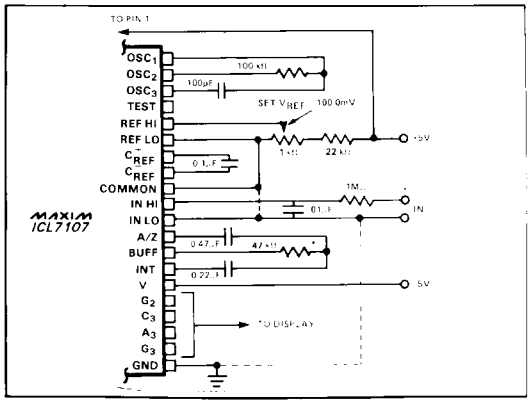


Figure 14. ICL7107 Internal Reference. 200mV Full Scale; 3 Readings per Second, V_{IN} Tied to GND for Single Ended Inputs. (See discussion under "Analog Common".)

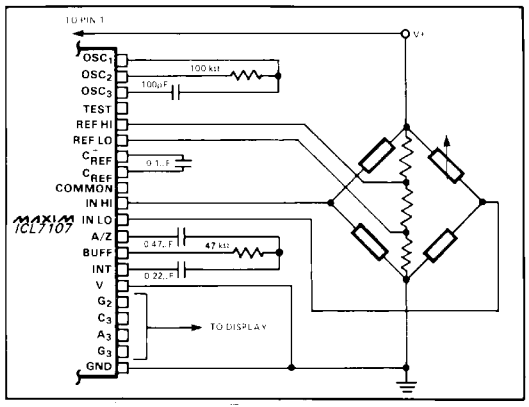


Figure 15. ICL7107 Measuring Ratiometric Values of a Load Cell. Desired Sensitivity is Determined by Resistor Values Within the Bridge.

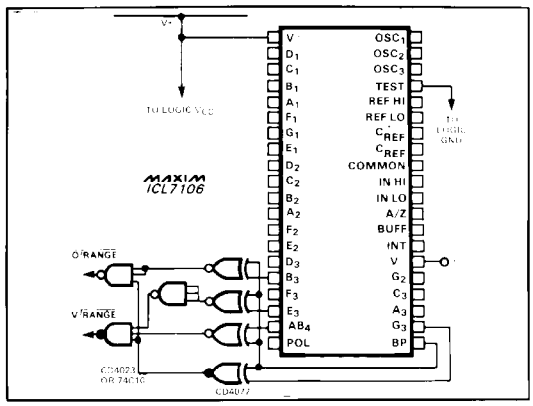


Figure 16. Circuit for Developing Under Range and Over Range Signals from ICL7106 Outputs.

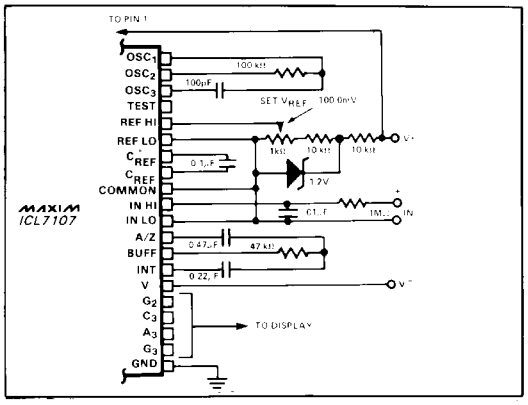


Figure 17. ICL7107 with a 1.2V External Band-Gap Reference V_{IN} tied to common.

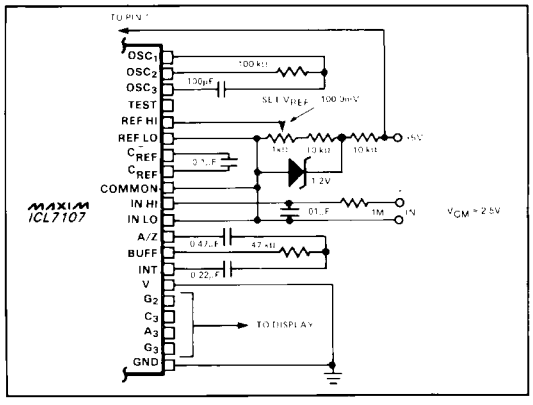


Figure 18. ICL7107 Operated from Single +5V Supply. An external Reference must be used in this application.

Typical Applications

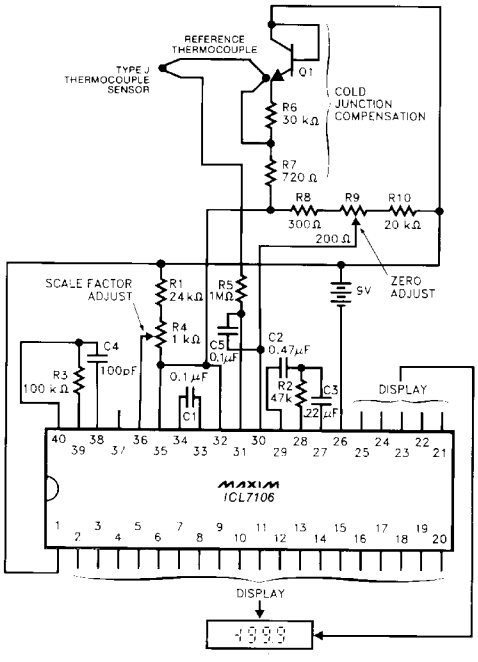


Figure 19. Thermocouple Thermometer. This circuit operates with approximately 50mV reference, so the 50.4μV/°C output of a Type J thermocouple results in 1 count/°C.

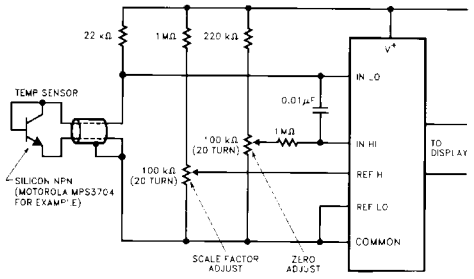


Figure 20. Digital Thermometer

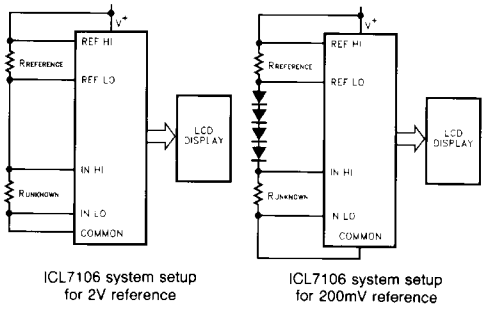
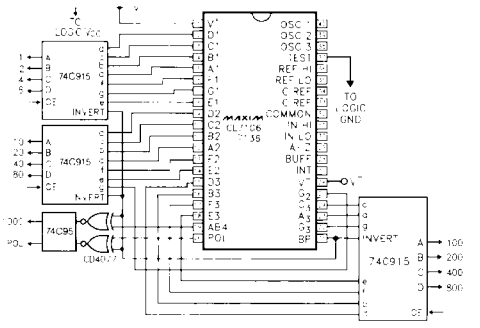
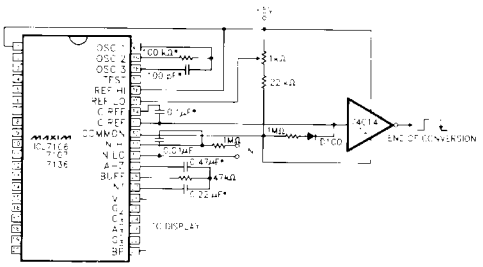


Figure 22. Ratiometric Ohms Measurement



* For ICL7107, tie "INVERT" high, and omit EX-NOR gates.

Figure 21. BCD Output from 7-Segment Drivers

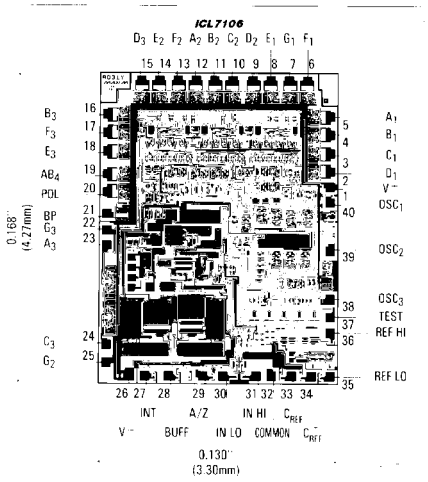


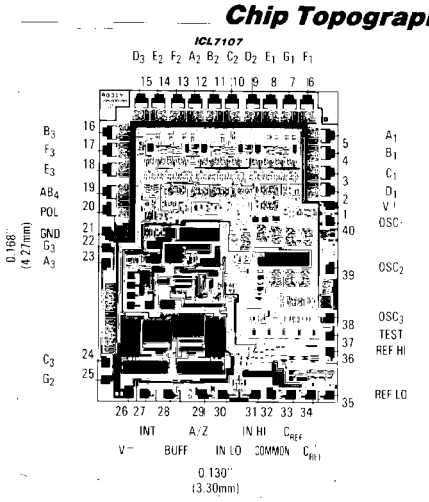
* ICL7106/7 only. See data sheet for values for other parts.

Figure 23. Simple End-of-Conversion Detector

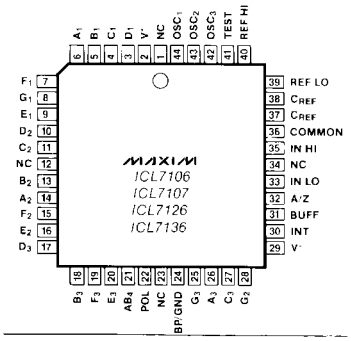
3½ Digit A/D Converter

Chip Topographies





Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pack)

Printed USA 2/87

TC7106/A/TC7107/A

3-1/2 Digit Analog-to-Digital Converters

Features

- Internal Reference with Low Temperature Drift
  - TC7106/7: 80ppm/°C Typical
  - TC7106A/7A: 20ppm/°C Typical
- Drives LCD (TC7106) or LED (TC7107) Display Directly
- Zero Reading with Zero Input
- Low Noise for Stable Display
- Auto-Zero Cycle Eliminates Need for Zero Adjustment
- True Polarity Indication for Precision Null Applications
- Convenient 9V Battery Operation (TC7106A)
- High Impedance CMOS Differential Inputs: $10^{12}\Omega$
- Differential Reference Inputs Simplify Ratiometric Measurements
- Low Power Operation: 10mW

Applications

- Thermometry
- Bridge Readouts: Strain Gauges, Load Cells, Null Detectors
- Digital Meters: Voltage/Current/Ohms/Power, pH
- Digital Scales, Process Monitors
- Portable Instrumentation

Device Selection Table

Package Code	Package	Pin Layout	Temperature Range
CPI	40-Pin PDIP	Normal	0°C to +70°C
IPL	40-Pin PDIP	Normal	-25°C to +85°C
IJL	40-Pin CERDIP	Normal	-25°C to +85°C
CKW	44-Pin PQFP	Formed Leads	0°C to +70°C
CLW	44-Pin PLCC	—	0°C to +70°C

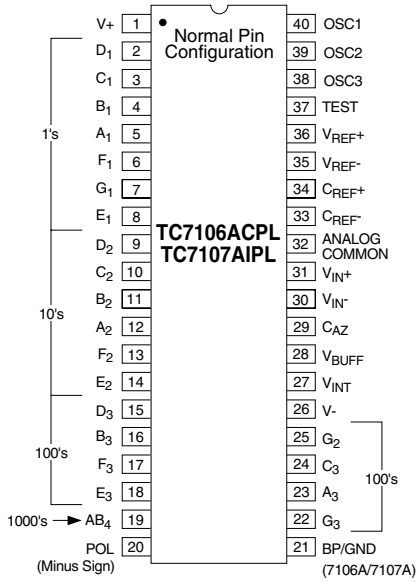
General Description

The TC7106A and TC7107A 3-1/2 digit direct display drive analog-to-digital converters allow existing 7106/7107 based systems to be upgraded. Each device has a precision reference with a 20ppm/°C max temperature coefficient. This represents a 4 to 7 times improvement over similar 3-1/2 digit converters. Existing 7106 and 7107 based systems may be upgraded without changing external passive component values. The TC7107A drives common anode light emitting diode (LED) displays directly with 8mA per segment. A low cost, high resolution indicating meter requires only a display, four resistors, and four capacitors.The TC7106A low power drain and 9V battery operation make it suitable for portable applications.

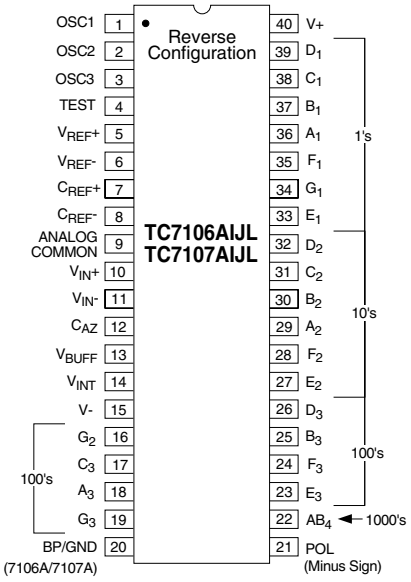
The TC7106A/TC7107A reduces linearity error to less than 1 count. Rollover error – the difference in readings for equal magnitude, but opposite polarity input signals, is below ±1 count. High impedance differential inputs offer 1pA leakage current and a $10^{12}\Omega$ input impedance. The differential reference input allows ratiometric measurements for ohms or bridge transducer measurements. The $15\mu V_{P-P}$ noise performance ensures a “rock solid” reading. The auto-zero cycle ensures a zero display reading with a zero volts input.

Package Type

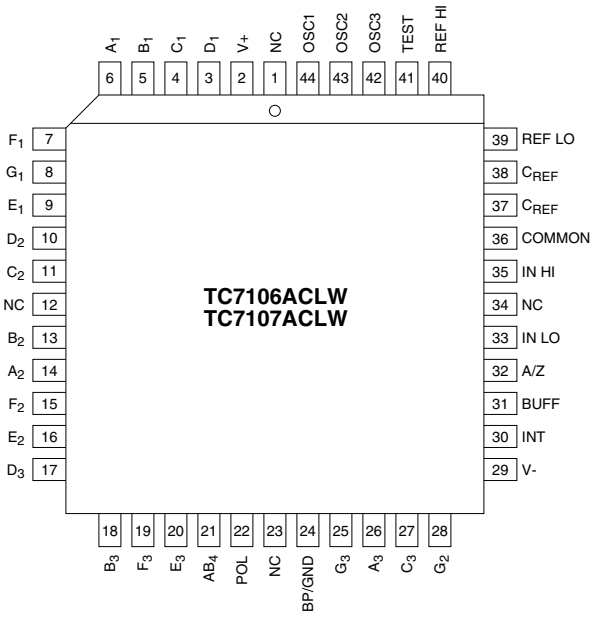
40-Pin PDIP



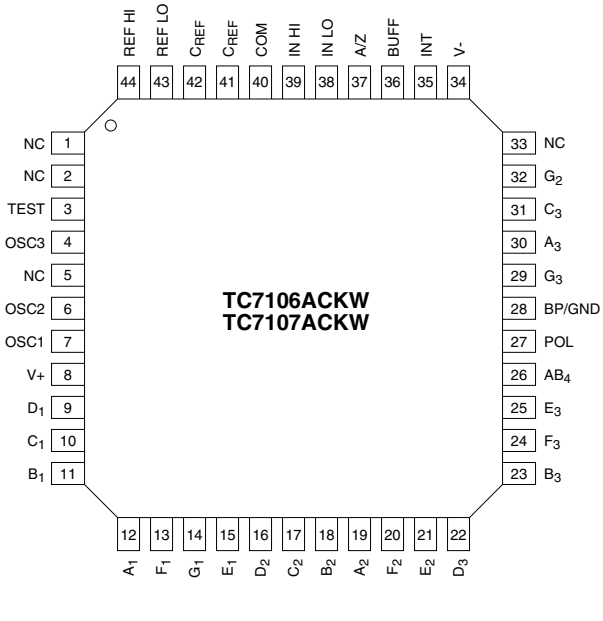
40-Pin CERDIP



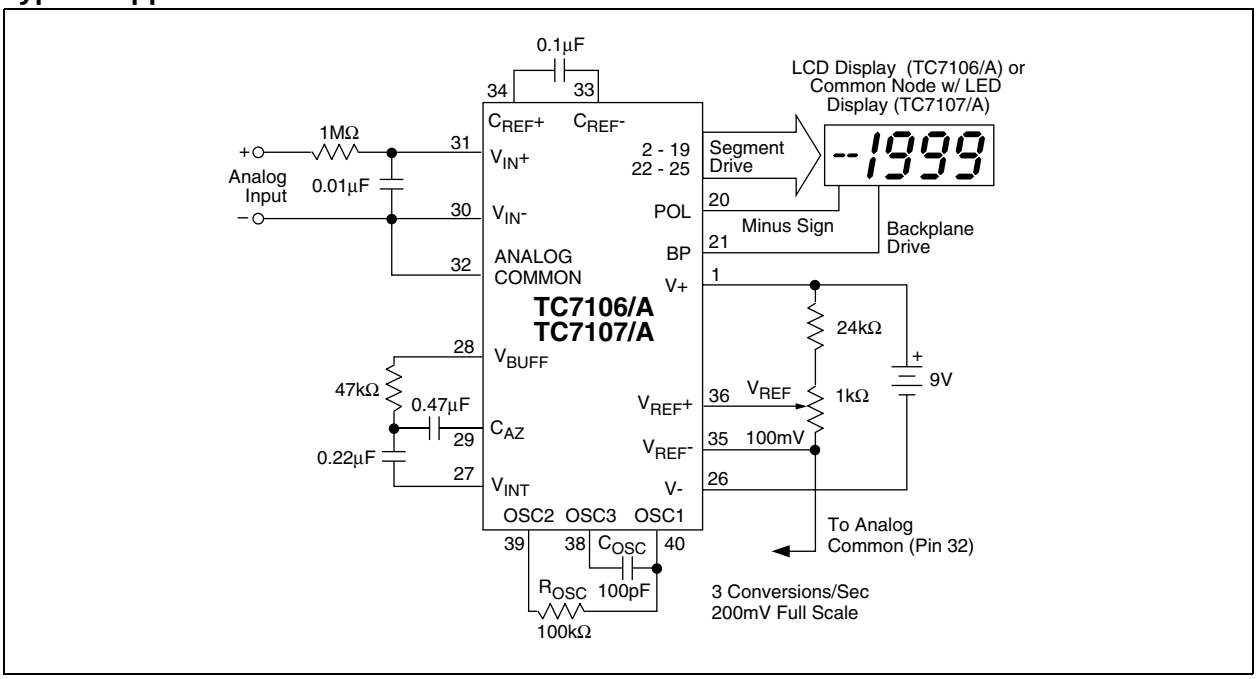
44-Pin PLCC



44-Pin PQFP



Typical Application



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

TC7106A

Supply Voltage (V+ to V-) 15V
Analog Input Voltage (either Input) **(Note 1)** ... V+ to V-
Reference Input Voltage (either Input) ..... V+ to V-
Clock Input ..... Test to V+
Package Power Dissipation ($T_A \leq 70°C$) **(Note 2)**:
- 40-Pin CERDIP 2.29W
- 40-Pin PDIP 1.23W
- 44-Pin PLCC 1.23W
- 44-Pin PQFP 1.00W

Operating Temperature Range:
- C (Commercial) Devices ..... 0°C to +70°C
- I (Industrial) Devices .....-25°C to +85°C

Storage Temperature Range .....-65°C to +150°C

TC7107A

Supply Voltage (V+) .....+6V
Supply Voltage (V-).....-9V
Analog Input Voltage (either Input) **(Note 1)** ... V+ to V-
Reference Input Voltage (either Input) ..... V+ to V-
Clock Input .....GND to V+
Package Power Dissipation ($T_A \leq 70°C$) **(Note 2)**:
- 40-Pin CERDip.....2.29W
- 40-Pin PDIP 1.23W
- 44-Pin PLCC 1.23W
- 44-Pin PQFP 1.00W

Operating Temperature Range:
- C (Commercial) Devices ..... 0°C to +70°C
- I (Industrial) Devices .....-25°C to +85°C

Storage Temperature Range .....-65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC7106/A AND TC7107/A ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise noted, specifications apply to both the TC7106/A and TC7107/A at T_A = 25°C, f_{CLOCK} = 48kHz. Parts are tested in the circuit of the Typical Operating Circuit.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Z_{IR}	Zero Input Reading	-000.0	±000.0	+000.0	Digital Reading	V_{IN} = 0.0V Full Scale = 200.0mV
	Ratiometric Reading	999	999/1000	1000	Digital Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV
R/O	Rollover Error (Difference in Reading for Equal Positive and Negative Reading Near Full Scale)	-1	±0.2	+1	Counts	V_{IN}- = + V_{IN}+ ≅ 200mV
	Linearity (Max. Deviation from Best Straight Line Fit)	-1	±0.2	+1	Counts	Full Scale = 200mV or Full Scale = 2.000V

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100µA.
2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3: Refer to “Differential Input” discussion.
4: Backplane drive is in phase with segment drive for “OFF” segment, 180° out of phase for “ON” segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

TC7106/A AND TC7107/A ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise noted, specifications apply to both the TC7106/A and TC7107/A at T_A = 25°C, f_{CLOCK} = 48kHz. Parts are tested in the circuit of the Typical Operating Circuit.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CMRR	Common Mode Rejection Ratio **(Note 3)**	—	50	—	µV/V	V_{CM} = ±1V, V_{IN} = 0V, Full Scale = 200.0mV
e_N	Noise (Peak to Peak Value not Exceeded 95% of Time)	—	15	—	µV	V_{IN} = 0V Full Scale - 200.0mV
I_L	Leakage Current at Input	—	1	10	pA	V_{IN} = 0V
	Zero Reading Drift	—	0.2	1	µV/°C	V_{IN} = 0V "C" Device = 0°C to +70°C
		—	1.0	2	µV/°C	V_{IN} = 0V "I" Device = -25°C to +85°C
TC_{SF}	Scale Factor Temperature Coefficient	—	1	5	ppm/°C	V_{IN} = 199.0mV, "C" Device = 0°C to +70°C (Ext. Ref = 0ppm°C)
		—	—	20	ppm/°C	V_{IN} = 199.0mV "I" Device = -25°C to +85°C
I_{DD}	Supply Current (Does not include LED Current For TC7107/A)	—	0.8	1.8	mA	V_{IN} = 0.8
V_C	Analog Common Voltage (with Respect to Positive Supply)	2.7	3.05	3.35	V	25kΩ Between Common and Positive Supply
V_{CTC}	Temperature Coefficient of Analog Common (with Respect to Positive Supply)	—	—	—	—	25kΩ Between Common and Positive Supply
		7106/7/A 7106/7	20 80	50 —	ppm/°C ppm/°C	0°C ≤ T_A ≤ +70°C ("C" Commercial Temperature Range Devices)
V_{CTC}	Temperature Coefficient of Analog Common (with Respect to Positive Supply)	—	—	75	ppm/°C	0°C ≤ T_A ≤ +70°C ("I" Industrial Temperature Range Devices)
V_{SD}	TC7106A ONLY Peak to Peak Segment Drive Voltage	4	5	6	V	V+ to V- = 9V **(Note 4)**
V_{BD}	TC7106A ONLY Peak to Peak Backplane Drive Voltage	4	5	6	V	V+ to V- = 9V **(Note 4)**
	TC7107A ONLY Segment Sinking Current (Except Pin 19)	5	8.0	—	mA	V+ = 5.0V Segment Voltage = 3V
	TC7107A ONLY Segment Sinking Current (Pin 19)	10	16	—	mA	V+ = 5.0V Segment Voltage = 3V

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100µA.

2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

3: Refer to "Differential Input" discussion.

4: Backplane drive is in phase with segment drive for "OFF" segment, 180° out of phase for "ON" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number (40-Pin PDIP) Normal	Pin No. (40-Pin PDIP) (Reversed	Symbol	Description
1	(40)	V+	Positive supply voltage.
2	(39)	D_1	Activates the D section of the units display.
3	(38)	C_1	Activates the C section of the units display.
4	(37)	B_1	Activates the B section of the units display.
5	(36)	A_1	Activates the A section of the units display.
6	(35)	F_1	Activates the F section of the units display.
7	(34)	G_1	Activates the G section of the units display.
8	(33)	E_1	Activates the E section of the units display.
9	(32)	D_2	Activates the D section of the tens display.
10	(31)	C_2	Activates the C section of the tens display.
11	(30)	B_2	Activates the B section of the tens display.
12	(29)	A_2	Activates the A section of the tens display.
13	(28)	F_2	Activates the F section of the tens display.
14	(27)	E_2	Activates the E section of the tens display.
15	(26)	D_3	Activates the D section of the hundreds display.
16	(25)	B_3	Activates the B section of the hundreds display.
17	(24)	F_3	Activates the F section of the hundreds display.
18	(23)	E_3	Activates the E section of the hundreds display.
19	(22)	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	POL	Activates the negative polarity display.
21	(20)	BP/GND	LCD Backplane drive output (TC7106A). Digital Ground (TC7107A).
22	(19)	G_3	Activates the G section of the hundreds display.
23	(18)	A_3	Activates the A section of the hundreds display.
24	(17)	C_3	Activates the C section of the hundreds display.
25	(16)	G_2	Activates the G section of the tens display.
26	(15)	V-	Negative power supply voltage.
27	(14)	V_{INT}	Integrator output. Connection point for integration capacitor. See INTEGRATING CAPACITOR section for more details.
28	(13)	V_{BUFF}	Integration resistor connection. Use a 47kΩ resistor for a 200mV full scale range and a 47kΩ resistor for 2V full scale range.
29	(12)	C_{AZ}	The size of the auto-zero capacitor influences system noise. Use a 0.47µF capacitor for 200mV full scale, and a 0.047µF capacitor for 2V full scale. See Section 7.1 on Auto-Zero Capacitor for more details.
30	(11)	V_{IN}-	The analog LOW input is connected to this pin.
31	(10)	V_{IN}+	The analog HIGH input signal is connected to this pin.
32	(9)	ANALOG COMMON	This pin is primarily used to set the Analog Common mode voltage for battery operation or in systems where the input signal is referenced to the power supply. It also acts as a reference voltage source. See Section 8.3 on ANALOG COMMON for more details.
33	(8)	C_{REF}-	See Pin 34.
34	(7)	C_{REF}+	A 0.1µF capacitor is used in most applications. If a large Common mode voltage exists (for example, the V_{IN}- pin is not at analog common), and a 200mV scale is used, a 1µF capacitor is recommended and will hold the rollover error to 0.5 count.
35	(6)	V_{REF}-	See Pin 36.

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number (40-Pin PDIP) Normal	Pin No. (40-Pin PDIP) (Reversed	Symbol	Description
36	(5)	$V_{REF}+$	The analog input required to generate a full scale output (1999 counts). Place 100mV between Pins 35 and 36 for 199.9mV full scale. Place 1V between Pins 35 and 36 for 2V full scale. See paragraph on Reference Voltage.
37	(4)	TEST	Lamp test. When pulled HIGH (to V+) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	(3)	OSC3	See Pin 40.
39	(2)	OSC2	See Pin 40.
40	(1)	OSC1	Pins 40, 39, 38 make up the oscillator section. For a 48kHz clock (3 readings per section), connect Pin 40 to the junction of a 100kΩ resistor and a 100pF capacitor. The 100kΩ resistor is tied to Pin 39 and the 100pF capacitor is tied to Pin 38.

3.0 DETAILED DESCRIPTION

(All Pin designations refer to 40-Pin PDIP.)

3.1 Dual Slope Conversion Principles

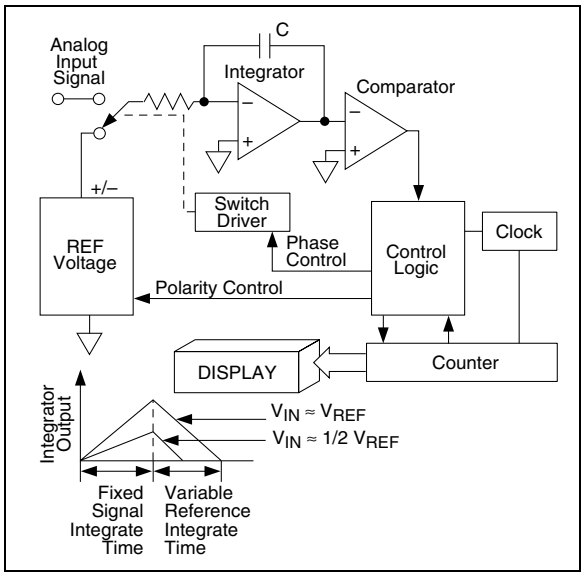
The TC7106A and TC7107A are dual slope, integrating analog-to-digital converters. An understanding of the dual slope conversion technique will aid in following the detailed operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (De-integration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}). See Figure 3-1.

FIGURE 3-1: BASIC DUAL SLOPE CONVERTER



In a simple dual slope converter, a complete conversion requires the integrator output to “ramp-up” and “ramp-down.” A simple mathematical equation relates the input signal, reference voltage and integration time.

EQUATION 3-1:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)dt = \frac{V_R T_{RI}}{RC}$$

Where:

V_R = Reference voltage
T_{SI} = Signal integration time (fixed)
T_{RI} = Reference voltage integration time (variable).

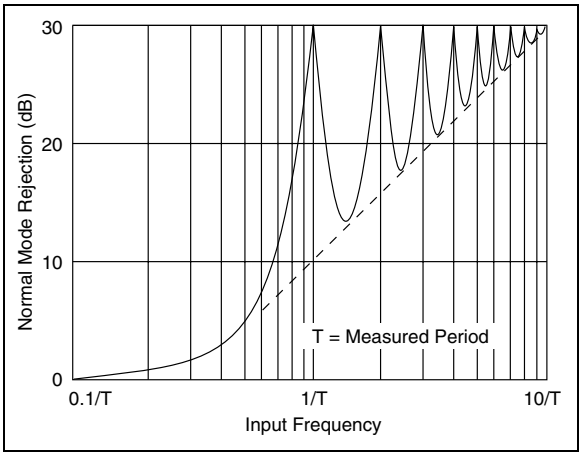
For a constant V_{IN}:

EQUATION 3-2:

$$V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60Hz power line period (see Figure 3-2).

FIGURE 3-2: NORMAL MODE REJECTION OF DUAL SLOPE CONVERTER



4.0 ANALOG SECTION

In addition to the basic signal integrate and de-integrate cycles discussed, the circuit incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without adjusting external potentiometers. A complete conversion consists of three cycles: an auto-zero, signal integrate and reference integrate cycle.

4.1 Auto-Zero Cycle

During the auto-zero cycle, the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The offset error referred to the input is less than 10µV.

The auto-zero cycle length is 1000 to 3000 counts.

4.2 Signal Integrate Cycle

The auto-zero loop is entered and the internal differential inputs connect to $V_{IN}+$ and $V_{IN}-$. The differential input signal is integrated for a fixed time period. The TC7136/A signal integration period is 1000 clock periods or counts. The externally set clock frequency is divided by four before clocking the internal counters.

The integration time period is:

EQUATION 4-1:

$$T_{SI} = \frac{4}{F_{OSC}} \times 1000$$

Where: F_{OSC} = external clock frequency.

The differential input voltage must be within the device Common mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, $V_{IN}-$ should be tied to analog common.

Polarity is determined at the end of signal integrate phase. The sign bit is a true polarity indication, in that signals less than 1LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

4.3 Reference Integrate Phase

The third phase is reference integrate or de-integrate. $V_{IN}-$ is internally connected to analog common and $V_{IN}+$ is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero.

The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 counts.

The digital reading displayed is:

EQUATION 4-2:

$$1000 = \frac{V_{IN}}{V_{REF}}$$

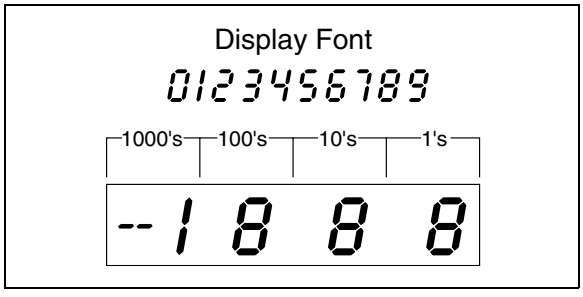
5.0 DIGITAL SECTION (TC7106A)

The TC7106A (Figure 5-2) contains all the segment drivers necessary to directly drive a 3-1/2 digit liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions/second, the backplane frequency is 60Hz with a 5V nominal amplitude. When a segment driver is in phase with the backplane signal, the segment is “OFF.” An out of phase segment drive signal causes the segment to be “ON” or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver is “ON” for negative analog inputs. If $V_{IN}+$ and $V_{IN}-$ are reversed, this indicator will reverse.

When the TEST pin on the TC7106A is pulled to V+, all segments are turned “ON.” The display reads -1888. During this mode, the LCD segments have a constant DC voltage impressed. DO NOT LEAVE THE DISPLAY IN THIS MODE FOR MORE THAN SEVERAL MINUTES! LCD displays may be destroyed if operated with DC levels for extended periods.

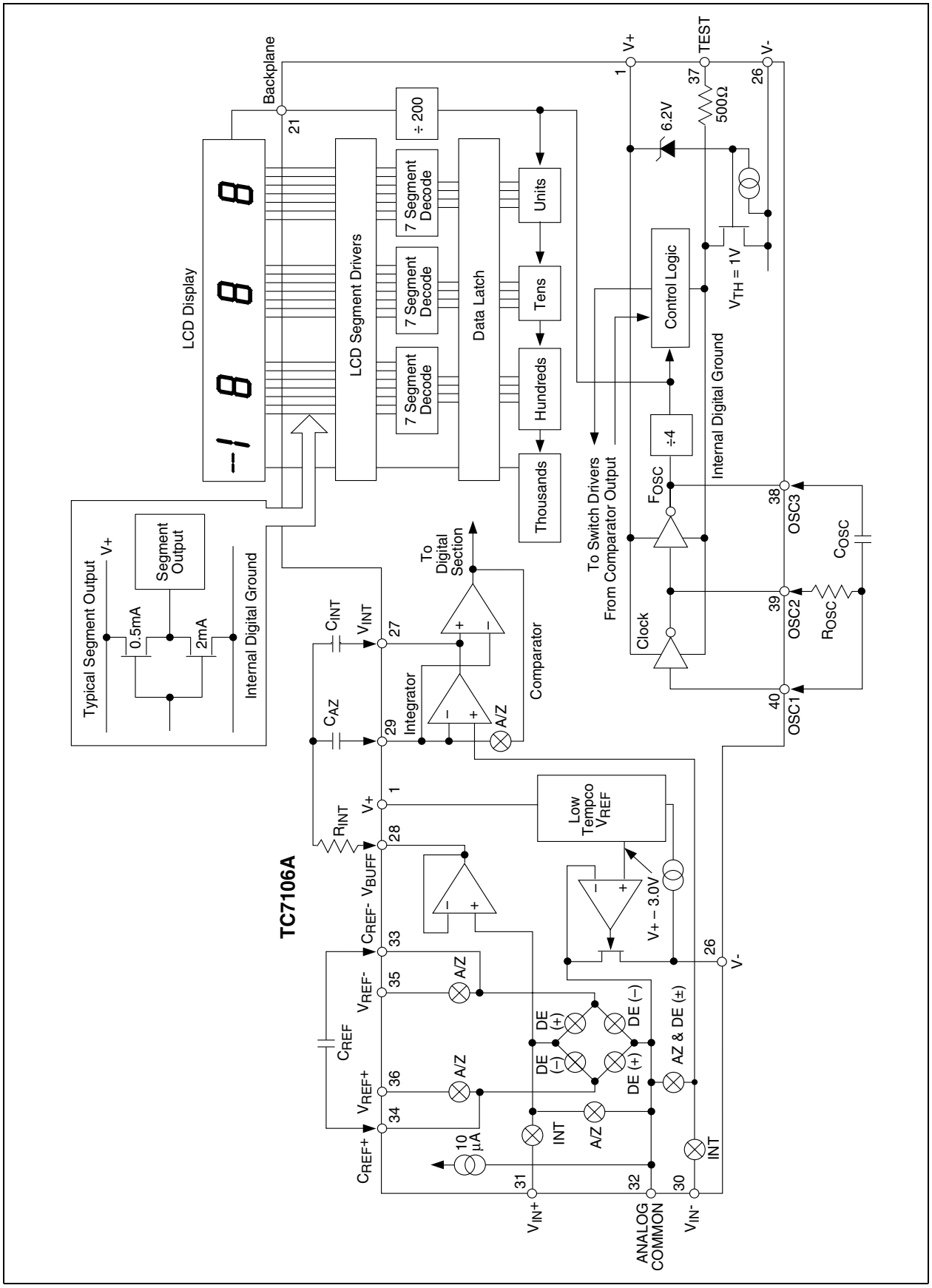
The display font and the segment drive assignment are shown in Figure 5-1.

FIGURE 5-1: DISPLAY FONT AND SEGMENT ASSIGNMENT



In the TC7106A, an internal digital ground is generated from a 6-volt zener diode and a large P channel source follower. This supply is made stiff to absorb the large capacitive currents when the backplane voltage is switched.

FIGURE 5-2: TC7106A BLOCK DIAGRAM



6.0 DIGITAL SECTION (TC7107A)

Figure 6-2 shows a TC7107A block diagram. It is designed to drive common anode LEDs. It is identical to the TC7106A, except that the regulated supply and backplane drive have been eliminated and the segment drive is typically 8mA. The 1000's output (Pin 19) sinks current from two LED segments, and has a 16mA drive capability.

In both devices, the polarity indication is “ON” for negative analog inputs. If V_{IN}- and V_{IN}+ are reversed, this indication can be reversed also, if desired.

The display font is the same as the TC7106A.

6.1 System Timing

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The four-phase measurement cycle takes a total of 4000 counts, or 16,000 clock pulses. The 4000-count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

1. Auto-zero phase: 1000 to 3000 counts (4000 to 12000 clock pulses).

For signals less than full scale, the auto-zero phase is assigned the unused reference integrate time period:

2. Signal integrate: 1000 counts (4000 clock pulses).

This time period is fixed. The integration period is:

EQUATION 6-1:

$$T_{SI} = 4000 \left(\frac{1}{F_{OSC}} \right)$$

Where: F_{OSC} is the externally set clock frequency.

3. Reference Integrate: 0 to 2000 counts (0 to 8000 clock pulses).

The TC7106A/7107A are drop-in replacements for the 7106/7107 parts. External component value changes are not required to benefit from the low drift internal reference.

6.2 Clock Circuit

Three clocking methods may be used (see Figure 6-1):

1. An external oscillator connected to Pin 40.
2. A crystal between Pins 39 and 40.
3. An RC oscillator using all three pins.

FIGURE 6-1: CLOCK CIRCUITS

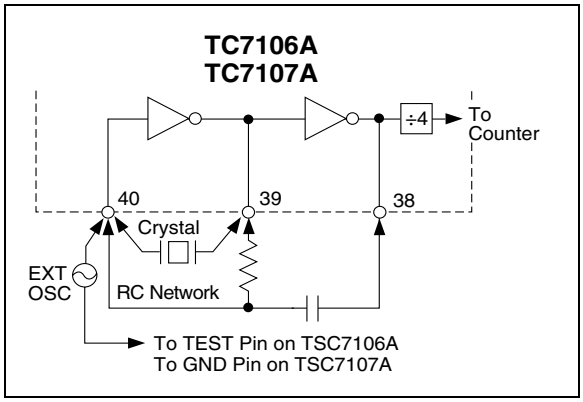
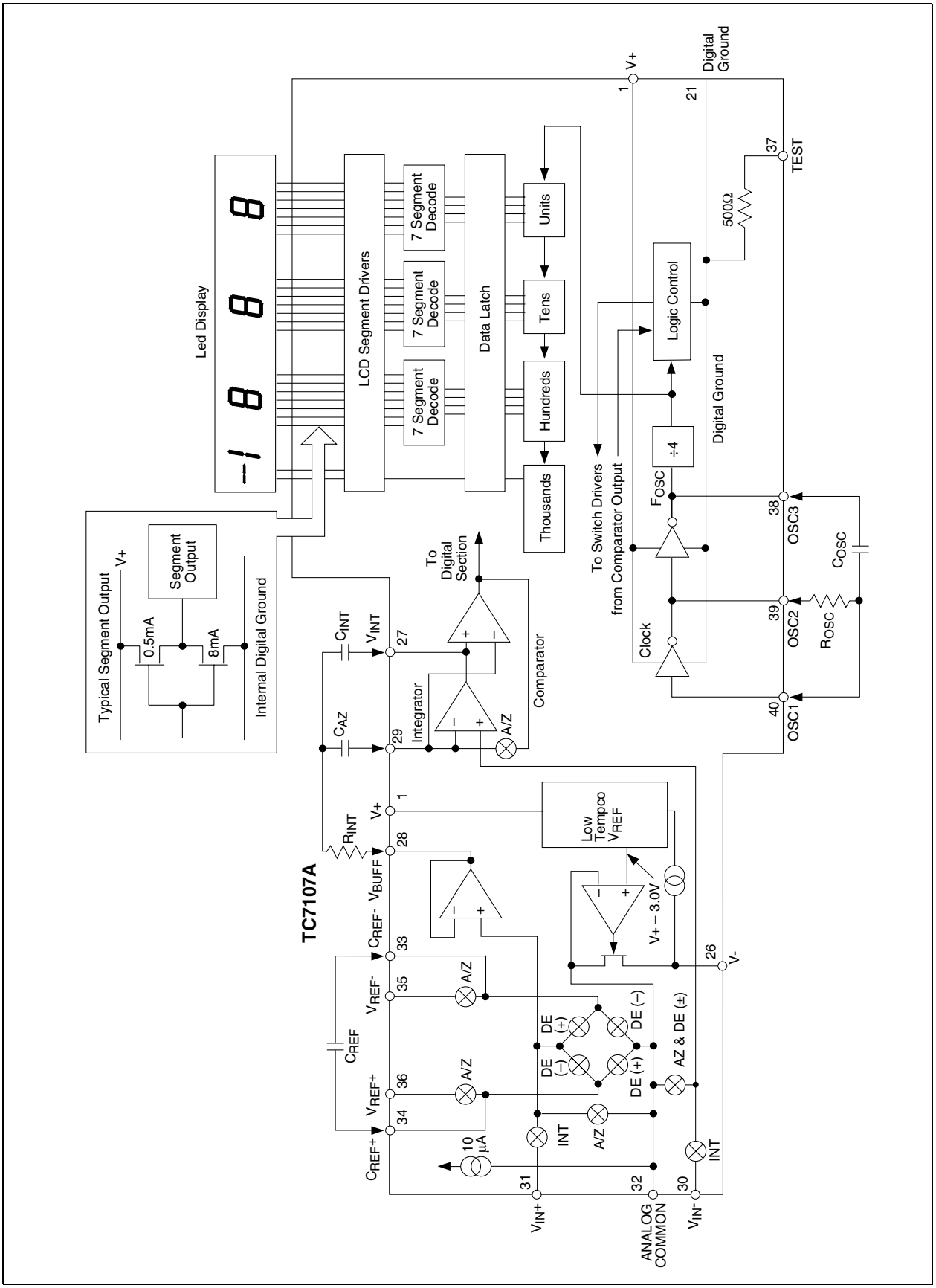


FIGURE 6-2: TC7107A BLOCK DIAGRAM



7.0 COMPONENT VALUE SELECTION

7.1 Auto-Zero Capacitor (C_{AZ})

The C_{AZ} capacitor size has some influence on system noise. A 0.47µF capacitor is recommended for 200mV full scale applications where 1LSB is 100µV. A 0.047µF capacitor is adequate for 2.0V full scale applications. A mylar type dielectric capacitor is adequate.

7.2 Reference Voltage Capacitor (C_{REF})

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1µF capacitor is acceptable when V_{IN}- is tied to analog common. If a large Common mode voltage exists (V_{REF}- – analog common) and the application requires 200mV full scale, increase C_{REF} to 1.0µF. Rollover error will be held to less than 1/2 count. A mylar dielectric capacitor is adequate.

7.3 Integrating Capacitor (C_{INT})

C_{INT} should be selected to maximize the integrator output voltage swing without causing output saturation. Due to the TC7106A/7107A superior temperature coefficient specification, analog common will normally supply the differential voltage reference. For this case, a ±2V full scale integrator output swing is satisfactory. For 3 readings/second (F_{OSC} = 48kHz), a 0.22µF value is suggested. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2V integrator swing.

An exact expression for C_{INT} is:

EQUATION 7-1:

$$C_{INT} = \frac{(4000)\left(\frac{1}{F_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}}$$

Where:

F_{OSC} = Clock Frequency at Pin 38
V_{FS} = Full Scale Input Voltage
R_{INT} = Integrating Resistor
V_{INT} = Desired Full Scale Integrator Output Swing

C_{INT} must have low dielectric absorption to minimize rollover error. A polypropylene capacitor is recommended.

7.4 Integrating Resistor (R_{INT})

The input buffer amplifier and integrator are designed with class A output stages. The output stage idling current is 100µA. The integrator and buffer can supply 20µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region, but not so large that printed circuit board leakage currents induce errors. For a 200mV full scale, R_{INT} is 47kΩ. 2.0V full scale requires 470kΩ.

Component Value	Nominal Full Scale Voltage	
	200.0mV	2.000V
C_{AZ}	0.47µF	0.047µF
R_{INT}	47kΩ	470kΩ
C_{INT}	0.22µF	0.22µF

Note: F_{OSC} = 48kHz (3 readings per sec).

7.5 Oscillator Components

R_{OSC} (Pin 40 to Pin 39) should be 100kΩ. C_{OSC} is selected using the equation:

EQUATION 7-2:

$$F_{OSC} = \frac{0.45}{RC}$$

For F_{OSC} of 48kHz, C_{OSC} is 100pF nominally.

Note that F_{OSC} is divided by four to generate the TC7106A internal control clock. The backplane drive signal is derived by dividing F_{OSC} by 800.

To achieve maximum rejection of 60Hz noise pickup, the signal integrate period should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 200kHz, 100kHz, 66-2/3kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz.

7.6 Reference Voltage Selection

A full scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full Scale Voltage*	V_{REF}
200.0mV	100.0mV
2.000V	1.000V

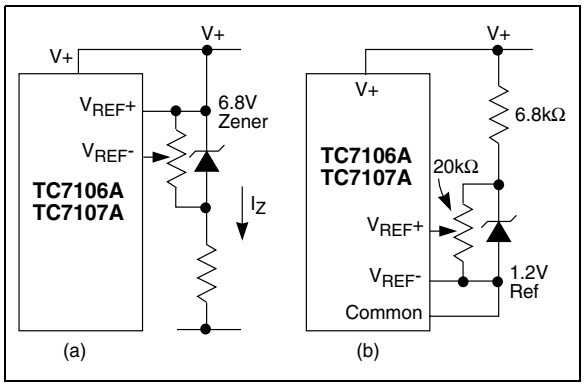
* $V_{FS} = 2V_{REF}$.

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 400mV for 2000 lb/in^2. Rather than dividing the input voltage by two, the reference voltage should be set to 200mV. This permits the transducer input to be used directly.

The differential reference can also be used when a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}-. The transducer output is connected between V_{IN}+ and analog common.

The internal voltage reference potential available at analog common will normally be used to supply the converter's reference. This potential is stable whenever the supply potential is greater than approximately 7V. In applications where an externally generated reference voltage is desired, refer to Figure 7-1.

FIGURE 7-1: EXTERNAL REFERENCE



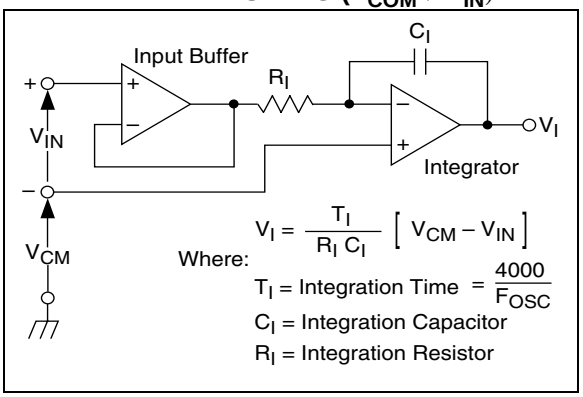
8.0 DEVICE PIN FUNCTIONAL DESCRIPTION

8.1 Differential Signal Inputs V_{IN}+ (Pin 31), V_{IN}- (Pin 30)

The TC7106A/7017A is designed with true differential inputs and accepts input signals within the input stage common mode voltage range (V_{CM}). The typical range is V+ – 1.0 to V+ + 1V. Common mode voltages are removed from the system when the TC7106A/TC7107A operates from a battery or floating power source (isolated from measured system) and V_{IN}- is connected to analog common (V_{COM}) (see Figure 8-2).

In systems where Common mode voltages exist, the 86dB Common mode rejection ratio minimizes error. Common mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worst case condition exists if a large positive V_{CM} exists in conjunction with a full scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (see Figure 8-1). For such applications the integrator output swing can be reduced below the recommended 2.0V full scale swing. The integrator output will swing within 0.3V of V+ or V- without increasing linearity errors.

FIGURE 8-1: COMMON MODE VOLTAGE REDUCES AVAILABLE INTEGRATOR SWING ($V_{COM} \neq V_{IN}$)



8.2 Differential Reference V_{REF}+ (Pin 36), V_{REF}- (Pin 35)

The reference voltage can be generated anywhere within the V+ to V- power supply range.

To prevent rollover type errors being induced by large Common mode voltages, C_{REF} should be large compared to stray node capacitance.

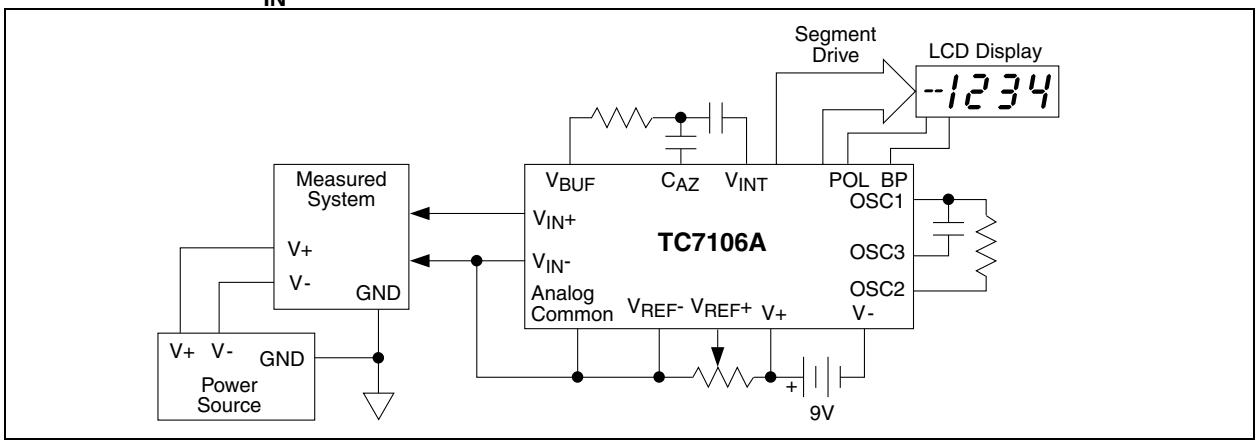
The TC7106A/TC7107A circuits have a significantly lower analog common temperature coefficient. This gives a very stable voltage suitable for use as a reference. The temperature coefficient of analog common is 20ppm/°C typically.

8.3 Analog Common (Pin 32)

The analog common pin is set at a voltage potential approximately 3.0V below V+. The potential is between 2.7V and 3.35V below V+. Analog common is tied internally to the N channel FET capable of sinking 20mA. This FET will hold the common line at 3.0V should an external load attempt to pull the common line toward V+. Analog common source current is limited to 10µA. Analog common is, therefore, easily pulled to a more negative voltage (i.e., below V+ – 3.0V).

The TC7106A connects the internal V_{IN}+ and V_{IN}- inputs to analog common during the auto-zero cycle. During the reference integrate phase, V_{IN}- is connected to analog common. If V_{IN}- is not externally connected to analog common, a Common mode voltage exists. This is rejected by the converter's 86dB Common mode rejection ratio. In battery operation, analog common and V_{IN}- are usually connected, removing Common mode voltage concerns. In systems where V- is connected to the power supply ground, or to a given voltage, analog common should be connected to V_{IN}-.

FIGURE 8-2: COMMON MODE VOLTAGE REMOVED IN BATTERY OPERATION WITH V_{IN}- = ANALOG COMMON



The analog common pin serves to set the analog section reference or common point. The TC7106A is specifically designed to operate from a battery, or in any measurement system where input signals are not referenced (float), with respect to the TC7106A power source. The analog common potential of V+ – 3.0V gives a 6V end of battery life voltage. The common potential has a 0.001% voltage coefficient and a 15Ω output impedance.

With sufficiently high total supply voltage (V+ – V- > 7.0V), analog common is a very stable potential with excellent temperature stability, typically 20ppm/°C. This potential can be used to generate the reference voltage. An external voltage reference will be unnecessary in most cases because of the 50ppm/°C maximum temperature coefficient. See Internal Voltage Reference discussion.

8.4 TEST (Pin 37)

The TEST pin potential is 5V less than V+. TEST may be used as the negative power supply connection for external CMOS logic. The TEST pin is tied to the internally generated negative logic supply (Internal Logic Ground) through a 500Ω resistor in the TC7106A. The TEST pin load should be no more than 1mA.

If TEST is pulled to V+ all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes with the TC7106A. With TEST = V+, the LCD segments are impressed with a DC voltage which will destroy the LCD.

The TEST pin will sink about 10mA when pulled to V+.

8.5 Internal Voltage Reference

The analog common voltage temperature stability has been significantly improved (Figure 8-3). The “A” version of the industry standard circuits allow users to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed. Figure 8-4 shows analog common supplying the necessary voltage reference for the TC7106A/TC7107A.

FIGURE 8-3: ANALOG COMMON TEMPERATURE COEFFICIENT

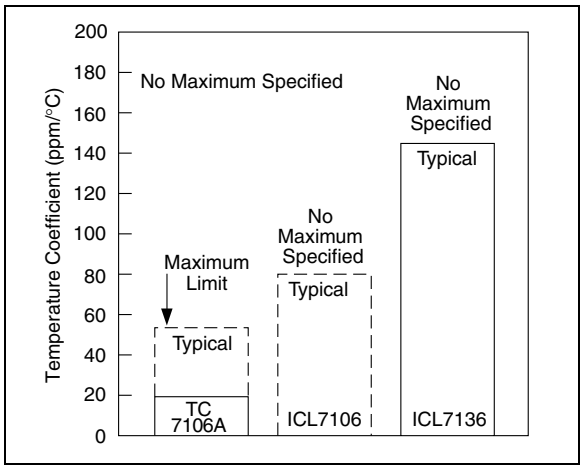
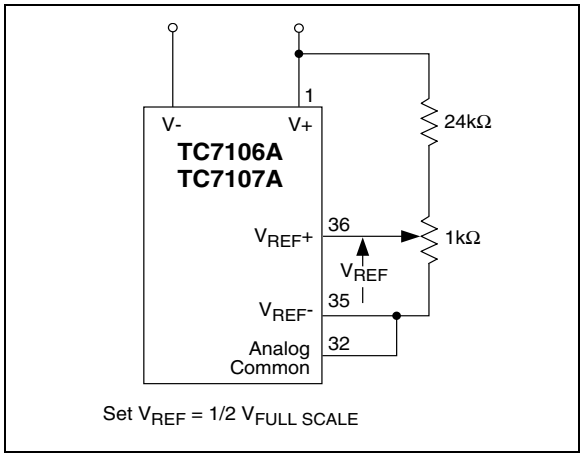


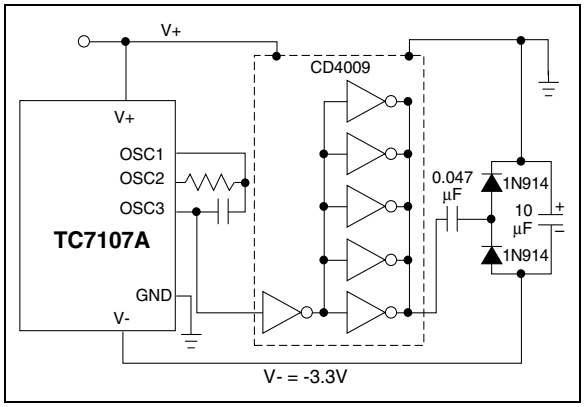
FIGURE 8-4: INTERNAL VOLTAGE REFERENCE CONNECTION



9.0 POWER SUPPLIES

The TC7107A is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors, and an inexpensive IC (Figure 9-1).

FIGURE 9-1: GENERATING NEGATIVE SUPPLY FROM +5V

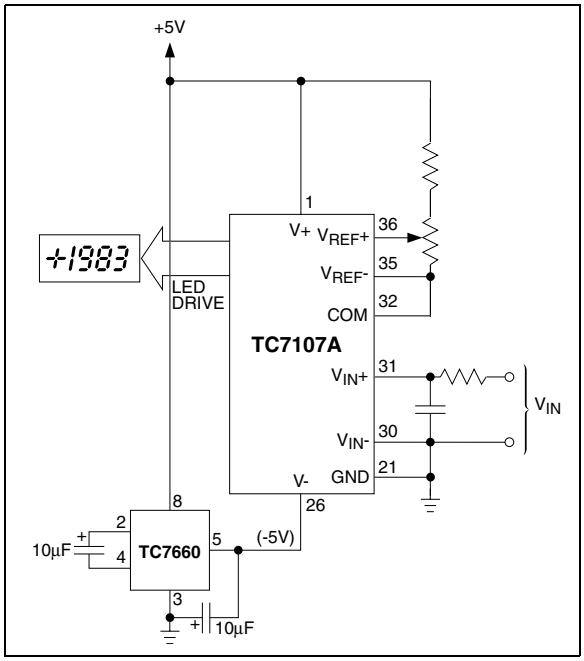


In selected applications a negative supply is not required. The conditions to use a single +5V supply are:

- The input signal can be referenced to the center of the Common mode range of the converter.
- The signal is less than ±1.5V.
- An external reference is used.

The TSC7660 DC to DC converter may be used to generate -5V from +5V (Figure 9-2).

FIGURE 9-2: NEGATIVE POWER SUPPLY GENERATION WITH TC7660

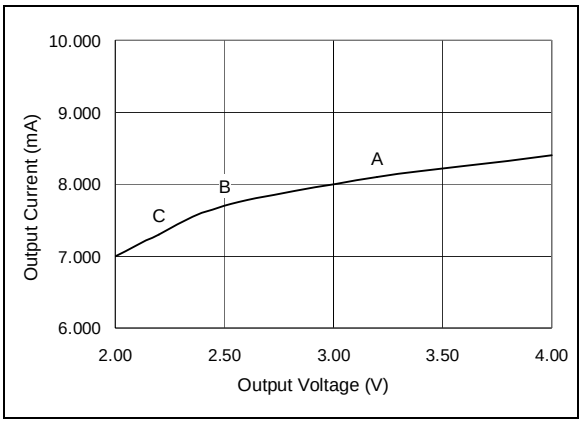


9.1 TC7107 Power Dissipation Reduction

The TC7107A sinks the LED display current and this causes heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing the LED common anode voltage, the TC7107A package power dissipation is reduced.

Figure 9-3 is a curve tracer display showing the relationship between output current and output voltage for a typical TC7107CPL. Since a typical LED has 1.8 volts across it at 7mA, and its common anode is connected to +5V, the TC7107A output is at 3.2V (point A on Figure 9-3). Maximum power dissipation is 8.1mA x 3.2V x 24 segments = 622mW.

FIGURE 9-3: TC7107 OUTPUT CURRENT VS. OUTPUT VOLTAGE



Notice, however, that once the TC7107A output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7V (point B in Figure 9-3) results in 7.7mA of LED current, only a 5 percent reduction. Maximum power dissipation is only 7.7mA x 2.5V x 24 = 462mW, a reduction of 26%. An output voltage reduction of 1 volt (point C) reduces LED current by 10% (7.3mA) but power dissipation by 38% (7.3mA x 2.2V x 24 = 385mW).

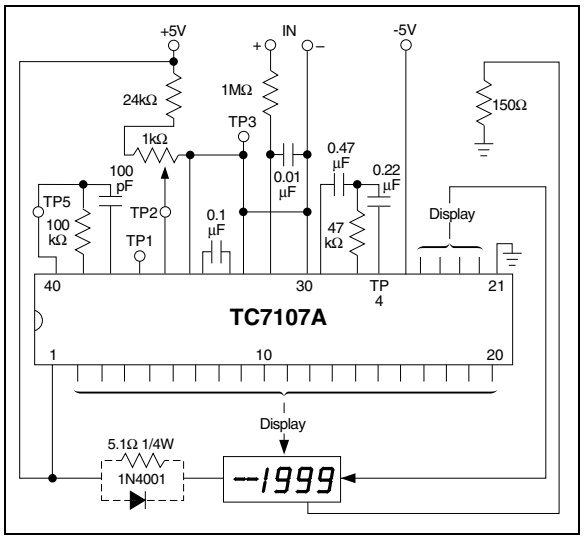
Reduced power dissipation is very easy to obtain. Figure 9-4 shows two ways: either a 5.1 ohm, 1/4 watt resistor or a 1 Amp diode placed in series with the display (but not in series with the TC7107A). The resistor will reduce the TC7107A output voltage, when all 24 segments are “ON,” to point “C” of Figure 9-4. When segments turn off, the output voltage will increase. The diode, on the other hand, will result in a relatively steady output voltage, around point “B.”

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. This effect is caused by the fact that, as fewer segments are “ON,” each “ON” output drops more voltage and current. For the best case of six seg-

ments (a “111” display) to worst case (a “1888” display), the resistor will change about 230mW, while a circuit without the resistor will change about 470mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, a diode may be used instead of the resistor.

FIGURE 9-4: DIODE OR RESISTOR LIMITS PACKAGE POWER DISSIPATION



10.0 TYPICAL APPLICATIONS

10.1 Liquid Crystal Display Sources

Several manufacturers supply standard LCDs to interface with the TC7106A 3-1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Representative Part Numbers*
Crystaloid Electronics	5282 Hudson Dr. Hudson, OH 44236 216-655-2429	C5335, H5535, T5135, SX440
AND	720 Palomar Ave. Sunnyvale, CA 94086 408-523-8200	FE 0201, 0701 FE 0203, 0701 FE 0501
Epson	3415 Kashikawa st. Torrance, CA 90505 213-534-0360	LD-B709BZ LD-H7992AZ
Hamlin, Inc.	612 E. Lake St. Lake Mills, WI 53551 414-648-236100	3902, 3933, 3903

Note: Contact LCD manufacturer for full product listing and specifications.

10.2 Light Emitting Diode Display Sources

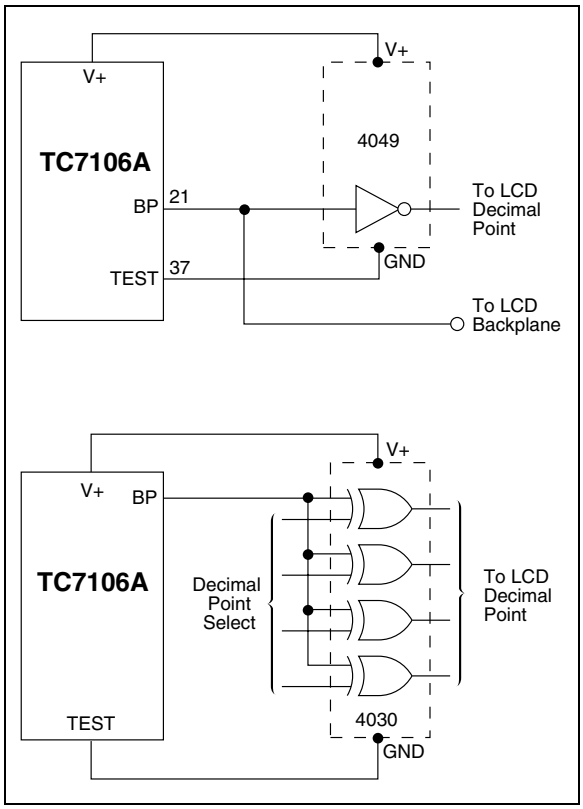
Several LED manufacturers supply seven segment digits with and without decimal point annunciators for the TC7107A.

Manufacturer	Address/Phone	Display
Hewlett-Packard Components	640 Page Mill Rd. Palo Alto, CA 94304	LED
AND	720 Palomar Ave. Sunnyvale, CA 94086 408-523-8200	LED

10.3 Decimal Point and Annunciator Drive

The TEST pin is connected to the internally generated digital logic supply ground through a 500Ω resistor. The TEST pin may be used as the negative supply for external CMOS gate segment drivers. LCD display annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1mA should be supplied by the TEST pin; its potential is approximately 5V below V+ (see Figure 10-1).

FIGURE 10-1: DECIMAL POINT DRIVE USING TEST AS LOGIC GROUND



10.4 Ratiometric Resistance Measurements

The true differential input and differential reference make ratiometric reading possible. Typically in a ratiometric operation, an unknown resistance is measured, with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor is applied to the reference input. If the unknown equals the standard, the display will read 1000.

The displayed reading can be determined from the following expression:

$$\text{Displayed(Reading)} = \frac{\text{RUnknown}}{\text{RStandard}} \text{x} 1000$$

The display will over range for:

$$R_{UNKNOWN} \geq 2 \text{ x } R_{STANDARD}$$

FIGURE 10-2: LOW PARTS COUNT RATIOMETRIC RESISTANCE MEASUREMENT

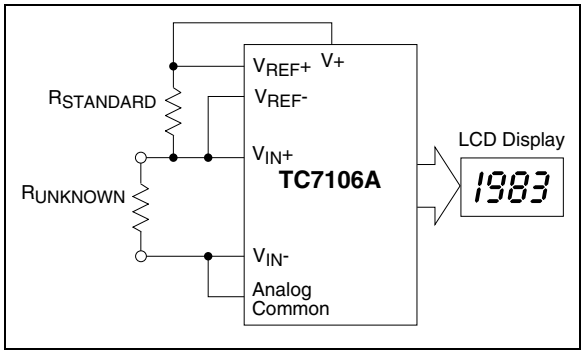


FIGURE 10-3: TEMPERATURE SENSOR

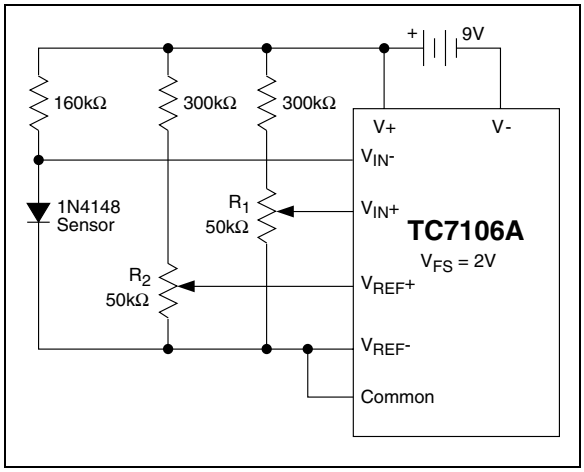


FIGURE 10-4: POSITIVE TEMPERATURE COEFFICIENT RESISTOR TEMPERATURE SENSOR

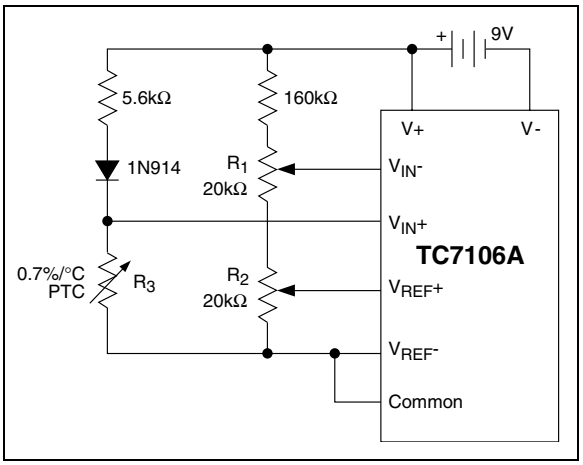


FIGURE 10-5: TC7106A, USING THE INTERNAL REFERENCE: 200mV FULL SCALE, 3 READINGS-PER-SECOND (RPS)

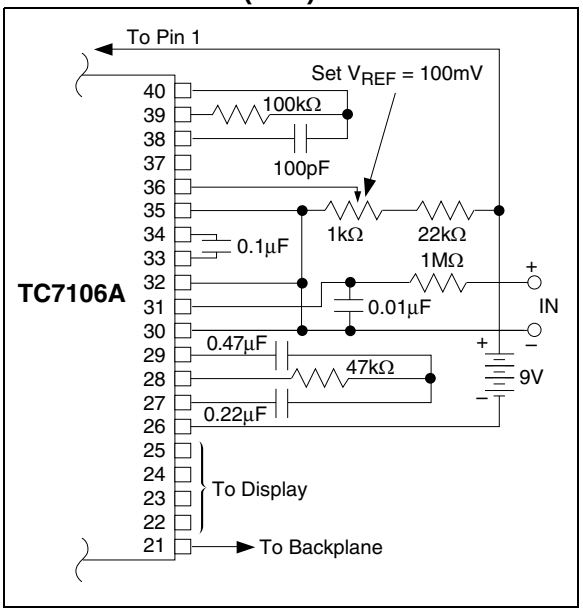


FIGURE 10-6: TC7107 INTERNAL REFERENCE: 200mV FULL SCALE, 3RPS, V_{IN}- TIED TO GND FOR SINGLE ENDED INPUTS

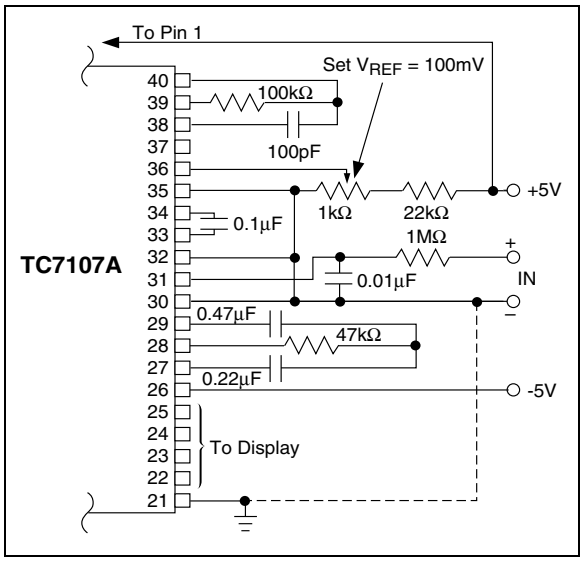


FIGURE 10-7: CIRCUIT FOR DEVELOPING UNDER RANGE AND OVER RANGE SIGNALS FROM TC7106A OUTPUTS

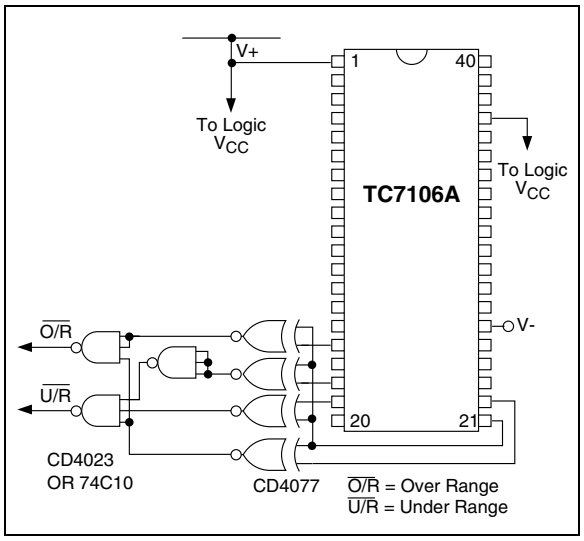


FIGURE 10-8: TC7106/TC7107: RECOMMENDED COMPONENT VALUES FOR 2.00V FULL SCALE

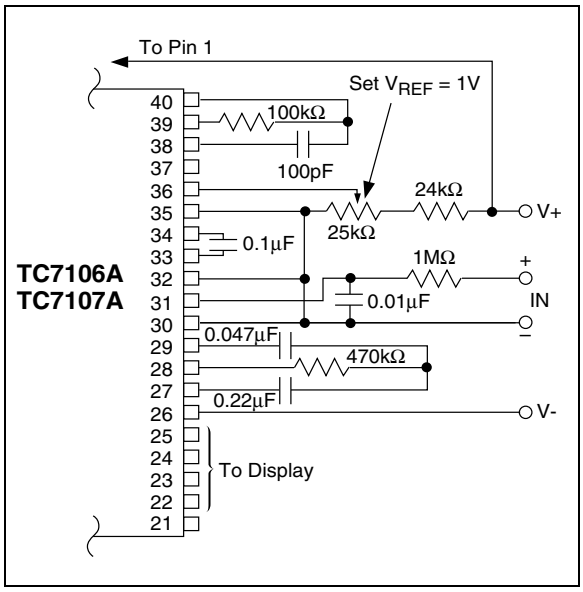
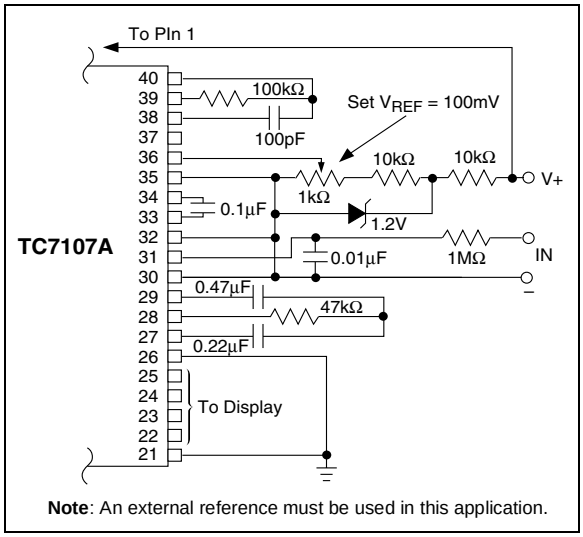


FIGURE 10-9: TC7107 OPERATED FROM SINGLE +5V SUPPLY



Note: An external reference must be used in this application.

FIGURE 10-10: 3-1/2 DIGIT TRUE RMS AC DMM

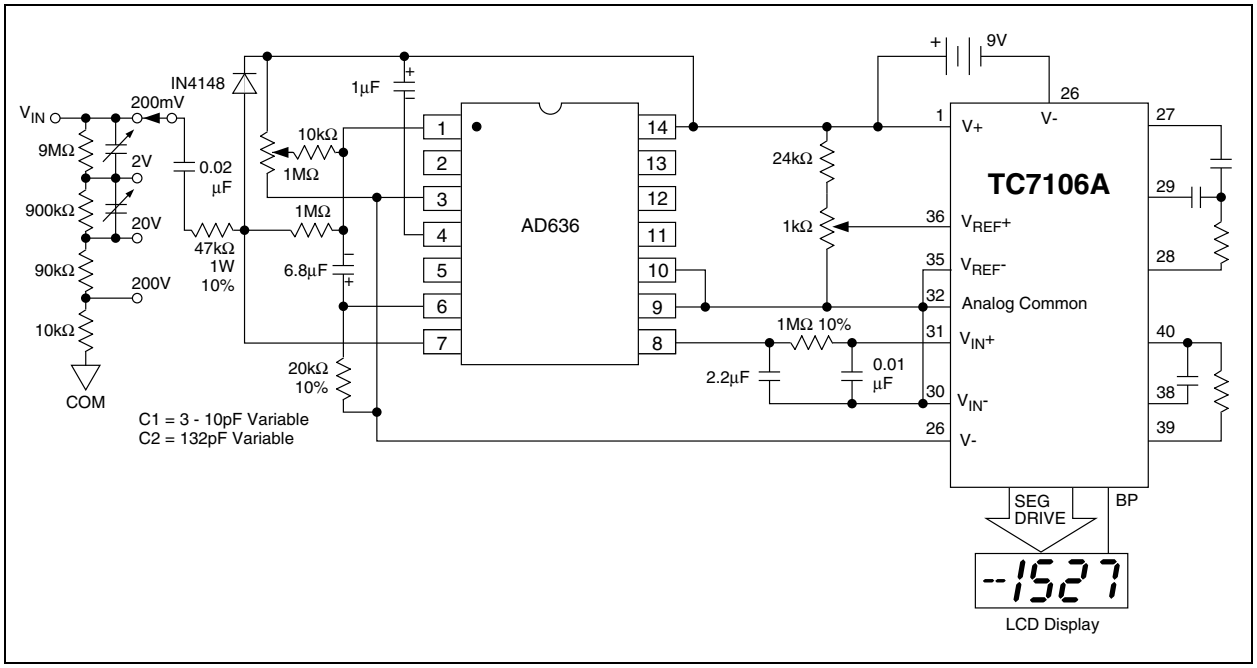
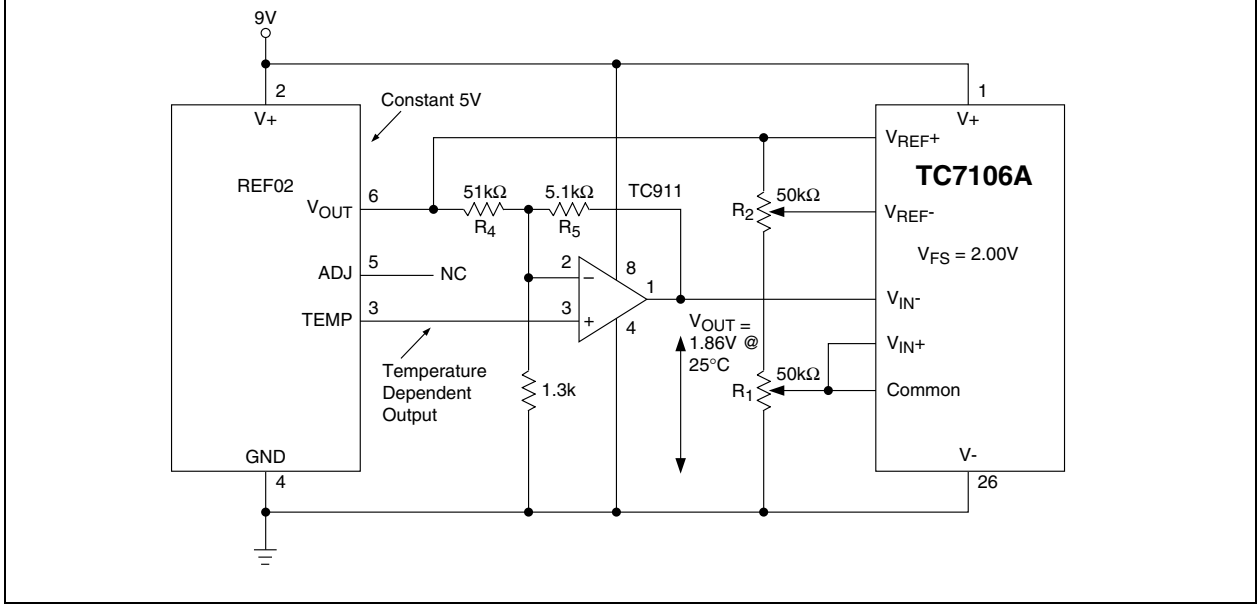


FIGURE 10-11: INTEGRATED CIRCUIT TEMPERATURE SENSOR



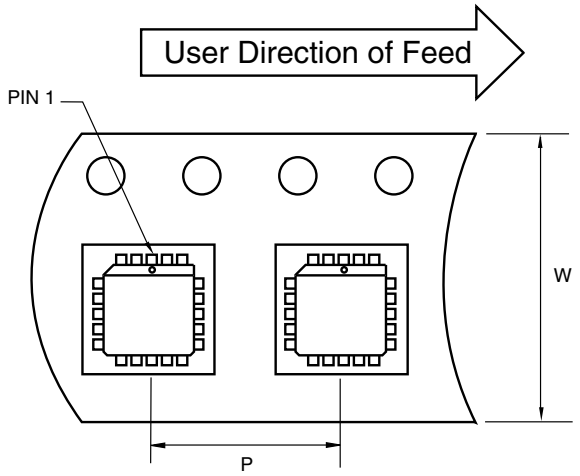
11.0 PACKAGING INFORMATION

11.1 Package Marking Information

Package marking data not available at this time.

11.2 Taping Form

Component Taping Orientation for 44-Pin PLCC Devices



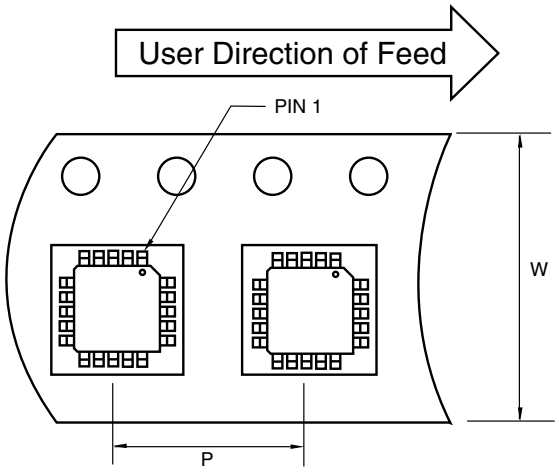
Standard Reel Component Orientation
for TR Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
44-Pin PLCC	32 mm	24 mm	500	13 in

Note: Drawing does not represent total number of pins.

Component Taping Orientation for 44-Pin PQFP Devices



Standard Reel Component Orientation
for TR Suffix Device

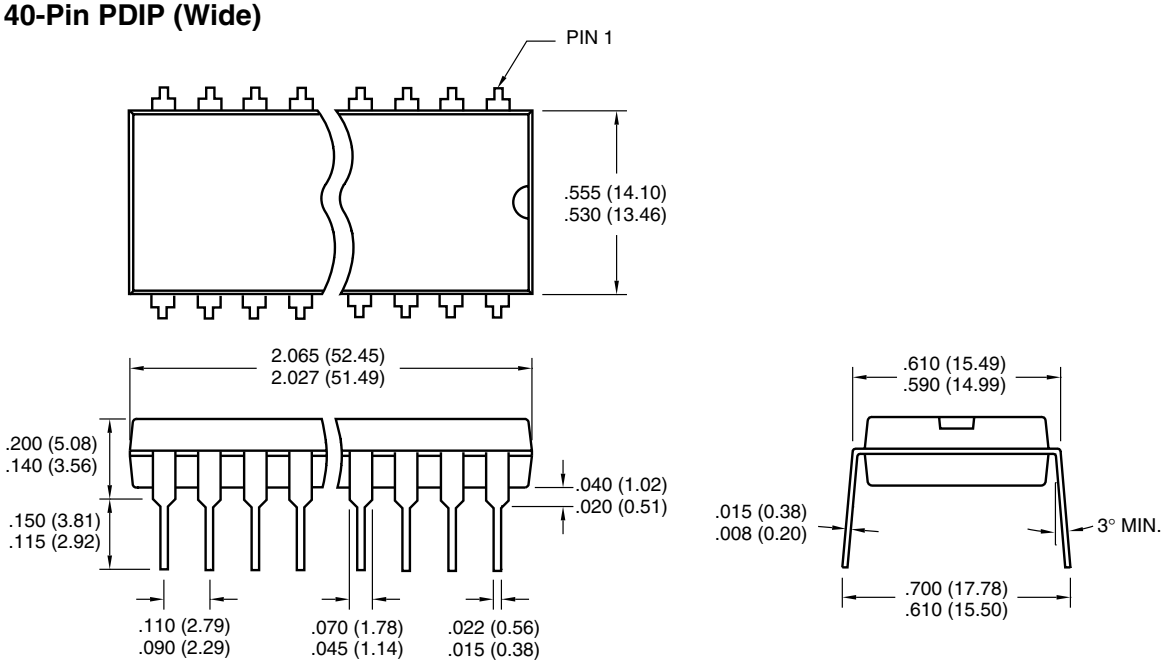
Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
44-Pin PQFP	24 mm	16 mm	500	13 in

Note: Drawing does not represent total number of pins.

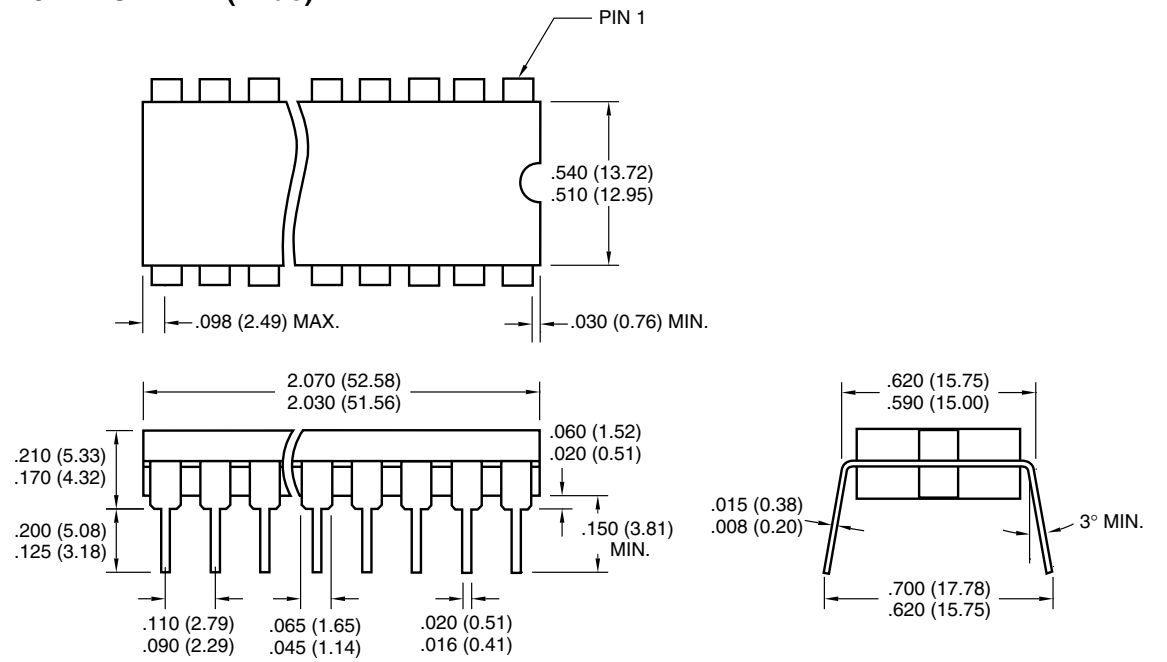
11.3 Package Dimensions

40-Pin PDIP (Wide)



Dimensions: inches (mm)

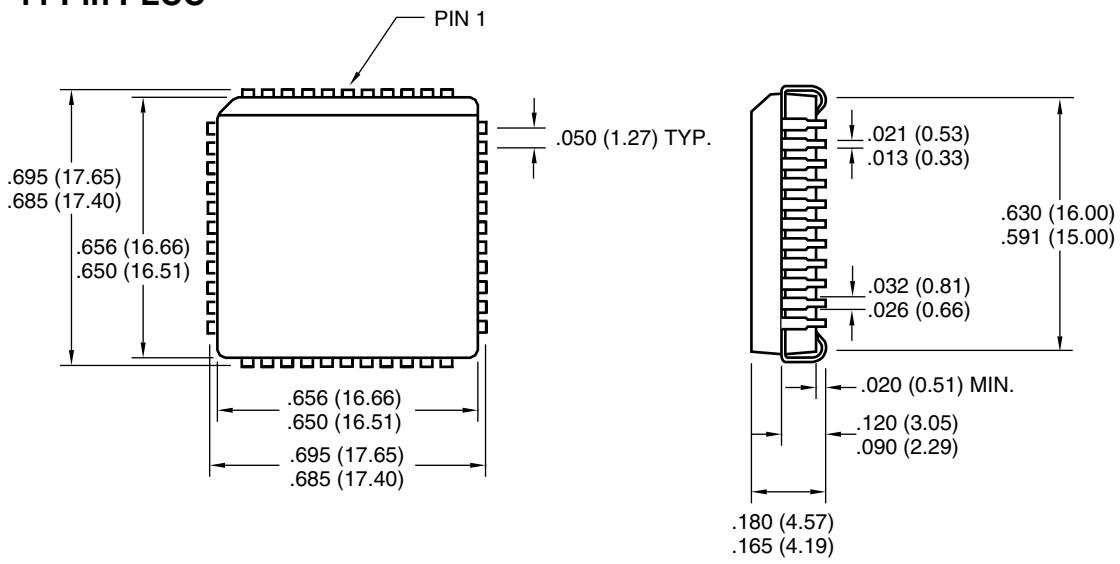
40-Pin CERDIP (Wide)



Dimensions: inches (mm)

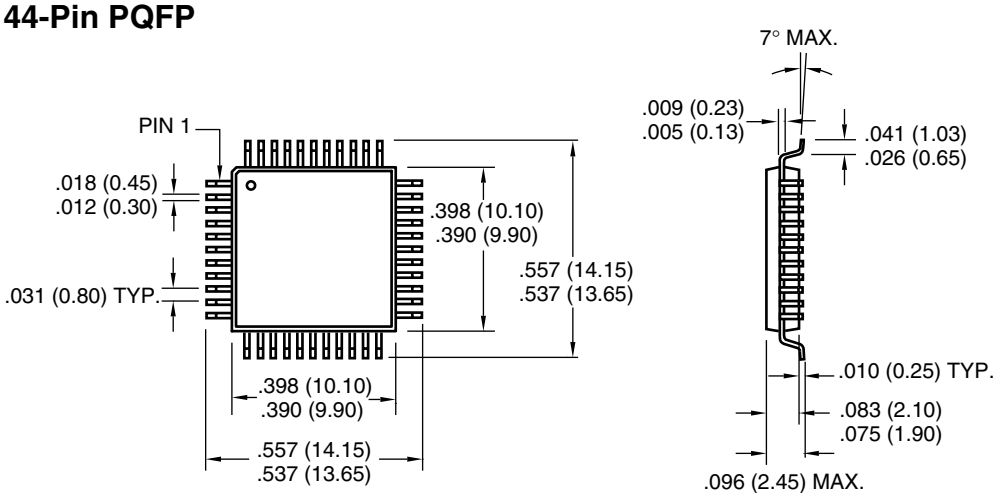
11.3 Package Dimensions (Continued)

44-Pin PLCC



Dimensions: inches (mm)

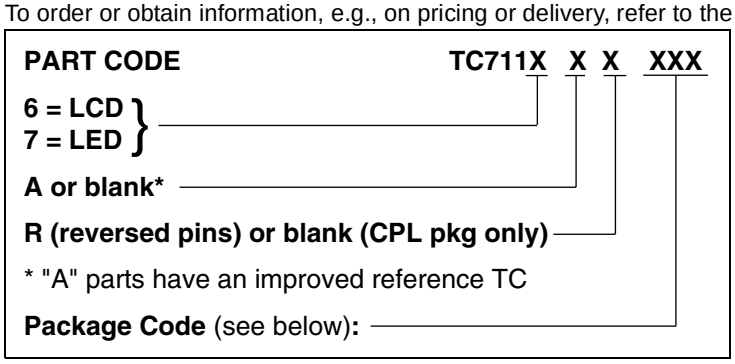
44-Pin PQFP



Dimensions: inches (mm)

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



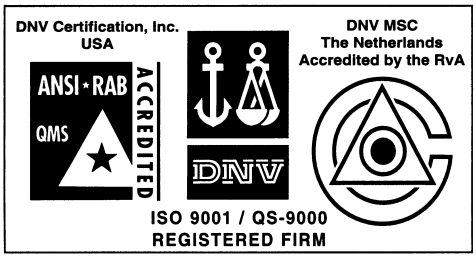
SALES AND SUPPORT

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System
Register on our web site (www.microchip.com/cn) to receive the most current information on our products.



Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Rocky Mountain
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-7456

Atlanta
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Detroit
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Kokomo
2767 S. Albright Road
Kokomo, Indiana 46902
Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia
Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing
Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu
Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-6766200 Fax: 86-28-6766599

China - Fuzhou
Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Shanghai
Microchip Technology Consulting (Shanghai) Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen
Microchip Technology Consulting (Shanghai) Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

Hong Kong
Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India
Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan
Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark
Microchip Technology Nordic ApS
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France
Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy
Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom
Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

03/01/02