2147H
HIGH SPEED 4096 x 1 BIT STATIC RAM

	2147H-1	2147H-2	2147H-3	2147H
Max. Access Time (ns)	35	45	55	70
Max. Active Current (mA)	180	180	180	160
Max. Standby Current (mA)	30	30	30	20

- **Pinout, Function, and Power Compatible to Industry Standard 2147**
- **HMOS* III Technology**
- **Completely Static Memory—No Clock or Timing Strobe Required**
- **Equal Access and Cycle Times**
- **Single +5V Supply**
- **0.8–2.0V Output Timing Reference Levels**
- **Direct Performance Upgrade for 2147**
- **Automatic Power-Down**
- **High Density 18-Pin Package**
- **Available in EXPRESS**
  - **Standard Temperature Range**
  - **Extended Temperature Range**
- **Separate Data Input and Output**
- **High Reliability Plastic or Cerdip**
- **Three-State Output**

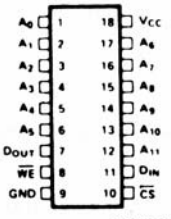
The Intel 2147H is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit using HMOS III, an ultra high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high—deselecting the 2147H—the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are deselected.

The 2147H is assembled in an 18-pin package configured with the industry standard 2147 pinout. It is directly TTL compatible in all respects: inputs, output, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

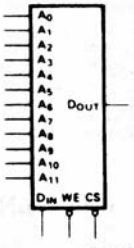
*HMOS is a patent process of Intel.

Pin Configuration



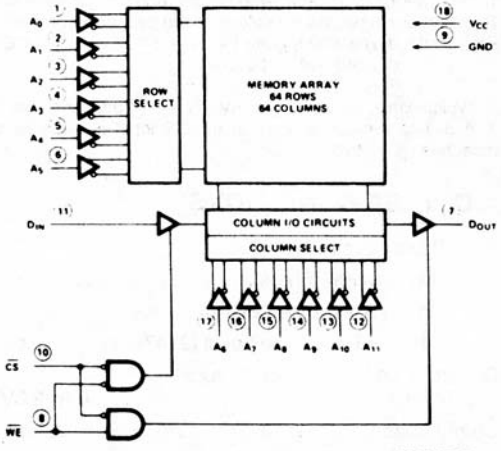
290086-1

Logic Symbol



290086-2

Block Diagram



290086-3

Pin Names

A_0–A_{11}	Address Inputs	V_{CC} Power (+5V)
$\overline{WE}$	Write Enable	GND Ground
$\overline{CS}$	Chip Select	
D_{IN}	Data Input	
D_{OUT}	Data Output	

Truth Table

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to 85°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... −3.5V to +7V
Power Dissipation 1.2W
D.C. Output Current ..... 20 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS(1)

T_A = 0°C to 70°C, V_{CC} = +5V ±10%, unless otherwise noted

Symbol	Parameter	2147H-1, 2, 3			2147H			Unit	Test Conditions	
		Min	Typ	Max	Min	Typ(2)	Max			
I_{LI}	Input Load Current (All Input Pins)		0.01	1.0		0.01	1.0	µA	V_{CC} = Max., V_{IN} = GND to V_{CC}	
$\|I_{LO}\|$	Output Leakage Current		0.1	10		0.1	10	µA	$\overline{CS}$ = V_{IH}, V_{CC} = 5.5V V_{OUT} = GND to 4.5V	
I_{CC}	Operating Current		120	170		100	150	mA	T_A = 25°C	V_{CC} = Max., $\overline{CS}$ = V_{IL}, Outputs Open
				180			160	mA	T_A = 0°C	
I_{SB}	Standby Current		18	30		12	20	mA	V_{CC} = Min. to Max. $\overline{CS}$ = V_{IH}	
I_{PO}(3)	Peak Power-On Current		35	70		25	50	mA	V_{CC} = GND to V_{CC} Min., $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.	
V_{IL}	Input Low Voltage	−3.0		0.8	−3.0		0.8	V		
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V		
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL} = 8 mA	
V_{OH}	Output High Voltage	2.4			2.4			V	I_{OH} = −4.0 mA	

NOTES:
1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute. Typical thermal resistance values of the package at maximum temperatures are:
For Plastic: θ_{JA}(@ 400 f_{PM} Air Flow) = 50°c/w For CERDIP: θ_{JA}(@400 f_{PM} Air Flow) = 40°c/w
θ_{JA}(Still Air) = 80°c/w θ_{JA}(Still Air) = 70°c/w
θ_{JC} = 30°c/w θ_{JC} = 25°c/w
2. Typical limits are at V_{CC} = 5V, T_A = +25°C, and specified loading.
3. A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.

A.C. TEST CONDITIONS

Input Pulse Levels ..... GND to 3.0V
Input Rise and Fall Times ..... 5 ns
Input Timing Reference Levels 1.5V
Output Timing Reference Level (2147H-1) 1.5V
Output Timing Reference Levels (2147H, H-2, H-3) 0.8–2.0V
Output Load ..... See Figure 1

CAPACITANCE(4) T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	6	pF	V_{OUT} = 0V

NOTE:
4. This parameter is sampled and not 100% tested.

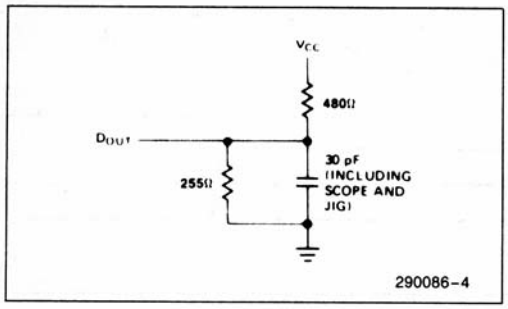


Figure 1. Output Load

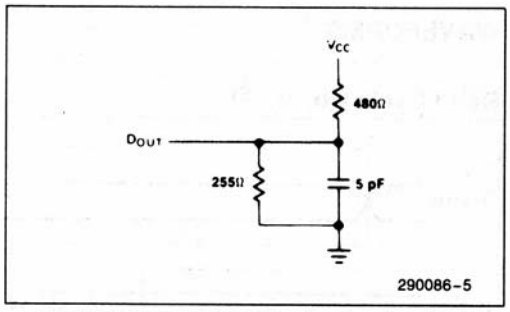


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

A.C. CHARACTERISTICS

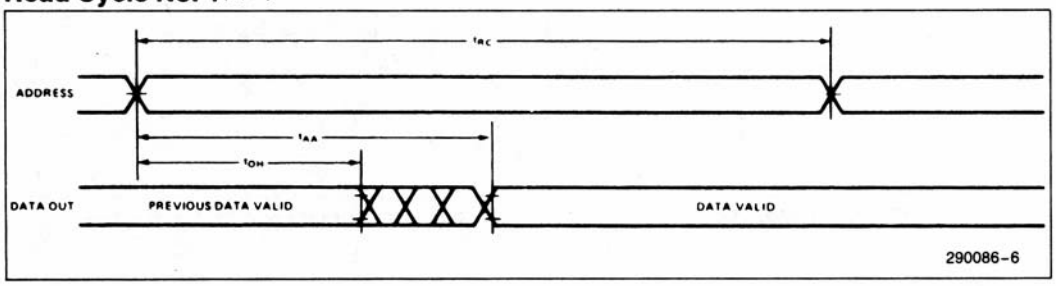
T_A = 0°C to 70°C, V_{CC} = +5V ±10% unless otherwise noted

Read Cycle

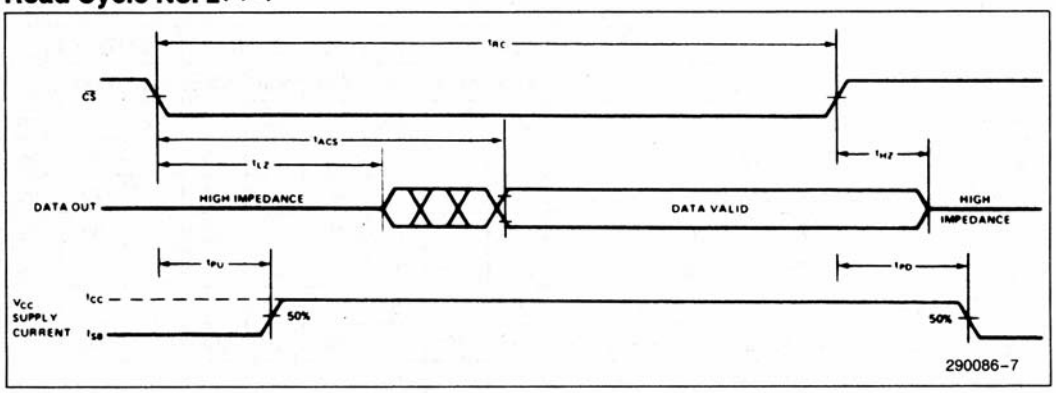
Symbol	Parameter	2147H-1		2147H-2		2147H-3		2147H		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}(1)	Read Cycle Time	35		45		55		70		ns
t_{AA}	Address Access Time		35		45		55		70	ns
t_{ACS1}(8)	Chip Select Access Time		35		45		55		70	ns
t_{ACS2}(9)	Chip Select Access Time		35		45		65		80	ns
t_{OH}	Output Hold from Address Change	5		5		5		5		ns
t_{LZ}(2, 3, 7)	Chip Selection to Output in Low Z	5		5		10		10		ns
t_{HZ}(2, 3, 7)	Chip Deselection to Output in High Z	0	30	0	30	0	30	0	40	ns
t_{PU}	Chip Selection to Power Up Time	0		0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time		20		20		20		30	ns

WAVEFORMS

Read Cycle No. 1[4, 5]



Read Cycle No. 2[4, 6]



NOTES:

1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500 mV from steady state voltage with specified loading in Figure 2.
4. $\overline{WE}$ is high for Read Cycles.
5. Device is continuously selected, $\overline{CS}$ = V_{IL}.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.
8. Chip deselected for greater than 55 ns prior to selection.
9. Chip deselected for a finite time that is less than 55 ns prior to selection. If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle No. 1. Applies to 2147H, 2147H-3.

A.C. CHARACTERISTICS (Continued)

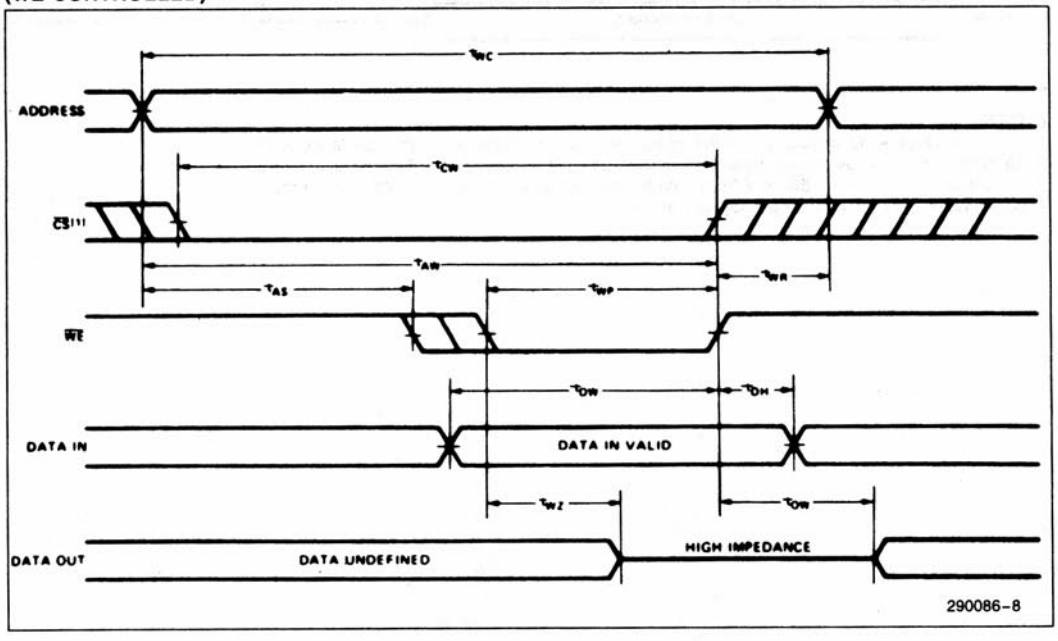
Write Cycle

Symbol	Parameter	2147H-1		2147H-2		2147H-3		2147H		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}[2]	Write Cycle Time	35		45		55		70		ns
t_{CW}	Chip Selection to End of Write	35		45		45		55		ns
t_{AW}	Address Valid to End of Write	35		45		45		55		ns
t_{AS}	Address Setup Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	20		25		25		40		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DW}	Data Valid to End of Write	20		25		25		30		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WZ}[3]	Write Enabled to Output in High Z	0	20	0	25	0	25	0	35	ns
t_{OW}[3]	Output Active from End of Write	0		0		0		0		ns

WAVEFORMS

Write Cycle No. 1

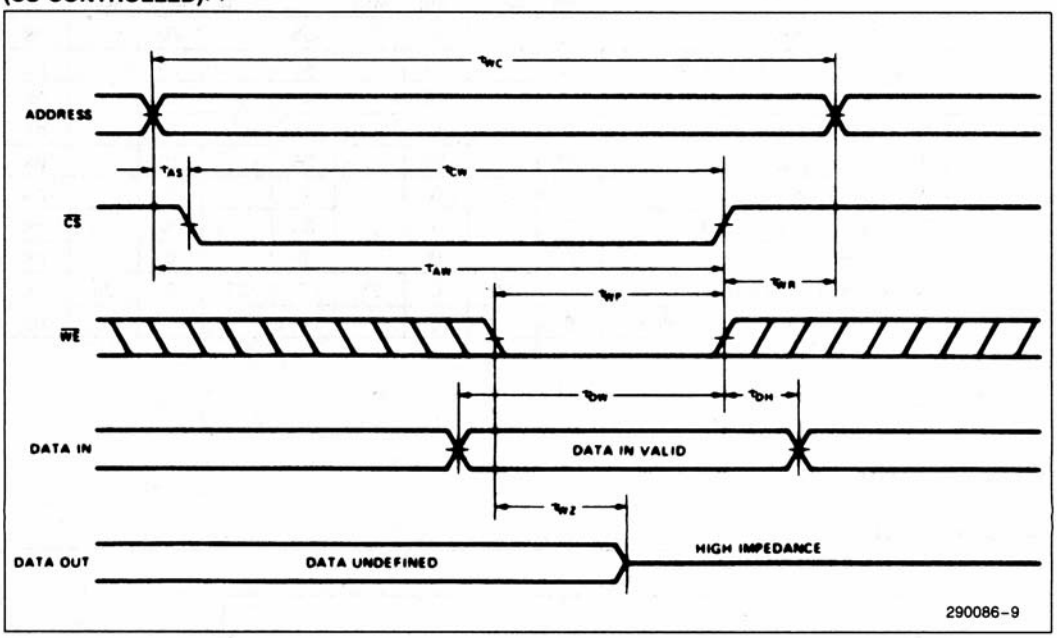
($\overline{WE}$ CONTROLLED)[4]



WAVEFORMS (Continued)

Write Cycle No. 2

($\overline{CS}$ CONTROLLED)(4)



NOTES:
1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady state voltage with specified loading in Figure 2.
4. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.