General Description

Continual advances in digital IC technology are creating stringent demands on EMI/RFI levels in equipment.

EMI/RFI low pass filters are required in personal computers, data terminals, test equipment and process controllers for high frequency suppression into or out of electronic equipment.

Filter Selection and Design Considerations

The "roll-off" frequency fc, defined as the frequency at which the filter passes one-half the power it receives at its input terminal, can be specified from the low megahertz range up to about 100MHz. This frequency, also known as the "-3 dB" frequency, will be determined by the R and C values chosen. Custom resistor and capacitor values are available to optimize system performance.

The specification of these values will depend on constraints relating to noise frequencies, system performance and driver loading. The following procedure is suggested to choose appropriate values of R and C.

The first step is to determine the desired roll-off frequency of the filter, which will lie between the signal frequency and the dominant frequencies of the EMI/RFI noise. By determining the pole of the filter (setting the denominator of the transfer function equal to zero), the roll-off frequency can be expressed in terms of R and C:

$$f_c = \frac{R_S + R_L + 2R}{2\pi C(R + R_S)(R + R_L)}$$

Furthermore, the RC combination must be chosen so that the additional RC time delay will not result in exceeding the sampling window of the receiving IC, due to excessive lengthening of signal rise and fall times.

Rise time from 10% to 90% of the waveform amplitude can be calculated in terms of the circuit's RC time constant using the 1 –exp (–t/RC) relationship for a charging capacitor. At 10%, t_L = 0.1 time constants, and at 90%, t_H = 2.3 time constants. "Time constant" equals $R_{th}C$, where R_{th} is the Thevenin-equivalent resistance as seen by the capacitor.

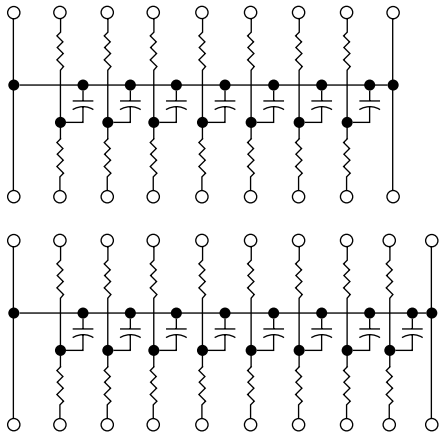
Therefore, equating the difference in the two times to the maximum tolerable rise (or fall) time:

$$t_{max} = t_H - t_L = 2.2R_{th}C$$

$$t_{max} = 2.2\,\frac{(R + R_S)(R + R_L)C}{R_S + R_L + 2R}$$

A final consideration is the insertion loss. As mentioned previously, the voltage drop across the two resistors will attenuate the voltage reaching the load. Normally, logic high and low levels will still be within valid limits. The signal attenuation can be minimized by choosing small R values relative to the load impedance. Typical values for R range from 10 to 50 ohms.

Bourns Low-pass Filters for EMI/RFI Suppression



NO. OF LINES	BOURNS P/N	PACKAGE
7	4118R-601-RC/CC	DIP
8	4120R-601-RC/CC	
8	4420P-601-RC/CC	Wide Body SMD

Standard Resistance/Capacitance Values And Codes

RC	R	CC	C
250	25Ω	500	50pF
270	27Ω	101	100pF
470	47Ω	181	180pF
820	82Ω	201	200pF
101	100Ω		

Reducing EMI/RFI

The radiation of electromagnetic interference and radio frequency interference (EMI/RFI) to the environment is a pressing concern for many manufacturers of electronic equipment. According to FCC regulations (Parts 15 and18), emissions must not exceed certain maximum levels depending on whether the equipment is for strictly industrial use or also for residential use. A graphical representation of these limits is shown in Figure 1. Similar restrictions apply to equipment sold in Europe (VDE 0871, a West German standard), Japan (VCCI), and to the military (MIL-STD-461/462.)

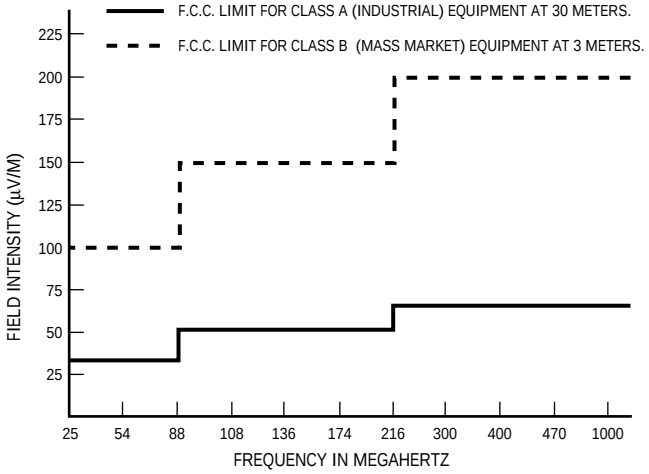


Figure 1.
F.C.C. radiation limits for class A and class B computing devices

Several approaches are available today to control EMI/RFI emissions, including grounded metal enclosures, shielded cables, judicious component placement and interconnect designs, power-supply decoupling, and low-pass filtering of signal lines.

Low-pass filtering can be effective for EMI/RFI filtering when the noise components to be rejected occur at frequencies higher than the signal frequency (to be passed). For these situations, Bourns has developed low-pass resistor-capacitor filter networks which are ideal for board-level EMI/RFI filtering.

A typical application would be to filter signal lines between RS-232 drivers and their corresponding connectors. In such low to medium frequency applications, these networks represent a more useful (and economical) solution than inductive type filters such as ferrite beads. In fact, ferrite beads become mostly ineffective below 10MHz.

The basic “T” configuration (Figure 2) is a standard R-C network available in versions for 7 or 8 input lines. The 8 input-line version is available in both through-hole DIP and surface-mount models.

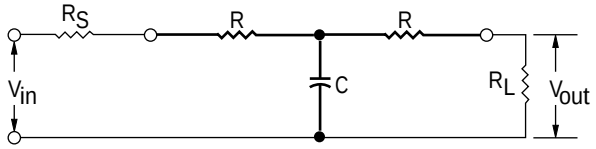


Figure 2.
basic T-Filter configuration

Under steady state conditions, the capacitor C offers an infinite impedance to the DC component of the input waveform (which will be assumed for the moment to be entering from the left side). Thus, the DC component of the signal voltage is passed to the load, but reduced in value by the voltage drop across the two resistors.

The impedance of C becomes lower at higher (noise) frequencies. Thus, the noise component of the signal faces a voltage divider consisting of the first resistor (R) and C. At the high frequencies of the noise component, R will be much greater than the impedance of C, therefore, most of the noise voltage will be dropped across the resistor. Almost no noise current flows through the load and, therefore, will hardly affect the DC voltages (i.e., the signal) across the load.

Since the filter is symmetric, its principle of operation is the same for waveforms traveling in the opposite direction, in which case the voltage divider is formed by the second resistor and the capacitor. Such a symmetrical design is useful for filtering signals on a bidirectional bus.

Assuming purely resistive source and load impedances, the transfer function is given by:

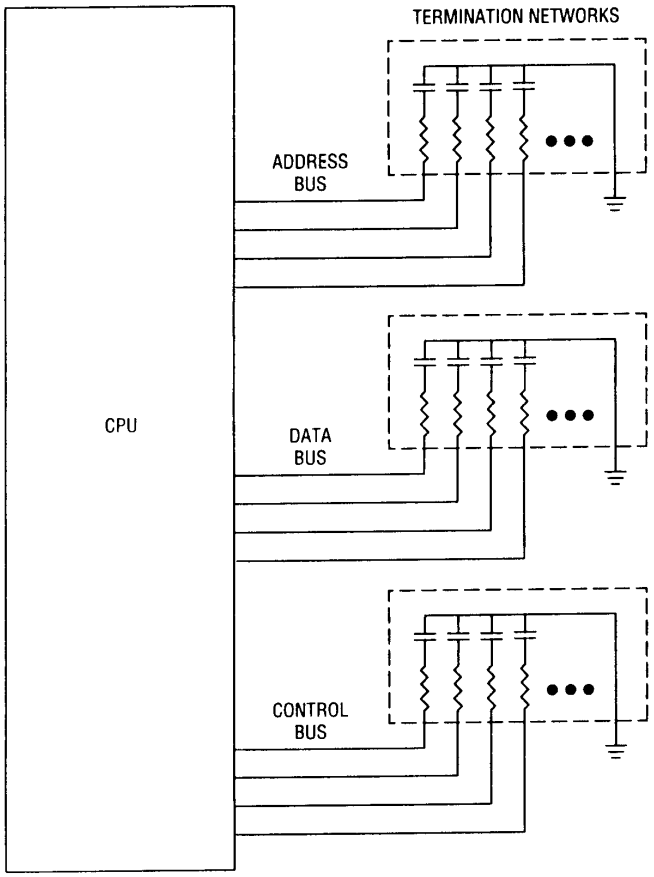
$$\frac{Vout}{Vin} = \frac{R_L}{j\omega C(R + R_S)(R + R_L) + (R_S + R_L + 2R)}$$

FOR PRODUCT SPECIFICATIONS, SEE PAGES 305 AND 306.

General Description

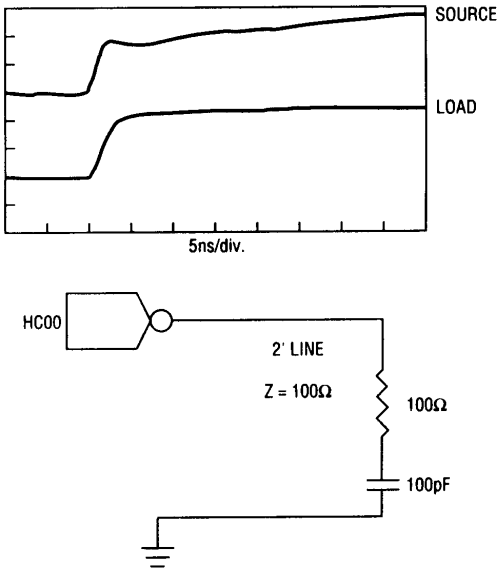
This series of RC Networks is designed to eliminate transmission line effects, such as signal reflections and ringing which influence high speed CMOS. The Networks capacitor blocks DC currents while acting as a short circuit during signal transmitions, thus reducing power consumption. The capacitor also holds the bus at the last logic level to avoid excessive currents.

Block Diagram Of CPU/BUS Configuration



Bus Termination Applications Of Bourns Networks

At high frequencies, the traces on a printed circuit board act as transmission lines—in which impedance mismatches can cause distortion of signals on that line. Terminating the lines with resistor or resistor-capacitor networks provides the means to match impedances and reduce signal distortion.



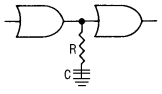
Bus termination (in this case, RC termination technique) considerably reduces overshoots and ringings.

Transmission lines require termination when the time it takes the signal to travel from one end of the line to the other (the propagation delay) amounts to 1/2 or more of the edge rate of the signal (signal rise time or fall time). In other words, termination is required when:

$T_{pd} > (1/2)Te$ T_e = edge rate, T_{pd} = propagation delay

Present high-speed logic families have typical rise times of 2 nanoseconds, while the propagation delay of a common PCB is about 1.77 ns per foot. Applying the above relationship, a transmission line will require termination if it is longer than 7 inches.

High performance systems will commonly need Bourns termination networks for CPU address, data, and control lines. In addition, clock inputs, write and read strobe lines, chip select or output enable lines of high speed devices such as static RAMs, PROMs, and PLDs will also need termination networks.

TERMINATION TECHNIQUE	TYPICAL POWER USAGE	ADDS DELAY	RESISTOR VALUE	CAPACITOR VALUE
RC 	MEDIUM	NO	Z_o	200-500pF

FOR PRODUCT SPECIFICATIONS, SEE PAGES 307 AND 308.

For designers developing high performance systems, exact termination resistances which account for line loading may be desirable. This resistance (or equivalent resistance) can be calculated using the formula:

$$R_{term} = \frac{Z_o}{\sqrt{1 + C_d / C_o}}$$

where Z_o is the characteristic impedance of the line, C_d is the total capacitance associated with the receiving devices (typically 5 pF per input gate) or other loads off the line, and C_o is the intrinsic capacitance of the line.

The series termination technique suppresses reflections at the driving device should any waveforms be reflected back from the driven end of the line. Series termination preserves power since there is no current path to ground or Vcc as in the other methods. However, this technique results in incident signals that transition slowly. It is also not appropriate for distributed loads due to the half-amplitude waveforms which exist at intermediate points along the line.

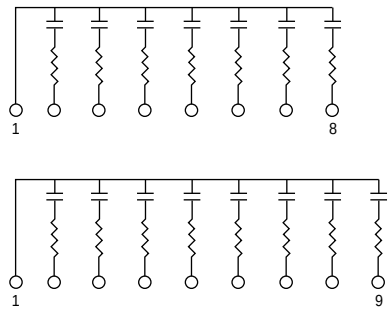
RC termination represents a compromise between power consumption and effect on performance. Its principle of operation is similar to parallel termination, but the capacitor blocks the DC component of the signal, thus reducing power consumption. However, the effectiveness of this method depends on the frequency and duty cycle of the application. RC termination also can be an expensive technique if implemented using discrete components rather than a network.

Typical Usage

While not every address, data and control line may require pull-up/pull-down or termination as part of the system's design, the table below shows common practice for some popular devices.

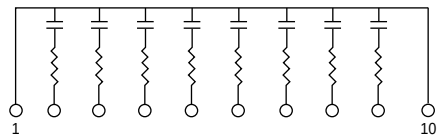
	MICROPROCESSORS				MICRO-CONTROLLERS	
	68000	**68020**	**80286**	**80386**	**68HC11**	**8051**
No. address lines	23	32	24	32		
Termination	0	32	0	32		
No. data lines	16	32	16	32		
Termination	0	32	0	32		
No. control lines	21	27	13	15		
Termination	0	27	0	15		
Total I/O lines	60	91	53	79	38	32
Termination	0	91	0	79	0	0

701



NO. OF LINES	BOURNS P/N	PACKAGE
7	4608H-701-RC/CC	High Profile Conformal SIP
8	4609H-701-RC/CC	
9	4610H-701-RC/CC	

702



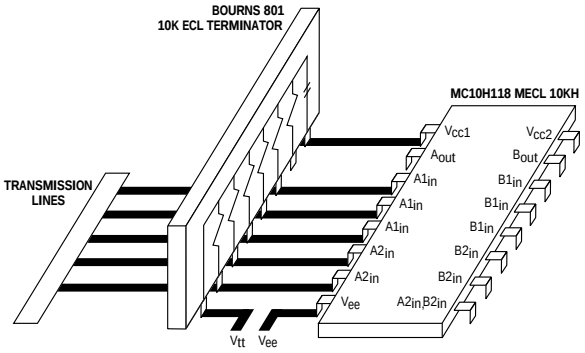
NO. OF LINES	BOURNS P/N	PACKAGE
8	4610H-702-RC/CC	High Profile Conformal SIP

For all RC terminators, standard R values are 50, 68, 75 and 100 ohms. Standard values for C are 47, 100, 500 and 1000pF. See data sheet to select custom combinations of R and C.

REFERENCES:
1. Blood, W.R., MECL System Design Handbook, Motorola, Inc., 1983.
2. F100K ECL Data Book, Fairchild Semiconductor Corp., 1986.
3. MECL Device Data, Motorola, Inc., 1987.

Typical Application

A typical application using a Bourns 801 RC Network in conjunction with a 10K ECL design is shown below. Vee is typically connected to -5.2 volts (10K ECL) or -4.5 volts (100K ECL). V_{cc} is typically connected to GND. V_{tt} is typically connected to -2.0 volts. The 801 network shown below can terminate up to 6 transmission lines and provides a 0.01 μF capacitor to reduce cross talk and feedthrough effects.



Transmission Line Considerations

In high speed circuit applications, the signal propagation delay (T_{pd}) and characteristic impedance (z_o), along a printed circuit board line must be taken into consideration. In general, if the two-way delay along the line is greater than the rise or fall time of the signal, then controlled impedance techniques (i.e., termination) must be utilized to prevent undesirable ringing or over- and undershoots. The delay and impedance can be calculated by knowing the intrinsic inductance (L_o) and capacitance (C_o) of the line:

$$T_{pd} = \sqrt{L_o C_o}$$

$$Z_o = \sqrt{L_o / C_o}$$

The actual, effective delay and impedance due to loading from stubs or additional devices off the line will be:

$$T_{pd}' = T_{pd}\sqrt{1 + C_d/C_o}$$

$$Z_o' = \frac{Z_o}{\sqrt{1 + (C_d/C_o)}}$$

Where C_o = intrinsic capacitance of the line
C_d = capacitance due to loading and stubs off the line
T_{pd} = basic propagation delay of the line
Z_o ....= basic impedance of the line

To formulate a guideline for when line termination is necessary, take the ratio of the rise time or fall time and the two-way delay along the line. The maximum length for unterminated lines will result as follows:

$$L_{max} = \frac{T_r}{2T_{pd}'}$$

Where T_r = rise or fall time
T_{pd} = propagation delay per unit length

The above equation implies that the faster the edge rate or the higher the loading on the line (i.e., higher fanout), the more likely that termination will be necessary for a given line length.

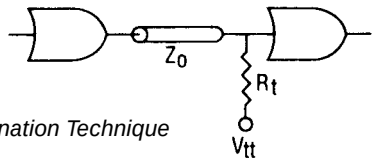
Parallel Termination

For maximum circuit performance or distributed loads, parallel termination is the most appropriate technique. A parallel terminated line uses a resistor connected to -2 volts (ECL application) at the receiving end. The resistor value matches the characteristic impedance of the line (Z_o), thereby producing zero reflection at the receiver. In addition, the terminating resistor also provides output pull down, so a separate pull down resistor at the driving end is unnecessary.

FOR PRODUCT SPECIFICATIONS, SEE PAGES 309 - 311.

Bourns Emitter Coupled Logic Terminator 800 Series

Bourns 801, 802, and 804 conformal coated SIP resistor capacitor networks are designed to terminate 6 transmission lines using the parallel termination technique. A 0.01 µF capacitor(s) is provided in each network to help maintain a solid Vtt level within the package, mitigating any potential cross talk or feedthrough effects. The 804 circuit also contains a 0.1 µF capacitor for bypassing the V_{ee} supply.



Parallel Termination Technique

Thevenin Equivalent Parallel Termination

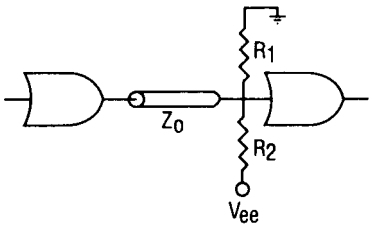
Parallel termination in ECL applications uses -2.0 volts as the terminating voltage. This represents a disadvantage since a separate V_{tt} power supply must be available (V_{ee} = -5.2 volts, V_{tt} = -2.0 volts). For systems in which a separate -2.0 volt supply is not available, the use of a Thevenin equivalent arrangement, although resulting in higher power consumption, provides a convenient solution.

Bourns 803 and 805 conformal coated SIP resistor capacitor networks are designed to terminate 8 transmission lines using the Thevenin equivalent parallel termination technique. Again, a 0.1 µF capacitor is provided to help maintain a solid Vee level within the package, mitigating any potential cross talk or feedthrough effects. The 803 is designed for use with 10K ECL whereas the 805 is designed for use with 100K ECL.

R_1 and R_2 are calculated using the following equations:
$R_2 = (V_{ee}/V_{tt})*Z_o$
$R_1 = (R_2*V_{tt})/(V_{ee}-V_{tt})$

For a 10K ECL supply voltage of -5.2V and V_{tt} of -2V:
$R_2 = 2.6*Z_o$
$R_1 = R_2/1.6$

For a 100K ECL supply voltage of -4.5V and V_{tt} of -2V:
$R_2 = 2.25*Z_o$
$R_1 = R_2/1.25$



Thevenin Equivalent Parallel Termination Technique

References:

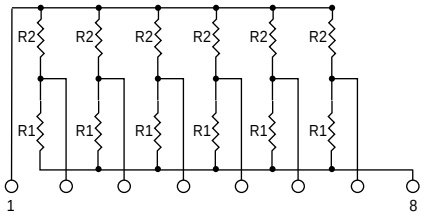
1. Blood, W.R., MECL System Design Handbook, Motorola, Inc., 1983.
2. F100K ECL Data Book, Fairchild Semiconductor Corp., 1986.
3. MECL Device Data, Motorola, Inc., 1987.
4. ECLinPS Data, Motorola, Inc., 1987.

Dual Terminator Resistor Network

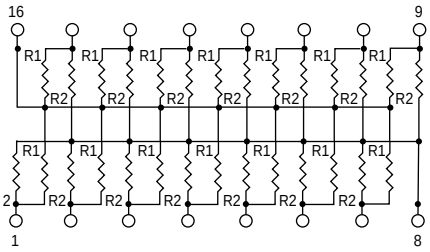
BOURNS®

The Dual Terminator (or Thevenin equivalent) Network is commonly used for TTL dual-line termination and pulse squaring or ECL line terminations. In ECL line terminator, R2 functions as an emitter pull-down resistor and is normally tied to the most negative supply voltage to provide proper line currents. R1 is normally tied to ground and functions as the termination resistor and in parallel with R2 provides the characteristic impedance of the transmission line. This results in a zero reflection coefficient of this line to eliminate reflections.

The Dual Terminator circuit is available in both SIP and DIP configurations, as shown below.



SIP



DIP

Testing of Dual Terminators

Since the Dual Terminator circuit has many resistors in parallel, a direct pin-to-pin measurement for the values of R1 and R2 can be made using an ohmmeter with guard capabilities.

The function of the guard pin is to apply and equal voltage across the adjacent (parallel) resistance path. When applied, current flow is eliminated allowing an accurate measurement of the resistor under test.

Using the 8-pin SIP network shown, the testing method would be as follows:

Test R1 Values

To test the first resistor, connect the ohmmeter measurement leads between pin 8 and 2. Connect the guard lead to pin 1. R1 is now guarded and an accurate measurement can be made.

To test the second R1 resistor, connect the measurement leads between pin 8 and pin 3. Connect the guard to pin 1 and make the resistance measurement.

Continue this testing scheme for the remainder of the R1 resistors, always guarding pin 1.

Test R2 Values

To test the first R2 resistor, connect the ohmmeter measurement leads between pin 1 and pin 2. Connect the guard lead to pin 8. The first R2 resistor is now guarded and an accurate measurement can be made.

To test the second R2 resistor, connect the ohmmeter measurement leads between pin 1 and pin 3. Connect the guard lead to pin 8 and make the resistance measurement.

Continue this testing scheme for the remainder of the R2 resistors, always guarding pin 8.

An example of the type of ohmmeter to be utilized that incorporates a guarded measurement capability. It must be noted that guarded measurements using ohmmeters are satisfactory measurements up to a ratio of about 10:1 between R1 and R2. Above a 10:1 ratio, accuracy is degraded and measurements can be incorrect because of inadequate guarding capability of the equipment.

Unguarded Resistance Measurements

In the case where no guarded ohmmeter is available, the individual resistors can be evaluated by comparing the unguarded resistance measurement to the theoretical value of the equivalent series-parallel circuit and determining the percent of error of each resistor.

Example:

Network 4608X-104-221/331 where R1 values are 220W and R2 values are 330Ω.

Rp = Parallel Resistance of Remaining Circuit (See diagram below.)

RE = Equivalent Series - Parallel Resistance Seen by Unguarded Meter

$$RE_{R1} = (P8\text{-}P2) = \frac{R1\,(R2 + Rp)}{R1 + (R2 + Rp)} = \frac{220\,(330 + 110)}{220 + (330 + 110)} = 146.67\Omega$$

2% Tolerance ≈ ±1.96Ω*

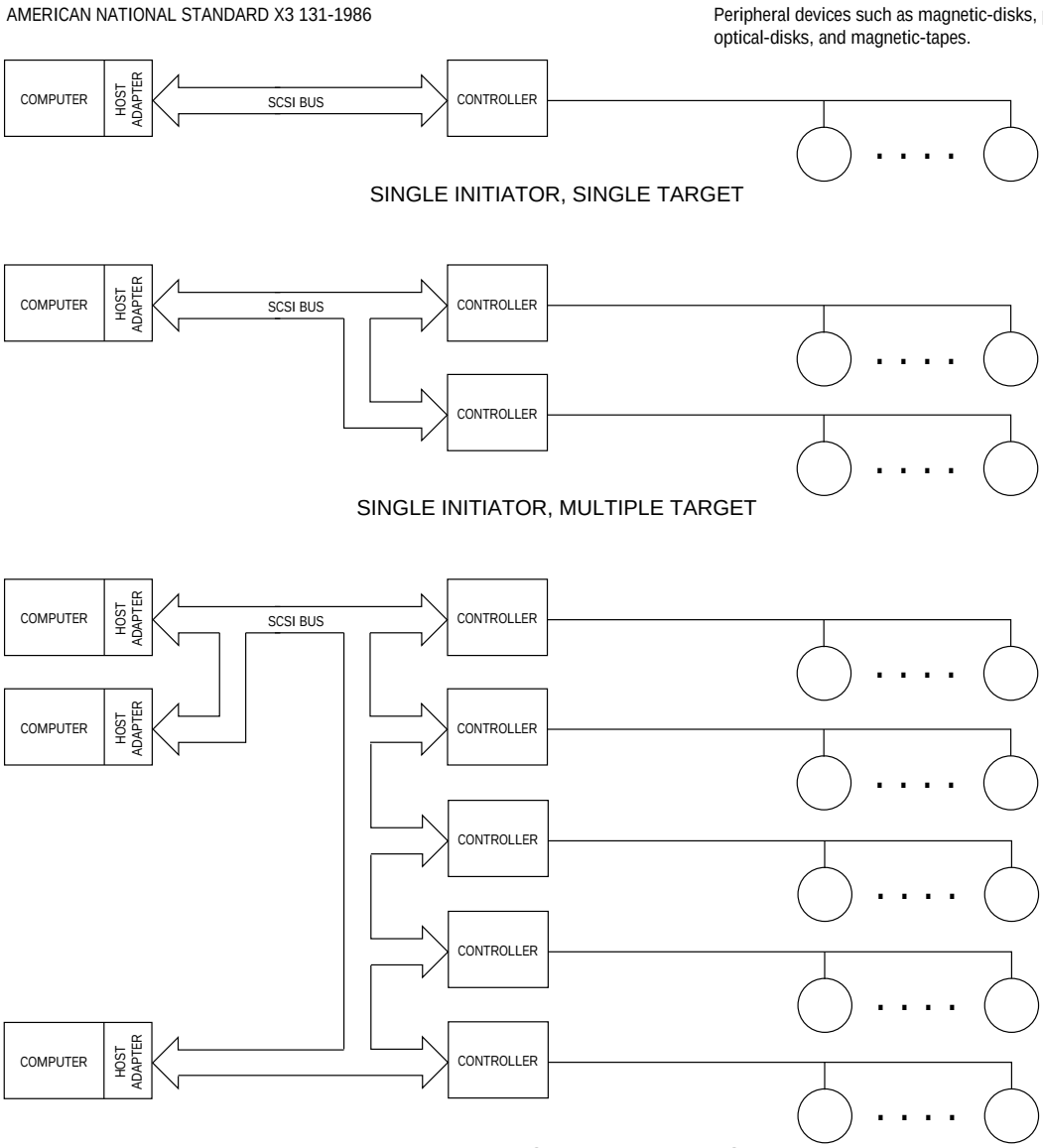
$$RE_{R2} = (P1\text{-}P2) = \frac{R1\,(R2 + Rp)}{R1 + (R2 + RP)} = \frac{3300\,(220 + 110)}{330 + (220 + 110)} = 165\Omega$$

2% Tolerance ≈ ±1.65Ω*

$$Rp = \frac{550}{5} = 110\Omega$$

Utilization of these formulas will enable you to determine the equivalent unguarded resistance to be expected from any values of R1 and R2 for a Dual Terminator Network.

$$*2\%\ \text{tolerance} \approx \frac{(RE_{R1})^2}{R1} \times .02 = 1.96\Omega$$



BLOCK DIAGRAM OF SCSI SYSTEM

Use Bourns Networks to:

- *Provide the terminating resistors required for SCSI implementation.*
- *Optimize signal transmission by eliminating overshoot and ringing.*
- *Minimize space and routing problems, and reduce manufacturing cost per installed resistive function.*
- *Increase board yields and reliability by reducing component count.*

Termination Of The SCSI Bus

The Small Computer System Interface follows American National Standard which provides the mechanical, electrical, and functional requirements for an input/output bus to connect small computers with a variety of peripheral devices. The most common application of this bus is to connect small computers with disk drive (mass storage) units.

The primary resistor network application in SCSI busses is line termination. The termination method is specified in ANSI X3.131-1986 as either a Thevenin equivalent dual terminator

configuration (Fig. 1) for the single-ended implementation of the SCSI bus, or a three-resistor terminator configuration (Fig. 2) for the differential-line version of the SCSI bus.

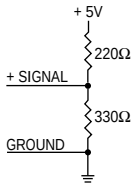


FIGURE 1.

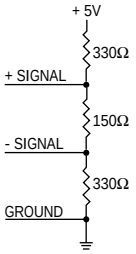


FIGURE 2.

In the single-ended configuration, the SCSI bus is defined for lengths up to 6 meters, while the differential-line version provides for better commonmode noise immunity over cable lengths up to 25 meters.

The signal assignments on the single-ended SCSI bus include 8 data lines, 1 parity line, and 9 control lines. Each of these 18 lines must be terminated, and it is convenient to do this using a resistor network which contains all of the required resistors. An additional 32 lines are ground or power lines which do not require termination (there are 50 lines total in the cable). In a similar fashion, the differential configuration of the SCSI bus uses 18 pairs of lines, each requiring termination.

As of 1989, an extended version of the SCSI standard has been in develop-ment by ANSI, called the SCSI-2 bus. This new standard allows for 16-bit to 32-bit wide data transfers, while also allowing a higher bit transfer rate.

Two cables are defined in the SCSI-2 bus, termed Cable A and Cable B, where Cable B is optional (“wide SCSI” option). Cable A is no different than the single cable used in the original SCSI bus, and therefore uses the same number and types of resistive terminators (i.e., dual terminators for single-ended and triple terminators for differential).

Cable B, however, is a 68-line cable, of which 29 lines (single-ended) or 29 line-pairs (differential) require termination.

Application Guidelines

The principles of transmission-line theory apply to SCSI terminators, and therefore for proper operation their placement must be restricted to the ends of the bus and nowhere else. This implies that the terminators should be placed as close to the SCSI devices as possible. It is permissible to place the terminator inside the SCSI device, but only if that device is located at the end of the bus.

For disk drive applications, SCSI terminators must be present on the host adapter card and at the disk drive end as well. Many disk drive manufacturers have opted to design in removable SCSI terminators into their units to account for the possibility that their unit may not be the one at the end of the cable. For these manufacturers, the combination of a resistor network in a through-hole version plus a matching socket represents the only (and expensive) alternative.

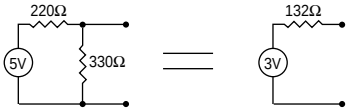
A final consideration is the cable itself. Since the terminators are comprised of 220 ohm and 330 ohm resistors (single-ended), the cable ideally should have a characteristic impedance which matches the Thevenin equivalent of this resistor combination, that is, 132 ohms. In the differential case, a characteristic impedance of 122 ohms would be ideal.

In addition, it is inadvisable to mix different, unmatched cables in the same bus. Such a practice will result in undesirable signal reflections which may compromise the integrity of the data transfer.

Bourns supplies a number of resistor network models designed for both SCSI and SCSI-2 termination .

Cable A (SCSI and SCSI-2) Single-ended

Dual Terminators



PACKAGE	NO. REQ'D.	BOURNS P/N
DIP	1	4120R-3-221/331
CSIP*	2	4611X-104-221/331
CSIP*	3	4608X-104-221/331
MSIP*	3	4308R-104-221/331

Differential:

PACKAGE	NO. REQ'D.	BOURNS P/N
DIP	2	4120R-820-1 4120R-820-2
DIP	3	4116R-8-2
CSIP*	3	4614M-8-2
MSIP	5	4310M-820-2 4120P-830-2 4420P-820-1 4420P-820-2 4420P-830-2

Cable B (SCSI-2 Only) Single-ended

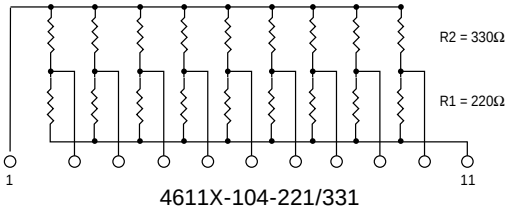
PACKAGE	NO. REQ'D.	BOURNS P/N
DIP	2	4118R-3-221/331
CSIP*	3	4612X-104-221/331
CSIP*	4	4610X-104-221/331
MSIP*	4	4310R-104-221/331

Differential:

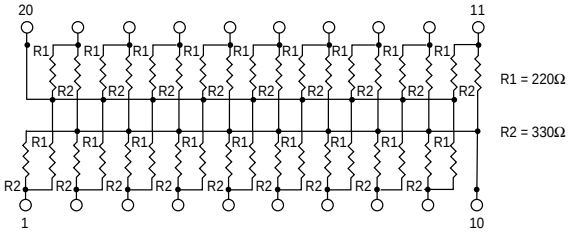
PACKAGE	NO. REQ'D.	BOURNS P/N
DIP	4	4118R-820-2
DIP	5	4116R-8-2
CSIP*	5	4614M-820-2
MSIP*	8	4310M-820-2

*MEDIUM PROFILE (.250” SEATED HEIGHT) AND HIGH PROFILE (.350” SEATED HEIGHT) ARE AVAILABLE BY PLACING THE LETTER “M” OR “H,” RESPECTIVELY, IN THE FIFTH POSITION OF THE PART NUMBER.

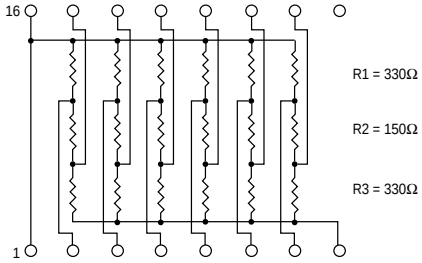
Representative Terminator Schematics



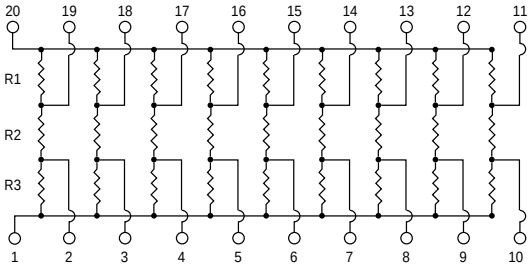
4611X-104-221/331



4120R-3-221/331

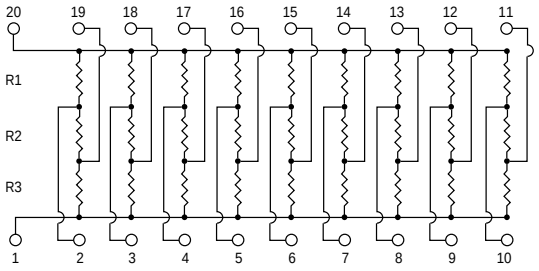


4116R-8-2



820 ELECTRICAL SCHEMATIC

4120R-820-1 4420P-820-1	4120R-820-2 4420P-820-2
R1 = 270Ω	R1 = 330Ω
R2 = 820Ω	R2 = 150Ω
R3 = 180Ω	R3 = 330Ω



830 ELECTRICAL SCHEMATIC

4120R-830-1 4420P-830-1	4120R-830-2 4420P-830-2
R1 = 270Ω	R1 = 330Ω
R2 = 820Ω	R2 = 150Ω
R3 = 180Ω	R3 = 330Ω

Abbreviations

DIP = Dual In-Line Package
MSIP = Molded Single In-Line Package
CSIP = Conformal Coated Single In-Line Package
PCC = Plastic Chip Carrier
SOM = Small Outline Surface Mount Package, Medium Body (.220")
SOL = Small Outline Surface Mount Package, Wide Body (.300")
SON = Small Outline Surface Mount Package, Narrow Body (.154")

References

1. "Small Computer System Interface", (ANSI X3.131-1986), American National Standards Institute Inc., 1986.
2. "Small Computer System Interface 2" (working draft proposal), Revision 5, American National Standards Institute Inc., August 9, 1988.
3. Standard Products Data Book, NCR Corporation, 1988.

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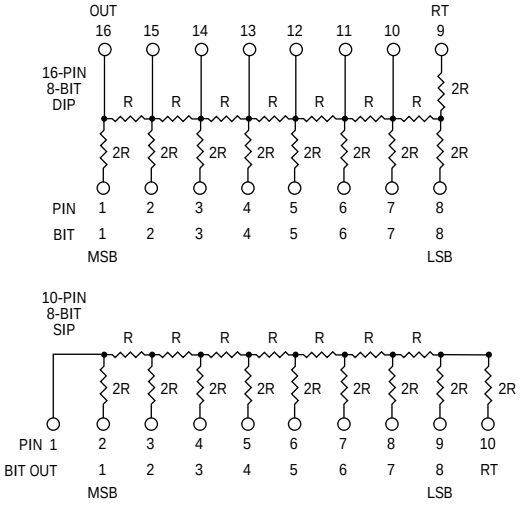
R/2R Ladder Networks

BOURNS®

R/2R Ladder Networks are available in both DIP and SIP (Molded or Conformal) configurations.



The R/2R Ladder Network is commonly used for Digital to Analog (D/A) conversions and Analog to Digital (A/D) conversion by successive approximations. The bits of the ladder are the points at which input signals are presented to the ladder and the output terminal (OUT) is the point at which the output is taken from the R/2R ladder. This terminal (OUT) is commonly used to drive an operational amplifier. R_T (the terminating resistor) is always connected to ground.

Standard R/2R Ladder Networks have a resistance tolerance of ±2.0% (±1.0% available on all but low profile SIPs).

Standard R/2R Ladder Networks

Availability is as follows:

DIP/SMD	SIP-CONFORMAL	SIP MOLDED
14 Pin - 7 Bit	6 Pin - 4 Bit	6 Pin - 4 Bit
16 Pin - 8 Bit	7 Pin - 5 Bit	8 Pin - 6 Bit
	8 Pin - 6 Bit	10 Pin - 8 Bit
	9 Pin - 7 Bit	
	10 Pin - 8 Bit	
	11 Pin - 9 Bit	
	12 Pin -10 Bit	
	14 Pin -12 Bit	

Resistor Power Ratings @ 70˚ C

Low Profile SIP & DIP	.125W
Medium Profile SIP	.170W
High Profile SIP	.200W

How To Order R/2R Ladder Networks

41 16 R - R2R - 503

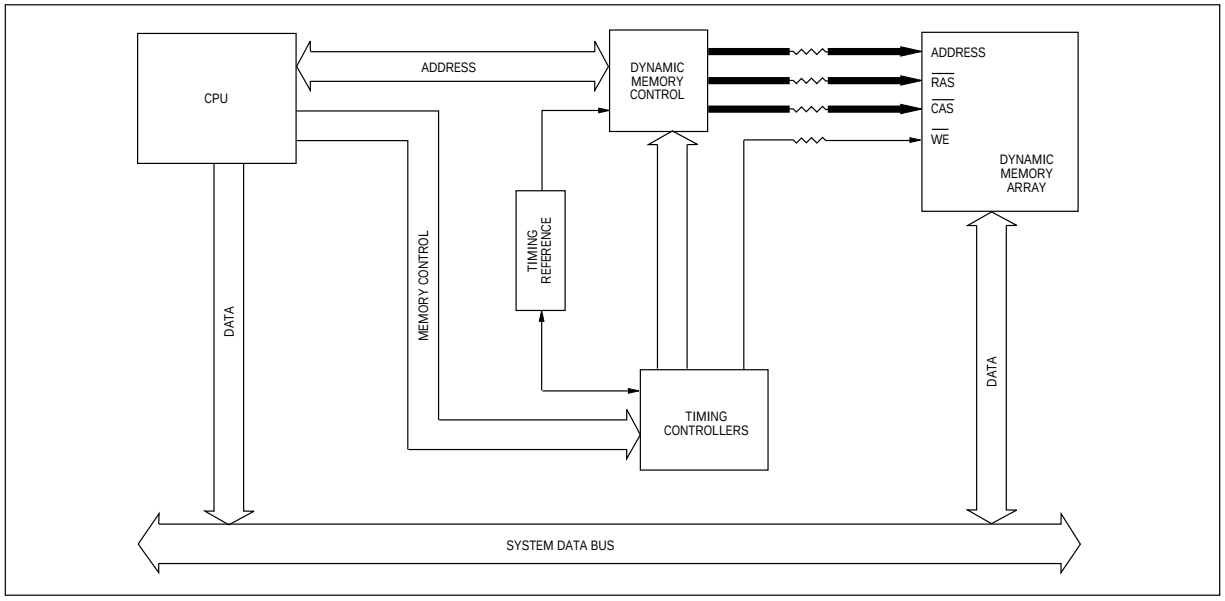
Model
(41 = Molded DIP)
(43 = Molded SIP)
(44 = Wide Body SMD)
(46 = Conformal SIP)
(48 = SMD)

Number of Pins

Physical Configuration
(R = Low Profile - Molded)
(X = Low Profile - Conformal)
(M = Medium Profile)
(H = High Profile)
(P = Medium Body SOIC)

Resistance/Capacitance Code
(For value of R). 2R is double this value.
- First 2 digits are significant.
- Third digit represents the number of zeros to follow.

Electrical Configuration
- R2R = R/2R Ladder Network



BLOCK DIAGRAM OF DRAM SYSTEM

Use Bourns Networks To:

- *Match impedance between memory driver and the DRAM array.*
- *Minimize reflections and ringing in DRAM inputs.*
- *Prevent undershoot of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals which may result in latch-up of DRAM inputs*
- *Improve system performance by allowing faster setting times for DRAM inputs.*

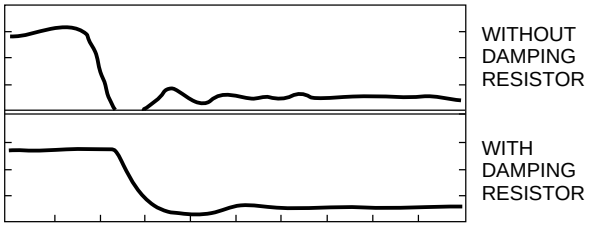
Need For Damping

The address lines ($\overline{RAS}$, $\overline{CAS}$) and control lines ($\overline{WE}$) of dynamic RAM arrays are driven in parallel, causing significant loading on the driver of the DRAM arrays. Each DRAM control input ($\overline{WE}$) has capacitive loading between 5pF to 7pF, while each address line input has about a 10pF load.

Thus each DRAM input can be modeled as a transmission line with distributed inductance and capacitance. If not properly terminated, signal reflections and ringing on the line will result, adversely affecting the performance of the memory system. The effects on signal transitions will be:

1. Increased settling time delay on low-to-high transitions.
2. Voltage undershoot on high-to-low transitions.

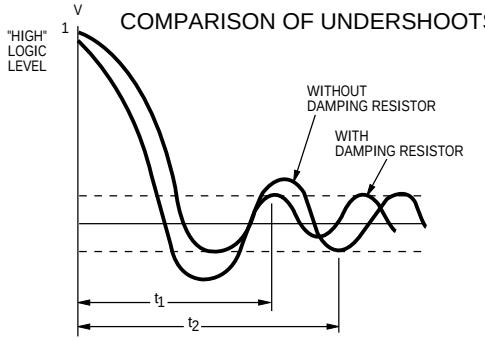
EFFECT OF DAMPING RESISTOR



Courtesy of B. Narasimhan and J. Shaffer, Micron Techology Corporation.

Increased settling time due to ringing reduces system performance because the design has to allow for the settling delay before sampling the signal. Undershoot, by bringing the input voltage below 0 volts, can damage the driver IC as well as alter the DRAM's internal address register contents, causing potential loss of data.

COMPARISON OF UNDERSHOOTS



t_1 - TIME TO ACCEPTABLE "LOW" LOGIC LEVEL FOR DRIVER WITHOUT DAMPING RESISTOR

t_2 - TIME TO ACCEPTABLE "LOW" LOGIC LEVEL WITHDAMPING RESISTOR

Application Guidelines

Termination of address and control lines is typically accomplished with low-valued resistors placed in series at the driver output. Selection of the proper resistance value is performed in two steps: approximation of the proper resistance using transmission line equations, and secondly, through trial and error, changing the resistance value to account for real world deviations such as PCB vias and bends.

The appropriate transmission line equations are as follows:

Z_o = characteristic line impedance (microstrip)

$$= \frac{87}{\sqrt{er + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \text{ ohms}$$

T_d = propagation delay of the line

$$= 1.017 \sqrt{0.475e_r + 0.67} \text{ ns/in.}$$

C_o = trace capacitance = 1000 (T_d/Z_o) pF/in.

C_d = equivalent trace capacitance associated with each DRAM. It takes 0.5 inch to interconnect one DRAM.

$$= 3.5\text{pF}/0.5 \text{ in.} = 7 \text{ pF/in.}$$

Z_o' = effective characteristic impedance, accounting for capacitive loading of the DRAMs.

$$= \frac{Zo}{\sqrt{1 + C_d/C_o}}$$

T_d' = effective propagation delay, accounting for the capacitive loading of the DRAMs

$$T_d = T_d \sqrt{1 + C_d/C_o}$$

where e_r = relative dielectric constant of the PCB's glass epoxy layer

h = distance from the trace to the ground plane

w = width of trace

t = thickness of trace

(Ref. MMI Systems Design Handbook, pp. 10-5 and 10-6.)

For example, for a trace with the following characteristics:

e_r = 5 (for G10 glass epoxy)

h = 30 mils

w = 15 mils

t = 3 mils

then, Z_o = 85 ohms

T_d = 0.15 ns/in.

C_o = 1.76 pF/in.

Z_o' = 38 ohms

T_d' = 0.35 ns/in.

Thus on a theoretical basis, the design will require the resistance of 38 ohms to match the trace impedance of the PCB.

However, the actual impedance will differ from this theoretical value due to the non-ideal characteristics of the PCB trace geometry (i.e., bends, curves and vias in the trace), as well as the manufacturing variations inherent in the components and materials. Therefore, a trial-and-error process must be employed in order to optimize the value of the damping resistor.

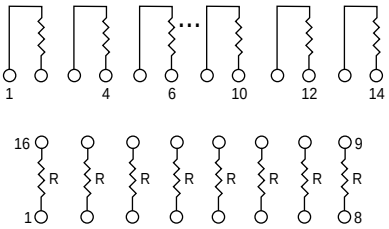
The procedure involves selecting various values around the calculated value and observing the resulting waveforms on an oscilloscope. Choose the value that best balances the reduction in ringing/reflection and the reduction in speed: a large resistance value provides better damping, but will also add delay by slowing the edge rate. Typically, resistance values for memory damping will be in the range of 10 ohms to 50 ohms, with the most common values in the 20 ohm to 30 ohm range.

Since memory damping is a type of series termination, distributed loading along the line will not be possible. That is, the entire lumped load must be located at the end of the line, with no other loads along the signal path. This will guarantee that the waveform will remain undisturbed as it travels along the line. For related reasons, the placement of the series damping resistor should be as close to the driving device as possible.

Bourns Networks For Memory Damping

Bourns can supply a wide range of standard resistor networks for memory damping applications. Standard resistance values (see below) are normally in stock. However, any intermediate value within the range 10 ohms to 10 megohms can be supplied.

The following package and pin count options are available:



NUMBER OF LINES				
	2	**3**	**4**	**5**
MSIP* CSIP* PCC	4304M-102-RC 4604X-102-RC	4306R-102-RC 4606X-102-RC	4308R-102-RC 4608X-102-RC	4310R-102-RC 4610X-102-RC 4210P-102-RC
	6			
MSIP* CSIP* PCC	4612X-102-RC			
	7	**8**	**9**	**10**
DIP CSIP* SOM SOL SOL-J PCC	4114R-1-RC 4614X-102-RC 4814P-1-RC	4116R-1-RC 4816P-1-RC 4416P-1-RC 4416J-1-RC	4118R-1-RC	4120R-1-RC 4420P-1-RC 4420J-1-RC 4420P-102-RC

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Thin film is the preferred generic description for the field of micro-electronics in which conductive, resistive, and/or insulating films are deposited or sputtered on a ceramic or other insulating substrate. The films can be deposited either in a required pattern or as a complete film layer and photoprocessed and etched to form the required pattern.

The term “thin film” is derived from the fact that the deposited films are of the order of a few micrometers in thickness compared with the 10 to 50 micrometers for thick film. Often, thin film conductors are plated to improve conductivity.

Thin Film Applications

Thin film resistor networks typically find application in the analog world. The number one use of thin film is in controlling the gain on operational amplifiers. Some other applications are as a stable reference, stable voltage division, stable feedback loops and analog to digital or digital to analog conversion. These networks may also be used for “wire-OR” pull-up, ECL output pull-down, TTL input pull-down, power down pull-up, open collector pull-up, digital pulse squaring, current summing amplifiers, TTL unused gate pull-up, TTL/MOS interfacing, coding and decoding, and telemetry.

Thin film resistors in a network form offer additional benefits in performance. The resistors in a network are more closely matched in resistance and TCR and actually see reduced differentials of temperature in the end use application. These combine to provide improved tracking in networks. This improved tracking would be an advantage to the instrumentation and industrial control markets.

Potential target markets for thin film include harsh environmental conditions as well as the need for precision resistors. The improved ability to be stable at extended temperatures and the increased ability to handle moist environments are both benefits of the thin film offering. Target applications such as automotive and telecommunications will benefit from these capabilities.

Thin Film Vs. Thick Film

The basic distinction between thick film and thin film is the method of deposition of the metallization. In thick film, specially formulated pastes are applied and fired onto a substrate. The pastes are usually applied with a silk screen method and the substrate is of 96% alumina ceramic. In thin film, a layer of metallization is sputtered onto a substrate and then a pattern is etched into the previously applied metal layer, the substrates are often 99.5% alumina ceramic, silicon, or glass. Thick film is an additive process where layers of termination and resistor material are added to the substrate, while thin film is a subtractive process where the unwanted material is etched away in a succession of selective photoetching processes. The use of photolithographic processes to form thin film patterns produce much finer lines and traces than thick film processes. Thin film is very appropriate for high density and high frequency applications.

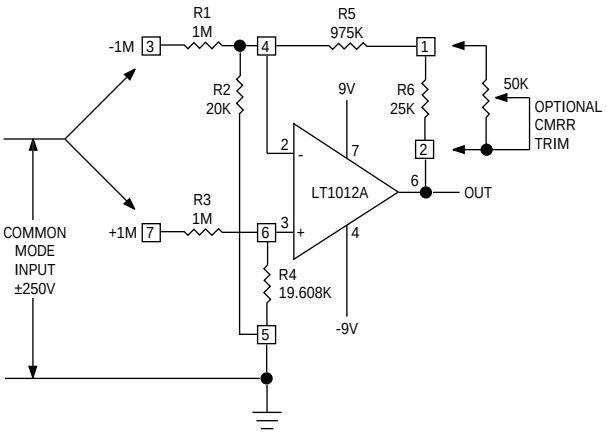
Thick and thin film technologies are well suited for low to medium volume custom circuits. Thick film has the advantages of lower cost (both of tooling up new designs and of production runs), of being able to handle more power, and of being able to service a higher range of ohmic values. Thin film has the advantages of tighter absolute and ratio tolerances and more environmentally stable components with lower noise and tighter TCR than thick film.

Thin film technology is used wherever precision resistors are needed.

Differential Op-amp Input

Differential Op Amps are needed in electrically dirty environments to reject noise transients that are picked up by wires. The differential Op Amps subtracts the noise out of the two signal wires.

Thin film tracking capabilities are needed in these circuits to ensure that the input resistors do not affect the contents of the incoming signal.

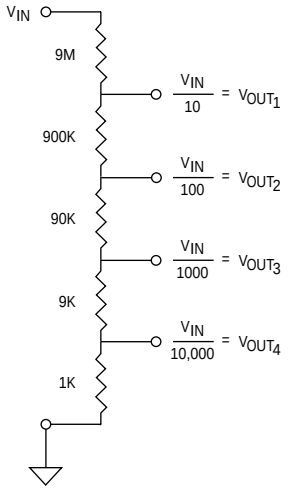


TYPICAL PERFORMANCE:
COMMON MODE REJECTION RATIO = 74dB (RESISTOR LIMITED)
WITH OPTIONAL TRIM = 130dB
OUTPUT OFFSET (TRIMMABLE TO ZERO) = 500µV
OUTPUT OFFSET DRIFT = 10µV/°C
INPUT RESISTANCE = 1M (CM)
2M (DIFF)
BANDWIDTH = 13KHz
BATTERY CURRENT = 370µA

±250V Common Mode Range Instrumentation Amplifier (A_V=1)

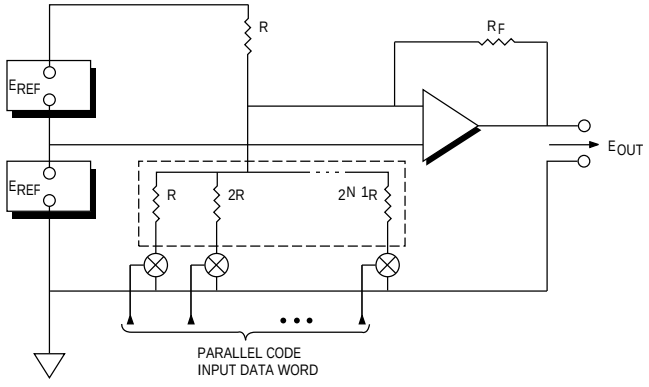
Voltage Divider

Voltage dividers are used to step down voltages for analog processing. Applications are found in multi-meters, oscilloscopes, oscillator stage of voltage control oscillators, etc. The application needs precise resistors to ensure that errors are not added during the conversion process.



Data Conversion

Data converters are used to convert digital data to analog signals or vice versa. The precision of the high bit affects the overall precision of the data convertor. Thus, thick film resistors are used in the lower bits while the thin film or bulk foil resistors are used in the high order bits.



Parallel bit conductance switching D/A converter.

THICK FILM VS. THIN FILM
STANDARD VS. PRECISION

Parameter	Thick Film Circuits	Thin Film Circuits
Resistance	3 Ω to 20MΩ	10Ω to 100KΩ
Resistance Tolerance	.5%, 1%, 2%, 5%	.1%, .2%, .5%
TCR	±100ppm/°C	±25ppm/°C
TCR Tracking	100ppm/°C	5ppm/°C
Operating Temperature	-55°C to +125°C	-55°C to +125°C
Max. Operating Voltage	100 volts	50 volts
Resistor Power	.125W to .5W	.1W to .2W

Soldering And Cleaning Processes

BOURNS®

This application note is designed to provide step-by-step processing recommendations. It covers the popular soldering process currently in use and provides recommendations and cautions for each step. Since many variations of time, temperature, processes, cleaning agents and board types in use, you will want to verify your own system. Bourns does not recommend the backside mounting of passive components.

The process steps, recommendations and cautions are based on Bourns surveys of users, equipment manufacturers and materials suppliers. No warranty expressed or implied is made in regards to the following recommendations.

1 Solder Paste Printing

Reflow; Convection, IR and Vapor Phase

GENERAL

Use the optimum solder paste for the pattern, printing process, and solder joint quality.

RECOMMENDED

Typical solder paste alloy is 63Sn/37Pb. RMA,No-Clean or Halide Free Water Soluble fluxes should be used.

CAUTION

Since solder paste usually contains a high percentage of activators, you must ensure adequate cleaning to remove all residues. Consult your solder paste supplier for cleaning methods. When cleaning additives are needed, only those that are Halide Free should be used.

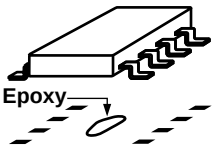
2 Adhesive Application

GENERAL

The adhesive must hold the unit in correct orientation upon placement and maintain the correct position during any physical handling before the final soldering process.

RECOMMENDED

To assure positional stability, place a single dot of epoxy under the unit.



CAUTION

Use sufficient adhesive to assure stability through the cure process.

Avoid overflow of epoxy onto solder pads and terminal areas.

Excessive curing before placement may not allow full seating of the part causing incomplete solder connections.

3 Network Placement

GENERAL

Use pick-and-place equipment with a vacuum nozzle ID that allows adequate suction to pick the unit out of the pocket cavity.

RECOMMENDED

Ensure nozzle inside diameter and vacuum levels are adequate to maintain suction and part alignment.

CAUTION

Ensure parts are placed so that all leads are centered on the solder pads.

Align the leads with the solder belt direction of travel to avoid the part body creating a thermal shadowing effect.

Excessive placement force to the part should be avoided to minimize the risk of package damage.

4 Adhesive Cure

GENERAL

Heat/time cure should be accomplished using either an infrared radiation or a convection oven.

RECOMMENDED

Cure using the temperature profile specified by the adhesive manufacturer.

CAUTION

Use sufficient cure time to ensure complete adhesive transition from fluid to solid.

Care should be taken to assure the placed units are not exposed to temperatures in excess of the manufacturer's maximum.

Do not exceed the maximum temperature rating of the component.

5 Flux Application

Flow (Wave)

GENERAL

Use the correct flux to remove surface oxides, prevent re-oxidation and promote wetting.

RECOMMENDED

RMA (Rosin Mildly Activated) flux or Halide Free Water Soluble flux is recommended.

CAUTION

Avoid fluxes with Halide activators.

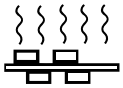
BOURNS®

These are the common methods, materials and maximum temperature/ time parameters for soldering and cleaning processes:

Soldering/Cleaning Methods

Process Step	REFLOW: Hot Air, Infrared (Solvent)	REFLOW: Vapor Phase (Solvent)	FLOW: Wave (Solvent)	FLOW: Wave (Aqueous)	Material
1. Solder Paste Printing	X	X			RMA
2. Adhesive Application			X	X	Epoxy
3. Switch Placement	X	X	X	X	
4. Adhesive Cure			X	X	
5. Flux Application			X		Rosin
5. Flux Application				X	Organic Acid
6. Solder (Reflow)	X	X			63/37 Sn/Pb
7. Solder (Flow)			X	X	63/37 Sn/Pb
8. Wash (Solvent)	X	X	X		ODS Free
9. Wash (Aqueous)				X	DI H_2O; Detergent
High Pressure Fluids				X	
Ultrasonics	X	X	X		
Max. Temp.(°C)/Time (Seconds)	240/30	215/180	260/5	260/5	

6



Solder

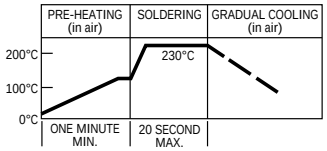
Reflow; Convection, IR and Vapor Phase

GENERAL

Preheat sufficiently using both time and temp. to bring the flux to activation and minimize thermal shock. Consult your solder paste supplier for the recommended profile.

RECOMMENDED

Typical IR/Convection profile.



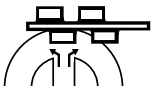
Use convection or Vapor Phase when possible and minimize the time above reflow temperature.

CAUTION

Do not exceed time and temperature reflow profile of 240°C for 30 sec. for Hot Air/IR reflow and 215°C for 3 minutes for vapor phase reflow.

Minimize thermal shock by limiting temperature ramps to 3°C/sec. and by stabilizing board and component temperature during preheating.

7



Solder

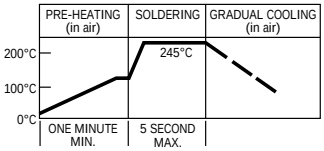
Flow (Wave)

GENERAL

For maximum component reliability and performance, minimize the time of temp. exposure above 200°C.

RECOMMENDED

Typical alloy is Sn63/Pb37. A typical wave solder zone profile is 245˚C for 5 sec.



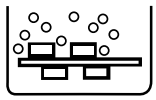
CAUTION

Always preheat before the soldier wave using the temperature for flux activation recommended by the manufacturer.

Do not exceed 240˚C peak temperature for dual wave solder process with a flow zone totaling 5 seconds.

Minimize thermal shock by limiting temperature ramps to 3˚C/sec. and by stabilizing board and component temperature during preheating.

8



Wash

Solvent

GENERAL

Use solvent cleaning primarily for nonpolar contaminants such as rosin based flux residues.

RECOMMENDED

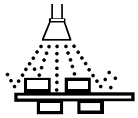
Use any suitable washing solvents that meet ODS requirements.

CAUTION

Limit excessive direct spray pressure to 60 psi.

Allow the assembly to sufficiently cool prior to the washing operation for minimized thermal stress.

9



Wash

Aqueous

GENERAL

Use aqueous cleaning primarily for polar contaminants such as organic flux residues.

RECOMMENDED

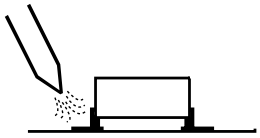
Use De-ionized or Reverse Osmosis water with multistage rinsing. Post bake at 100˚C for 30 minutes to remove any residual moisture.

CAUTION

Limit excessive direct spray pressure to 60 psi.

Allow the assembly to sufficiently cool prior to the washing operation for minimized thermal stress.

Board Rework Technique



GENERAL

Excessive and/or repeated high temperature exposure may affect the component performance and reliability.

RECOMMENDED

Hot air reflow technique is preferred. Use No Clean or Rosin based fluxes only, OA fluxes are recommended.

CAUTION

Avoid the use of wave soldering or soldering irons as a rework technique. Avoid repeated and excessive temperature exposure.