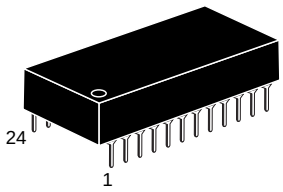
SGS-THOMSON MICROELECTRONICS

M48Z02
M48Z12

CMOS 2K x 8 ZEROPOWER SRAM

DATA BRIEFING

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- UNLIMITED WRITE CYCLES
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z02: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z12: 4.2V ≤ V_{PFD} ≤ 4.5V
- SELF CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 2K x 8 SRAMs



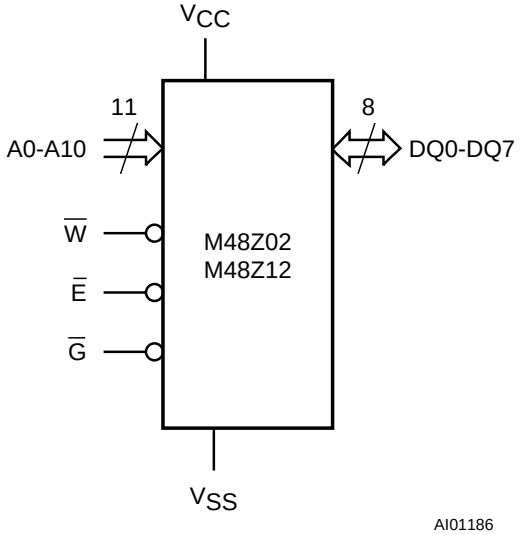
PCDIP24 (PC)
Battery CAPHAT

DESCRIPTION

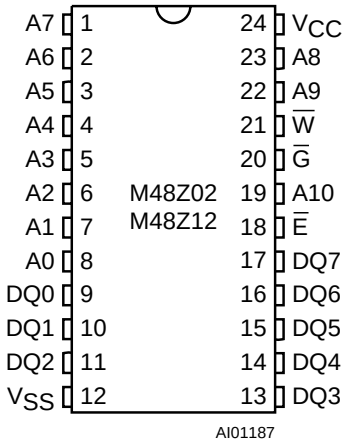
The M48Z02,12 ZEROPOWER® RAM is a 2K x 8 non-volatile static RAM which is pin and function equivalent to any JEDEC standard 2K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed. The M48Z02,12 is compatible with the MK48Z02,12.

A special 24 pin 600mil DIP CAPHAT™ package houses the M48Z02,12 silicon with a long life lithium button cell to form a highly integrated battery backed-up memory solution.

Logic Diagram



DIP Pin Connections



Signal Names

A0-A10	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Ordering Information Scheme

For a list of available options refer to the current Memory Shortform catalogue.
For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

Example: M48Z02 -120 PC 1

Supply Voltage and Write Protect Voltage

02 V_{CC} = 4.75V to 5.5V, V_{PFD} = 4.5V to 4.75V

12 V_{CC} = 4.5V to 5.5V, V_{PFD} = 4.2V to 4.5V

Speed

-120 120ns

-150 150ns

-200 200ns

Package

PC PCDIP24

Temp. Range

1 0 to 70 °C

6 –40 to 85 °C