19-1286; Rev 0; 6/97

MAXIM

MAX5012 Evaluation Kit

Evaluates: MAX5012

General Description

The MAX5012 evaluation kit (EV kit) is intended as a tool for device characterization and for demonstrating the performance of the MAX5012 12-bit, 100Msps, ECL binary digital-to-analog converter (DAC). Data is latched by applying up to a 12-bit ECL binary-data pattern and a clock. Due to the design of the board, the analog-output value is one sample behind the input value. The output voltage (negative-going amplitude) can be seen at the BNC connector OUT+ or at OUT- (inverted).

The evaluation board is designed to cover a wide variety of applications, and can be easily modified to suit a specific application. The following functional blocks are described in detail:

- Power Supplies and Grounding
- Reference Circuits
- Latch and Conversion Clocks
- Digital Input and Controls
- Analog Output

Applications

Engineering Prototype Aid

Incoming Inspection Tool

Guide for PC Board Layout

Guide for Interface Design

Reconstruction DAC

Features

- ♦ **Up to 100Msps Conversion Rate**
- ♦ **Selectable Clock Control for Updating Data**
- ♦ **Reference Voltage: Internal, On-Board, or External**
- ♦ **Selected High-Speed Test Points**
- ♦ **On-Board ECL Latches**
- ♦ **ECL Digital Input Connector**
- ♦ **Fully Assembled and Tested**

Ordering Information

PART	TEMP. RANGE
MAX5012EVKIT	0°C to 70°C

Component List

DESIGNATION	QTY	DESCRIPTION
C1, C2, C3, C4	4	10µF tantalum capacitors
C5, C6, C8, C10, C12, C14–C20	12	0.01µF chip capacitors
C9, C11, C13	3	0.1µF chip capacitors
CR1	1	1.2V reference diode
FB1–FB5	5	Ferrite beads
OUT+, OUT-, CCLK, DCLK	4	BNC connectors
P1	1	Connector
P2	1	Connector
R2	1	6.8kΩ resistor
R3	1	24Ω resistor
R4, R5, R20, R21, R22	5	51Ω, 1/8W, 5% resistors
R6	1	10kΩ, 1/8W, 5% CF resistor

DESIGNATION	QTY	DESCRIPTION
R7	1	1kΩ, 10-turns potentiometer
RN1, RN2, RN7, RN8	4	51Ω resistor networks
RN3–RN6, RN9	5	47Ω resistor networks
S1	1	2X SPDT switch (A0, A1)
U1, U2	2	Flip-flops
U3	1	Multiplexer
U4	1	MAX5012AEPI
N/A	6	Pin sockets
N/A	*	Single-row headers
N/A	4	Spacers
N/A	8	Test-point terminals
N/A	*	#4-40 pan-head screws
N/A	1	28-pin socket

**As required*

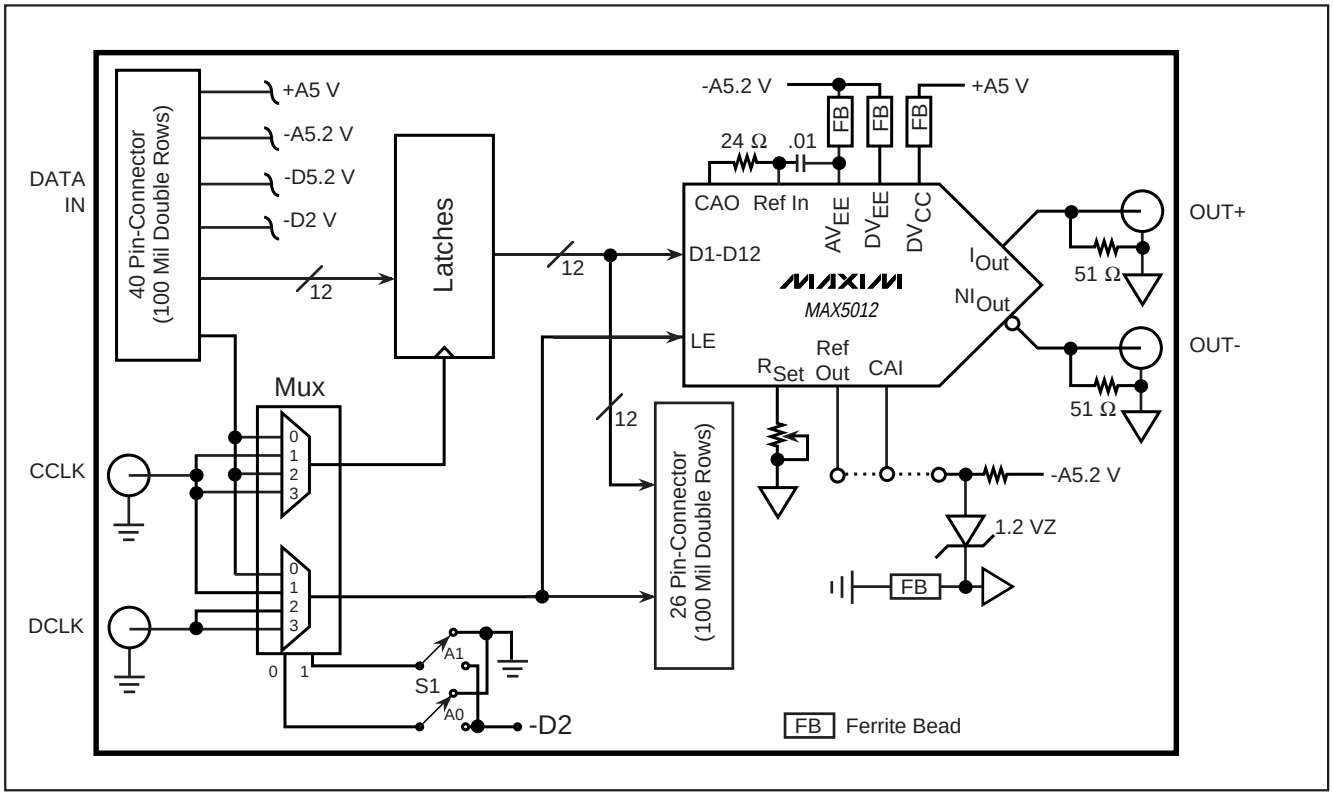


Figure 1. MAX5012 EV Kit Functional Diagram

Detailed Description

Power Supplies and Grounding

The MAX5012 evaluation kit (EV kit) is powered by -5.2V and -2V supplies. An auxiliary +5V supply has been added for prototyping. Power is supplied through the P1 connector or test points. Adequate power-supply decoupling is incorporated into the design; however, use of adequate low-noise, regulated, low-source-impedance supplies is recommended. (Refer to Table 1 for signal and power connections.) Power distribution to the MAX5012 (-5.2V) is filtered to isolate it from the digital switching noise associated with the on-board ECL latches.

Return-power connections and grounding are accomplished with a split ground plane: one for digital return and one for analog return. The two ground planes are coupled together through an inductive ferrite bead (FB1).

Note: The MAX5012 requires only -5.2V to operate.

Reference

Reference-Voltage Source

The MAX5012's control amplifier requires a reference voltage to set the reference current (see the R_{SET} section). This reference voltage can come from one of three different sources:

- Ref Out (pin 20 on the MAX5012). Ref Out is the MAX5012's -1.2V ±50mV internal reference source. To use it, short jumper J3A and open J3B.
- On-board -1.2V reference circuit. This circuit comprises zener diode D1 and resistor R6. To use it, short jumper J3B and open J3A.
- External reference source. Remove both J3 jumpers and apply the external reference-voltage source (between -0.1V and -2V) to the REF test point. A time-varying signal may be used at this REF test point. Refer to the MAX5012 data sheet for the control amplifier's input impedance and bandwidth capabilities.

RSET

The DAC's output current is determined by the resistive circuit formed by R2 and potentiometer R7 connected to the MAX5012's R_{SET} pin. Although this resistance is not directly measurable, it can be determined as a function of the DAC output current:

$I_{OUT} = (V_{REF} / R_{SET})$ x 128 (current out is a constant 128 times the reference current)

The output compliance voltage is not compromised if the board is set as in the *Standard Initial Setup and Operational Check* section.

Control-Amplifier Output

The MAX5012's control-amplifier output (CAO) biases the internal current sources. In the MAX5012 EV kit layout, the CAO is fed back into the reference input. **Note:** This signal must be decoupled to the DAC's analog V_{EE} supply.

Clock

The MAX5012 EV kit requires an external clock signal to initiate input data prelatching and MAX5012 data conversion. A single clock can be used for both data prelatching and MAX5012 conversion, or an additional decimation clock can be used to reduce the MAX5012's data-update rate. For proper operation, the external clock signals and the input data word must be within standard ECL signal levels. (Refer to Figure 2 for the clock's timing requirements.)

The U3 multiplexer (mux) controls clock-signal routing from the input connectors (P1, CCLK, DCLK) to the data latches (U1, U2) and the MAX5012 (U4). Toggle-switch S1 provides manual control of the mux's address lines A0 and A1.

Clock signals can be monitored at test points CCLK1–CCLK4 (refer to Figure 3 for test-point locations).

Single-Clock Configuration

Apply the external-clock signal to either connector P1 (pin 1) or the BNC labeled CCLK. Configure single-clock mode using toggle switch S1 (A0, A1) (refer to Table 2 for proper settings).

Dual-Clock Configuration

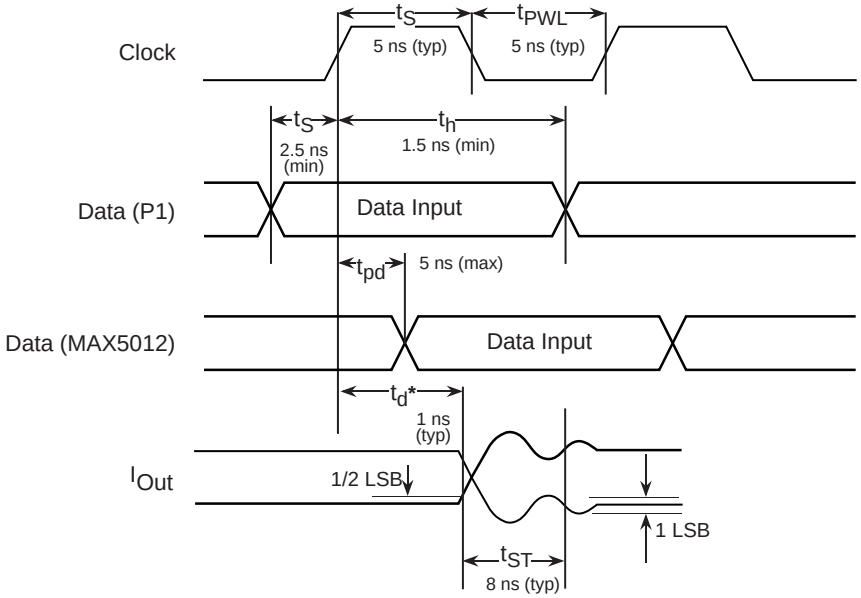
Apply the external-clock signal for data prelatching to either connector P1 (pin 1) or the BNC labeled CCLK. Apply a second decimation-clock signal to the BNC labeled DCLK. Configure dual-clock mode using toggle switch S1 (A0, A1) (refer to Table 2 for proper settings).

Table 1. Connector P1 Pinout

PIN	DESCRIPTION	PIN	DESCRIPTION
1	Data Latch CLK	21	Data Bit 2
2	Digital Ground	22	Digital Ground
3	Data Bit 11 (MSB)	23	Data Bit 1
4	Digital Ground	24	Digital Ground
5	Data Bit 10	25	Data Bit 0 (LSB)
6	Digital Ground	26	Digital Ground
7	Data Bit 9	27	Digital Ground
8	Digital Ground	28	Digital Ground
9	Data Bit 8	29	-5.2V (digital)
10	Digital Ground	30	Digital Ground
11	Data Bit 7	31	-2V (digital)
12	Digital Ground	32	Digital Ground
13	Data Bit 6	33	-5.2V (analog)
14	Digital Ground	34	Analog Ground
15	Data Bit 5	35	-5.2V (analog)
16	Digital Ground	36	Analog Ground
17	Data Bit 4	37	+5V (analog)
18	Digital Ground	38	Analog Ground
19	Data Bit 3	39	+5V (analog)
20	Digital Ground	40	Analog Ground

Table 2. Clock Configuration

S1 SETTING		CLOCK SOURCE		CLOCK MODE
A1	A0	DATA PRELATCH CLOCK	MAX5012 CONVERSION CLOCK	
0	0	P1 (connector)	P1 (connector)	Single
0	1	CCLK (BNC)	CCLK (BNC)	Single
1	0	P1 (connector)	DCLK (BNC)	Dual
1	1	CCLK (BNC)	DCLK (BNC)	Dual



Notes: Diagram assumes the use of a single clock for the data latches and the MAX5012.

Timing is measured from 50% levels.

*t_d does not take into account skew between output gates.

t_{ST} is measured as a voltage settling at midscale transition to 0.024% into R_L = 50Ω.

Figure 2. Timing Diagram

Analog Output

The MAX5012 output comprises complementary current sinks (I_{OUT}, NI_{OUT}). Being terminated to ground through a 51Ω resistor develops an associated voltage dependent on the R_{SET} value previously discussed. When V_{REF} and R_{SET} are set at their nominal levels:

Given: V_{REF} = -1.2V
R_{SET} = 7.5kΩ
$I_{OUT}(FS)$ = (-1.2V / 7.5kΩ) x 128 = -20.48mA

Then: $V_{OUT} = R_{LOAD} \times I_{OUT}(FS)$
= 51Ω x -20.48mA
= -1.044V
(near the -1.2V minimum compliance voltage)

The user can modify the MAX5012 output load to incorporate a wide variety of signal levels; however, equivalently loading the outputs results in superior operational performance. In any design, both current and voltage specifications must be maintained on the output of this device.

Layout

Careful consideration was given to the layout of this evaluation board to ensure maximum performance for the MAX5012 and to help users develop similar design and layout aspects for their own designs. Some of the highlights of this design are as follows:

- The ground planes are split into an analog plane and a digital plane. They are tied together at only one point (through ferrite bead FB1).
- This evaluation board provides both low- and high-frequency-bypass, power-supply-decoupling capacitors.
- Controlled-impedance signal traces guarantee controlled characteristic impedance. Stripline and/or microstrip layout are recommended in all high-speed designs.

- Proper termination and line-impedance matching are required for EV kit operation. 50Ω to -2V termination is required for proper operation of ECL devices. Series termination between the latches and the MAX5012 was added to suppress transient currents on the data lines due to the two stub lines: one going to the data-out connector and the other to the device under test (DUT). When the line lengths manifest a propagation delay of greater than one-half of the source rise or fall time, termination should be considered.

Standard Initial Setup and Operational Check

Before connecting the user-furnished P1 connection, verify that all power sources are disabled.

Perform the following steps:

1. Set S1 (A0, A1) to (0, 0).
2. Adjust potentiometer R7 to approximately mid-position.
3. Ensure that jumper J3A is installed and that J3B is removed.
4. Connect the P1 connector.
5. Enable user-supplied power supplies. Verify that -D2 (-2 ±0.1V), -D5.2 (-5.2 ±0.2V), and -A5.2 (-5.2 ±0.2V) are present.
6. Set user-input digital pattern to FFF hex, and clock this data in at least two clock cycles.
7. Monitor DAC I_{OUT} (assuming that the output load has not been changed). Adjust R7 until -1.044 ±0.005VDC is present on your measuring instrument. Next, clock in a data pattern of zero, and verify that the DAC I_{OUT} voltage is 0.00 ±0.005VDC.

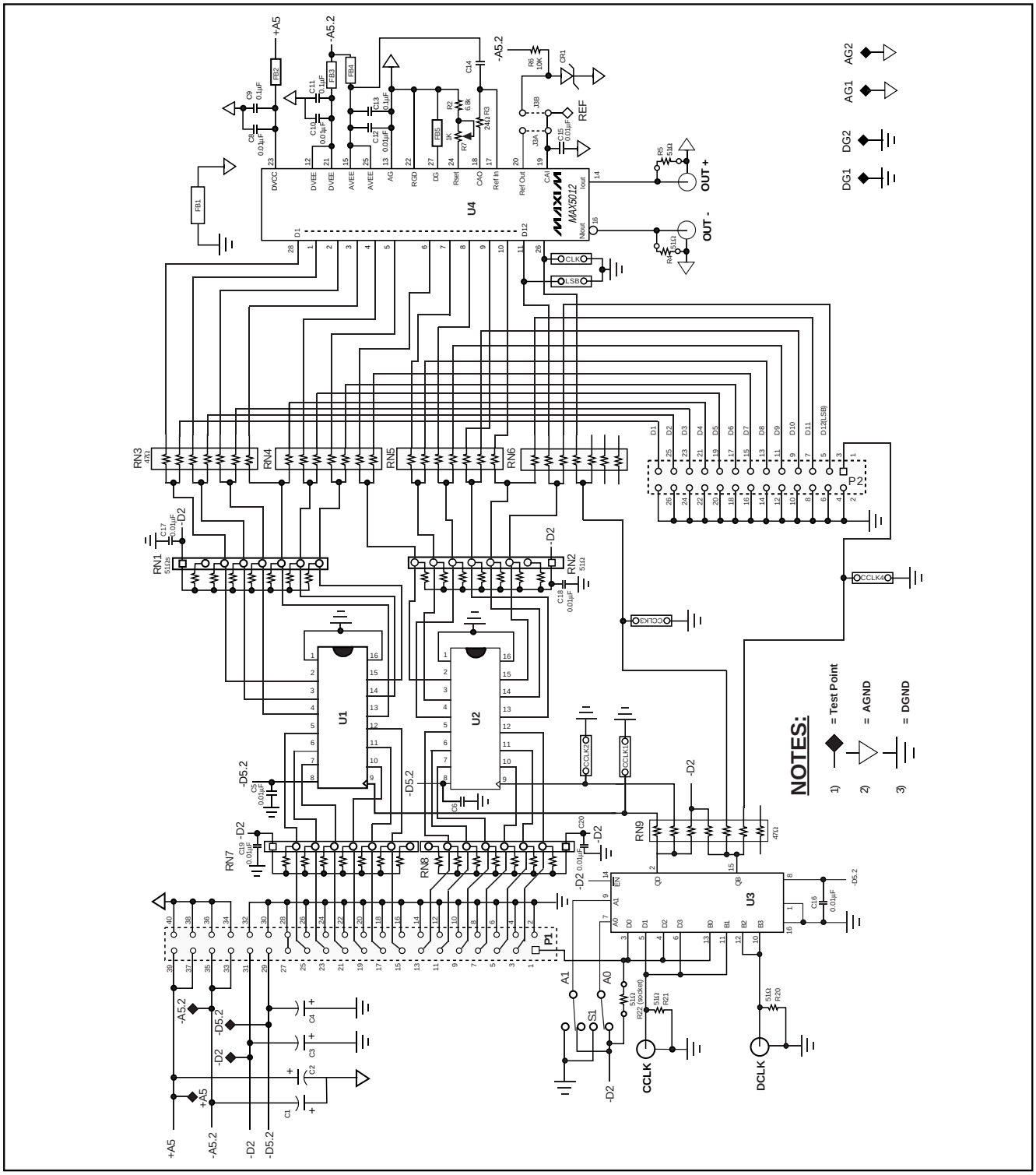


Figure 3. MAX5012 EV Kit Schematic

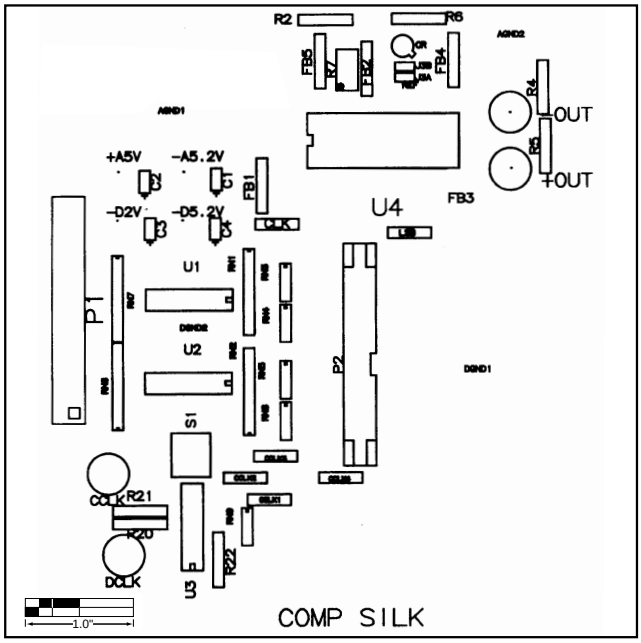


Figure 4. MAX5012 EV Kit Component Placement Guide—Component-Side Silk

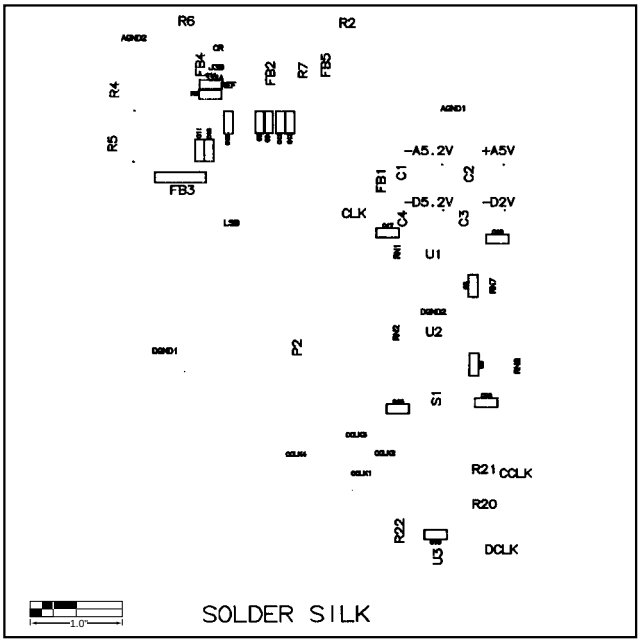


Figure 5. MAX5012 EV Kit Component Placement Guide—Solder-Side Silk

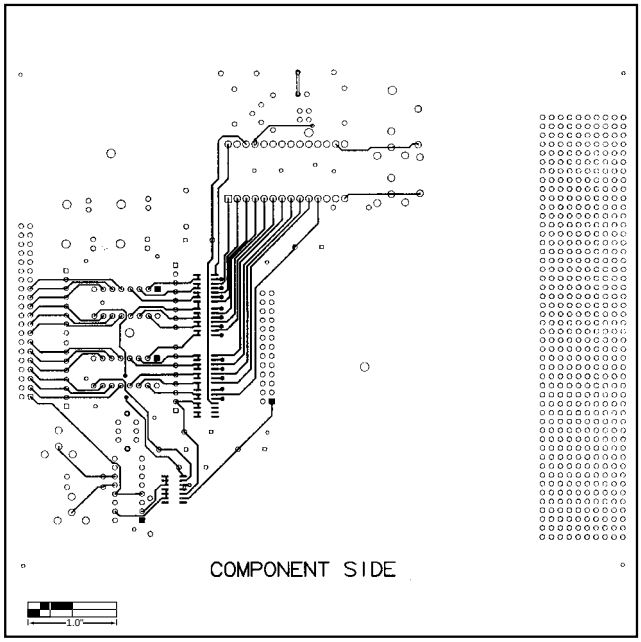


Figure 6. MAX5012 EV Kit PC Board Layout—Component Side

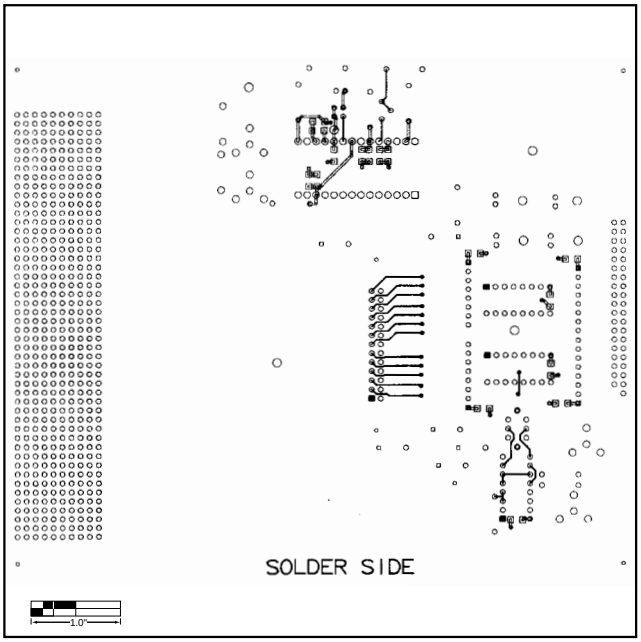


Figure 7. MAX5012 EV Kit PC Board Layout—Solder Side

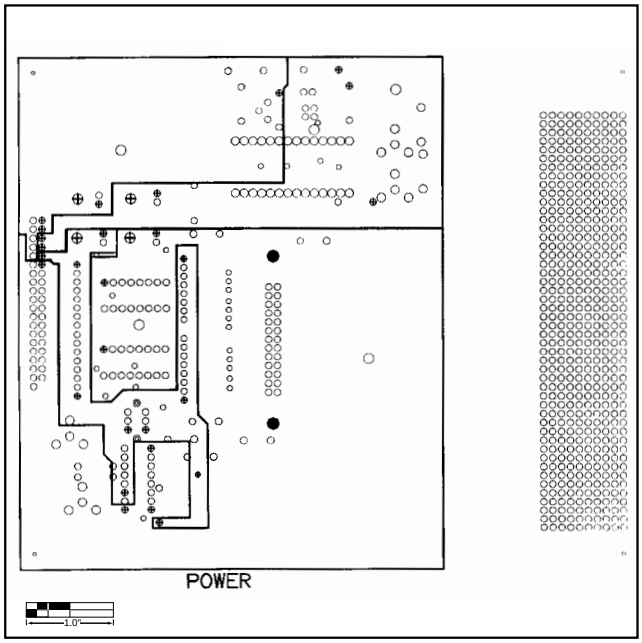


Figure 8. MAX5012 EV Kit PC Board Layout—Power Plane

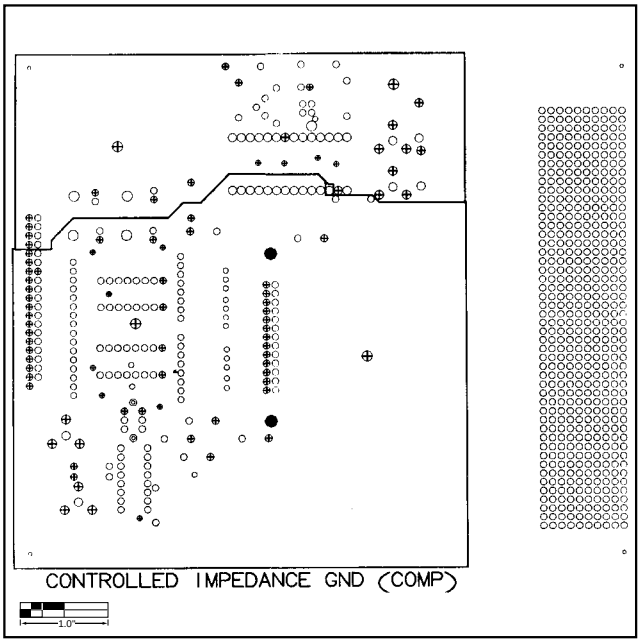


Figure 9. MAX5012 EV Kit PC Board Layout—Controlled-Impedance Ground Plane