19-1285; Rev 0; 7/97

MAXIM

MAX5013 Evaluation Kit

Evaluates: MAX5013

General Description

The MAX5013 evaluation kit (EV kit) is intended as a tool for device characterization and for demonstrating the performance of the MAX5013 12-bit, 100Msps, TTL binary digital-to-analog converter (DAC). Data is latched by applying up to a 12-bit TTL binary-data pattern and a clock. The output voltage (negative-going amplitude) can be seen at the BNC connector DAC OUT or at NDAC OUT (inverted).

The evaluation board is designed to cover a wide variety of applications, and can be easily modified to suit a specific application. The following functional blocks are described in detail:

- Power Supplies and Grounding
- Reference Circuits
- Latch and Conversion Clocks
- Digital Input and Controls
- Analog Output

Applications

Engineering Prototype Aid
Incoming Inspection Tool
Guide for PC Board Layout
Guide for Interface Design
Reconstruction DAC

Features

- ♦ **Up to 100Msps Conversion Rate**
- ♦ **Selectable Clock Control for Updating Data**
- ♦ **Reference Voltage: Internal, On-Board, or External**
- ♦ **Selected High-Speed Test Points**
- ♦ **Fully Assembled and Tested**
- ♦ **On-Board TTL Latches**
- ♦ **TTL Digital Input Connector**

Ordering Information

PART	TEMP. RANGE	BOARD TYPE
MAX5013EVKIT	0°C to +70°C	Through-Hole

Component List

DESIGNATION	QTY	DESCRIPTION
CCLK_EXT, DCLK_EXT, NDAC OUT, DAC OUT	4	BNC connectors
C1, C2, C3	3	10µF tantalum capacitors
C5–C8, C10, C14, C15, C51, C52	9	0.01µF chip capacitors
C9, C11, C13	3	0.1µF chip capacitors
C12, C50, C54	3	100pF chip capacitors
D1	1	1.2V reference diode
FB1–FB5	5	Ferrite beads
P1, P2	2	Connectors
R1, R2, R4, R6, R11, R12	6	51Ω, 1/8W, 5% resistors
R7	1	6.8kΩ chip resistor
R9	1	1kΩ, 12-turns potentiometer
R10	1	10kΩ, 1/8W, 5% resistor
R13–R16	4	47Ω chip resistors
R20	1	24Ω chip resistor
RN1, RN2, RN5, RN6	4	47Ω resistor networks
RN3, RN4	2	10kΩ resistor networks
U1, U2	2	Octal D flip-flops
U3	1	Exclusive-OR gate
U4	1	MAX5013AEPI
N/A	12	Pin sockets
N/A	*	Single-row header
N/A	4	Spacers
N/A	10	Test-point terminals
N/A	4	#4-40 pan-head screws
N/A	1	28-pin socket

**As required*

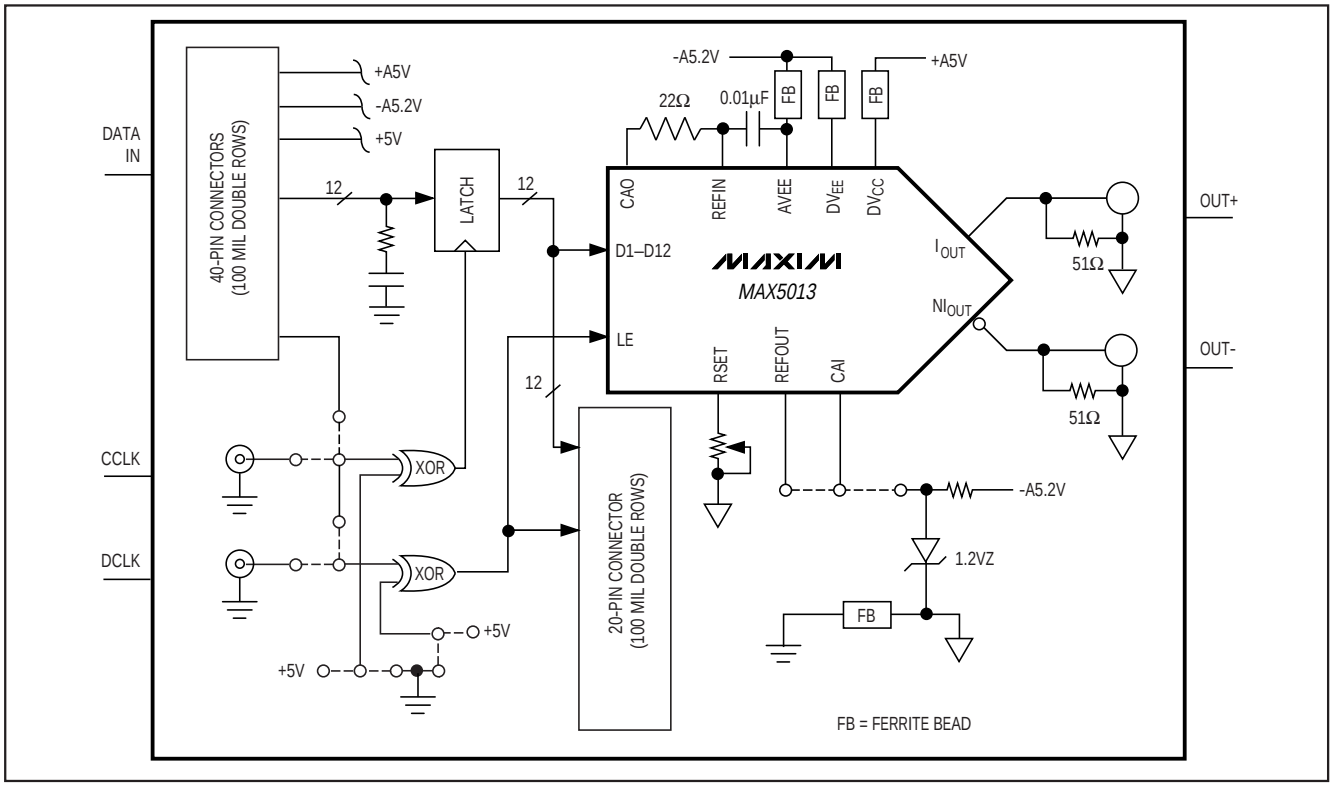


Figure 1. MAX5013 EV Kit Functional Diagram

Detailed Description

Power Supplies and Grounding

The MAX5013 evaluation kit (EV kit) is powered by two supplies: a -5.2V supply for the ADC and a +5V supply for digital latches and logic. Power is supplied through the P1 connector or test points. Adequate power-supply decoupling is incorporated into the design; however, use of adequate low-noise, regulated, low-source-impedance supplies is recommended. (Refer to Table 1 for signal and power connections.) Power distribution to the MAX5013 is filtered to isolate it from the digital switching noise associated with the on-board TTL latches.

Return-power connections and grounding are accomplished with a split ground plane: one for digital return and one for analog return. The two ground planes are coupled together through an inductive ferrite bead (FB1).

Reference

Reference-Voltage Source

The MAX5013's control amplifier requires a reference voltage to set the reference current (see the R_{SET} section). The reference voltage can come from one of three different sources:

- Ref Out (pin 20 on the MAX5013). Ref Out is the MAX5013's -1.2V ±50mV internal reference source. To use it, short jumper J5A and open J5B.
- On-board -1.2V reference circuit. This circuit comprises zener diode D1 and resistor R10. To use it, short jumper J5B and open J5A.
- External reference source. Remove both J5 jumpers and apply an external reference-voltage source (between -0.1V and -2V) to the REF test point. A time-varying signal may be used at this REF test point. Refer to the MAX5013 data sheet for the control amplifier's input impedance and bandwidth capabilities.

RSET

The DAC's output current is determined by the resistive circuit (R7 and potentiometer R9) connected to the MAX5013's R_{SET} pin (pin 24). Although this resistance is not directly measurable, it can be determined as a function of the DAC output current:

$$R_{SET} = (V_{REF} \times 128) / I_{OUT}$$

where: R_{SET} = resistance seen by MAX5013's R_{SET} pin
V_{REF} = reference voltage at test point REF
I_{OUT} = DAC output current

The output compliance voltage is not compromised if the board is set as in the *Standard Initial Setup and Operational Check* section.

Control-Amplifier Output

The MAX5013's control-amplifier output (CAO) biases the internal current sources. In the MAX5013 EV kit layout, the CAO is fed back into the reference input. **Note:** This signal must be decoupled to the DAC's analog V_{EE} supply.

Clock

The MAX5013 EV kit requires an external clock signal to initiate input data prelatching and MAX5013 data conversion. A single clock can be used for both data prelatching and MAX5013 conversion, or an additional decimation clock can be used to reduce the MAX5013's data-update rate. For proper operation, the external clock signals and the input data word must be within standard TTL signal levels. (Refer to Figure 2 for the clock's timing requirements.)

Jumpers J3 and J4 control clock-signal routing from the input connectors (P1, CCLK_EXT, DCLK_EXT) to the data latches (U1, U2) and the MAX5013 (U4). Jumpers J1 and J2 allow clock-signal inversion (see Table 2). Clock signals can be monitored at test points CCLK1–CCLK4 (refer to Figure 3 for test-point locations).

Single-Clock Configuration

Apply the external-clock signal to either connector P1 (pin 2) or the BNC labeled CCLK_EXT, and set jumper J3 accordingly. Configure single-clock mode using jumper J4 (position A) (refer to Table 2 and Figure 3).

Dual-Clock Configuration

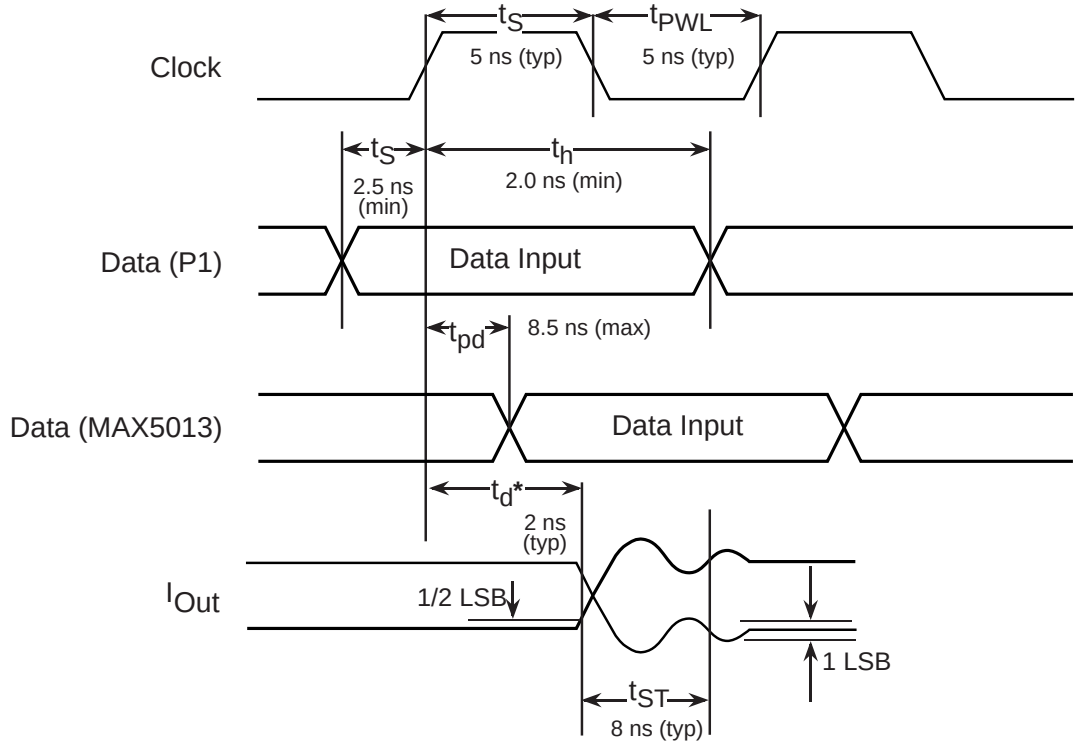
Apply the external-clock signal for data prelatching to either connector P1 (pin 2) or the BNC labeled CCLK_EXT, and set jumper J3 accordingly. Apply a second decimation-clock signal to the BNC labeled DCLK_EXT. Configure dual clock operation using jumper J4 (position B) (refer to Table 2 and Figure 3).

Table 1. Connector P1 Pinout

Pin No.	Description	Pin No.	Description
1	Digital Ground	21	Digital Ground
2	Clock	22	Data Bit 2
3	Digital Ground	23	Digital Ground
4	Data Bit 11 (MSB)	24	Data Bit 1
5	Digital Ground	25	Digital Ground
6	Data Bit 10	26	Data Bit 0
7	Digital Ground	27	Digital Ground
8	Data Bit 9	28	Digital Ground
9	Digital Ground	29	Digital Ground
10	Data Bit 8	30	No connection
11	Digital Ground	31	Digital Ground
12	Data Bit 7	32	+5V (digital)
13	Digital Ground	33	Analog Ground
14	Data Bit 6	34	-5.2V (analog)
15	Digital Ground	35	Analog Ground
16	Data Bit 5	36	-5.2V (analog)
17	Digital Ground	37	Analog Ground
18	Data Bit 4	38	+5V (analog)
19	Digital Ground	39	Analog Ground
20	Data Bit 3	40	+5V (analog)

Table 2. Clock Jumper Configuration

JUMPER	POSITION	DESCRIPTION/FUNCTION
J1	A	Data-latch clock, noninverted
	B	Data-latch clock, inverted
J2	A	MAX5013 conversion clock, noninverted
	B	MAX5013 conversion clock, inverted
J3	A	Data-latch clock, P1 source
	B	Data-latch clock, CCLK_EXT BNC source
J4	A	MAX5013 conversion clock, data-latch clock source
	B	MAX5013 conversion clock, DCLK_EXT BNC source



Notes: Diagram assumes the use of a single clock for the data latches and the MAX5013.

Timing is measured from 50% levels.

*t_d does not take into account skew between output gates.

t_{ST} is measured as a voltage settling at midscale transition to 0.024% into R_L = 50Ω.

Figure 2. Timing Diagram

Analog Output

The MAX5013's output comprises complementary current sinks (I_{OUT}, NI_{OUT}). Load resistors (R11, R12) develop an output voltage proportional to the DAC output current. The DAC output current is a function of the total resistance (R_{SET}) seen by the MAX5013's R_{SET} pin and the reference voltage (V_{REF}). For example:

Given: V_{REF} = -1.2V
R_{SET} = 7.5kΩ
$I_{OUT}(FS)$ = (-1.2V / 7.5kΩ) x 128 = -20.48mA

Then: $V_{OUT} = R_{LOAD} \times I_{OUT}(FS)$
= 51Ω x -20.48mA
= -1.044V (near the -1.2V minimum compliance voltage)

The user can modify the MAX5013 EV kit output load to incorporate a wide variety of signal levels; however, equivalently loading the outputs results in superior operational performance. In any design, both current and voltage specifications must be maintained on the output of this device.

Layout

Careful consideration was given to the layout of this evaluation board to ensure maximum performance for the MAX5013 and to help users develop similar design and layout aspects for their own designs. Some of the highlights of this design are as follows:

- The ground planes are split into an analog plane and a digital plane. They are tied together at only one point (through ferrite bead FB1).
- This evaluation board provides both low and high-frequency-bypass, power-supply-decoupling capacitors.
- Controlled-impedance signal traces are used to control characteristic impedance. Stripline and/or microstrip layout are recommended in all high-speed designs.
- Signal termination was added to suppress transient currents on the data lines due to mismatch of trace impedance to the device input; i.e., proper termination of the signal line. When the line lengths manifest a propagation delay of greater than one-half of the source's rise/fall time, termination should be considered.

Standard Initial Setup and Operational Check

Before connecting to the P1 connection, verify that all power sources are disabled.

Perform the following steps:

1) Set jumper J3 to the A or B position (depending on the CLK input). Set jumpers J1A, J2A, and J4A.
2) Adjust potentiometer R7 to approximately mid-position.
3) Ensure that jumper J5A is installed and that J5B is removed.
4) Connect the P1 connector.
5) Enable user-supplied power supplies. Verify that +A5.0 (+5.0 ±0.2V), -A5.2 (-5.2 ±0.2V), and +D5.0 (+5.0 ±0.2V) are present.
6) Set user-input digital pattern to FFF hex, and enable this data by toggling the clock at least two times.
7) Monitor DAC I_{OUT} (assuming that the output load has not been changed). Adjust R7 until -1.044 ±0.005V_{DC} is present on your measuring instrument. Next, clock in a data pattern of zero, and verify that the DAC I_{OUT} voltage is 0.00 ±0.005V_{DC}.

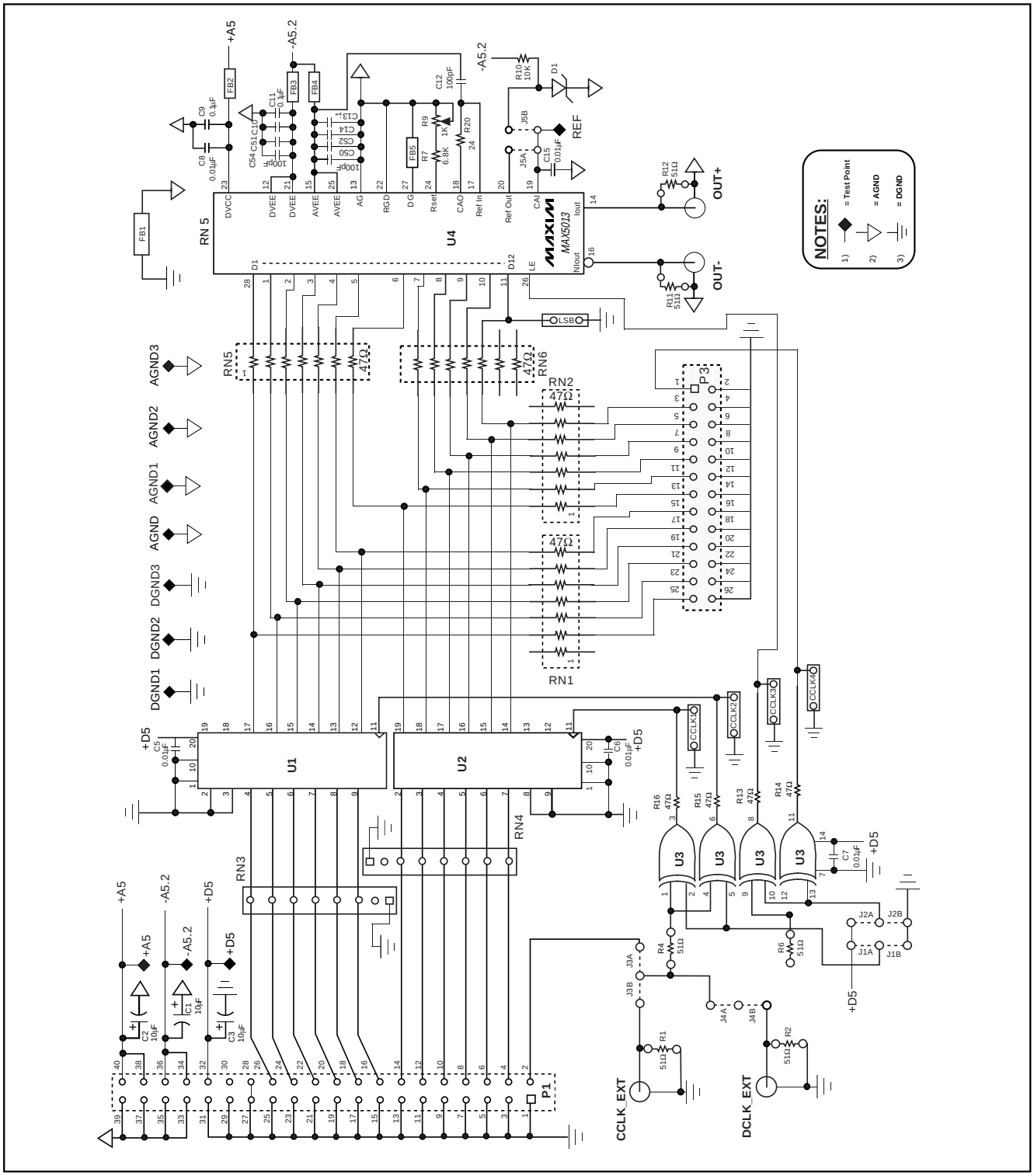


Figure 3. MAX5013 EV Kit Schematic

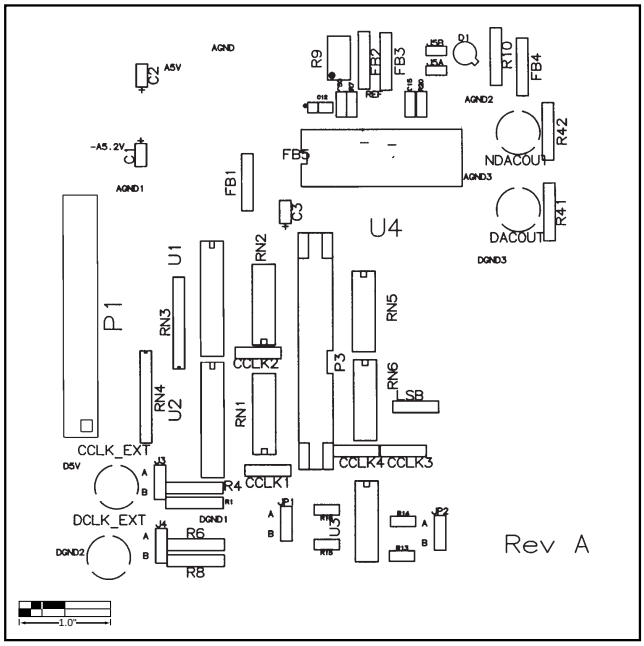


Figure 4. MAX5013 EV Kit Component Placement Guide—Component-Side Silk

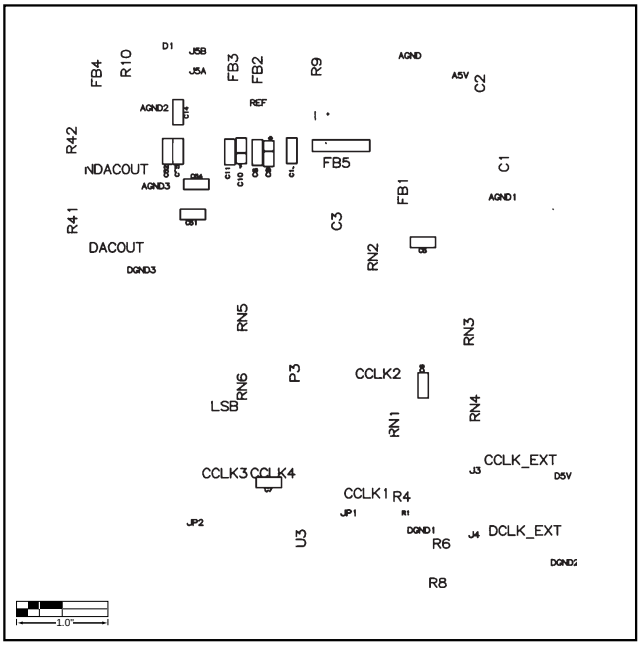


Figure 5. MAX5013 EV Kit Component Placement Guide—Solder-Side Silk

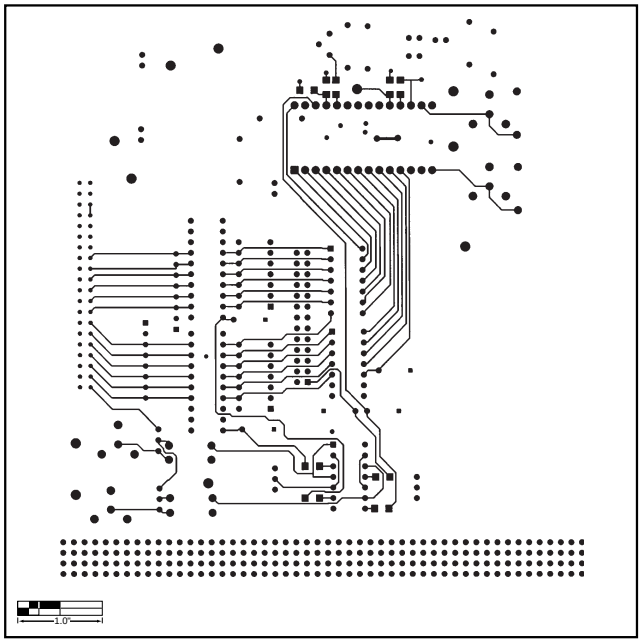


Figure 6. MAX5013 EV Kit PC Board Layout—Component Side

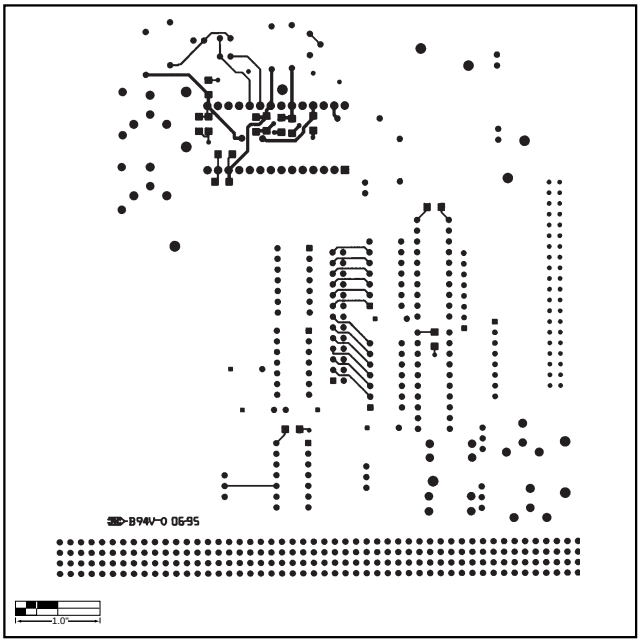


Figure 7. MAX5013 EV Kit PC Board Layout—Solder Side

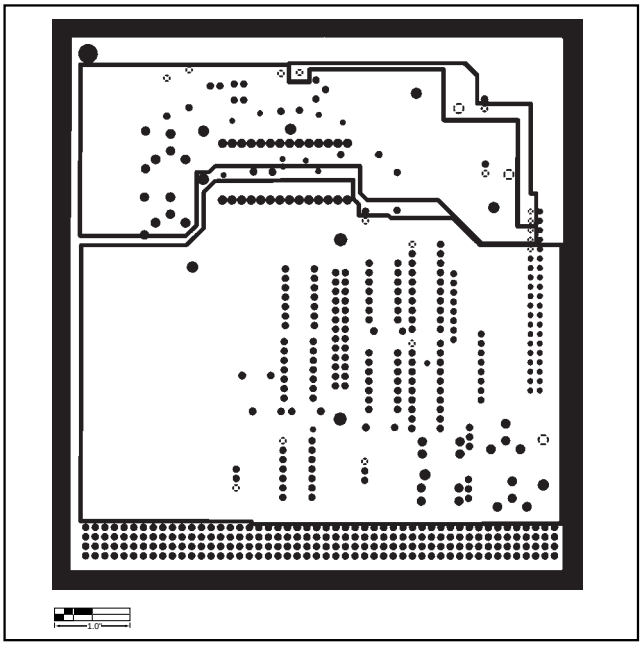


Figure 8. MAX5013 EV Kit PC Board Layout—Power Plane

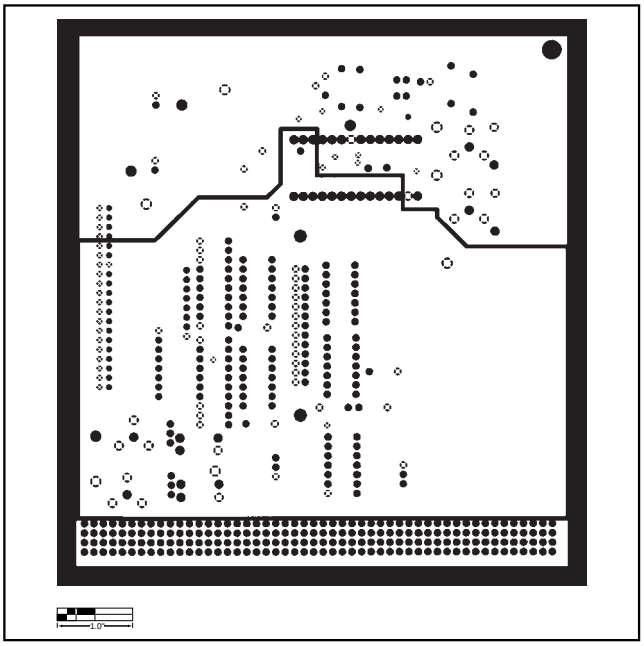


Figure 9. MAX5013 EV Kit PC Board Layout—Ground Plane