19-1256; Rev 0; 7/97

EVALUATION KIT MANUAL FOLLOWS DATA SHEET

Direct-Conversion Tuner IC for Digital DBS Applications

MAX2102

General Description

The MAX2102† is a low-cost direct-conversion tuner IC designed for use in digital direct-broadcast satellite (DBS) television set-top box units. Its direct-conversion architecture reduces system cost compared to devices with IF-based architectures.

The MAX2102 directly tunes L-band signals to baseband using a broadband I/Q downconverter. Operating frequency range spans from at least 950MHz to 2150MHz.

The IC includes an LNA with AGC, two downconverter mixers, an oscillator buffer with 90° quadrature generator and prescaler, and baseband amplifiers.

Applications

DirecTV, PrimeStar, EchoStar DBS Tuners

DVB-Compliant DBS Tuners

Cellular Basestations

Wireless Local Loop

Broadband Systems

LMDS

Features

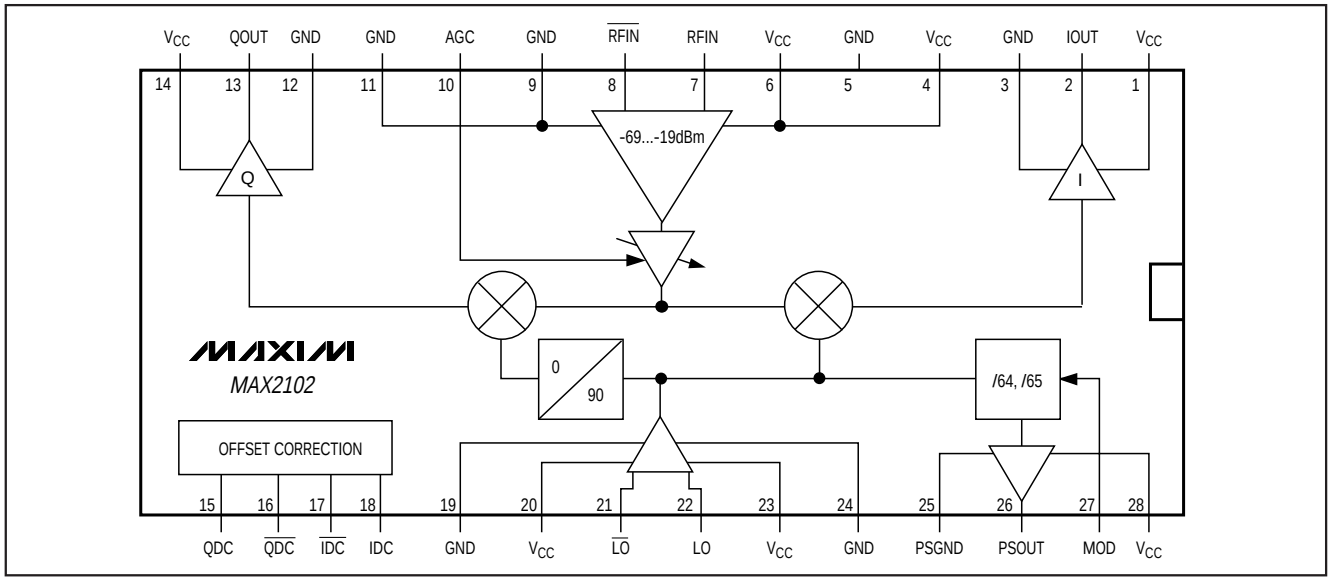
- **Low-Cost Bipolar Design, Lowest Cost Architecture**
- **Operates from Single +5V Supply**
- **950MHz to 2150MHz Input Frequency Range***
- **On-Chip Quadrature Generator, Dual-Modulus Prescaler (/64, /65)**
- **Input Levels: -19dBm to -69dBm per Carrier**
- **Over 50dB AGC Control Range**
- **Noise Figure = 13.2dB; IIP3 = 6.5dBm (at 1450MHz)**
- **Automatic Baseband Offset Correction**
- **Easy Interface to MAX1002/MAX1003 Dual ADC and Popular Baseband ICs**
- **Evaluation Kit Available, Tuner Reference Design Assistance Available**

**Contact factory for MAX2102 versions with expanded frequency range.*

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2102CWI	0°C to +70°C	28 SO

Functional Diagram



†*Patents Pending*

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.5V to 7V
RFIN to $\overline{RFIN}$ .....±2V
LO- to $\overline{LO}$ .....±2V
AGC, MOD, RFIN, $\overline{RFIN}$, LO, $\overline{LO}$ to GND...-0.5V to (V_{CC} + 0.5V)
AGC CURRENT .....±50mA
IDC to $\overline{IDC}$, QDC to $\overline{QDC}$.....±2V
IOUT or QOUT to GND Short-Circuit Duration 10sec
PSOUT to GND Short-Circuit Duration.....None

IDC, $\overline{IDC}$, QDC, $\overline{QDC}$ to GND .....-0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
SO (derate 12.50mW/°C above + 70°C).....1.025W
Operating Temperature Range
MAX2102CWI.....0°C to +70°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.25V; GND = 0V; PSGND = GND; AGC = 1.3V; MOD = 0.8V; P_{RFIN} = OFF; f_{LO} = 1450.125MHz; P_{LO} = -15dBm; I_{OUT}, Q_{OUT} = open; T_A = 0°C to +70°C; unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY					
Supply Voltage		4.75		5.25	V
Supply Current			150	195	mA
CONTROL INPUTS, PRESCALER					
MOD Input Low Level				0.8	V
MOD Input High Level		2.0			V
MOD Input Bias Current	0V < MOD < V_{CC}	-80		10	µA
AGC Input Bias Current	1V < AGC < 4V	-180		180	µA
IOUT, QOUT Common-Mode Voltage		2.2		2.6	V

AC ELECTRICAL CHARACTERISTICS

(MAX2102 EV kit circuit (Figure 1); V_{CC} = 5V; PSGND = open; MOD = GND; f_{RFIN} = 2150MHz; P_{RFIN} = -19dBm; f_{LO} = 2150.125MHz; P_{LO} = -15dBm driven single-ended into LO; AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p; IOUT, QOUT drives AC-coupled 100Ω load; 2kΩ from PSOUT to GND; T_A = +25°C; unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF FRONT END					
RFIN Carrier Frequency Range	(Note 1)	950		2150	MHz
RFIN Maximum Single-Carrier Input Power	Refers to single-carrier power generating V_{IOUT} = V_{QOUT} = 0.5Vp-p. 950MHz < f_{RFIN} < 2150MHz, 950MHz < f_{LO} < 2150MHz (Note 4)	-19			dBm
RFIN Minimum Single-Carrier Input Power	Refers to single-carrier power generating V_{IOUT} = V_{QOUT} = 0.5Vp-p. 950MHz < f_{RFIN} < 2150MHz, 950MHz < f_{LO} < 2150MHz (Note 4)			-69	dBm
AGC Range	1V < V_{AGC} < 4V	50			dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2102 EV kit circuit (Figure 1); V_{CC} = 5V; PSGND = open; MOD = GND; f_{RFIN} = 2150MHz; P_{RFIN} = -19dBm; f_{LO} = 2150.125MHz; P_{LO} = -15dBm driven single-ended into LO; AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p; IOUT, QOUT drives AC-coupled 100Ω load; 2kΩ from PSOUT to GND; T_A = +25°C; unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RFIN Input Third-Order Intercept Point	P_{RFIN} = -19dBm per tone, AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p per tone, $f1_{RFIN}$ = 1448.1MHz, $f2_{RFIN}$ = 1449MHz, f_{LO} = 1451MHz			6.5		dBm
RFIN Input Second-Order Intercept Point	P_{RFIN} = -19dBm per tone, AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p per tone, $f1_{RFIN}$ = 1200MHz, $f2_{RFIN}$ = 2150MHz, f_{LO} = 951MHz			15.1		dBm
Noise Figure	f_{RFIN} = 1441MHz, f_{LO} = 1451MHz	P_{RFIN} = -69dBm		13.2		dB
	f_{RFIN} = 2141MHz, f_{LO} = 2151MHz	P_{RFIN} = -69dBm		12.9		
		AGC = 4V, P_{RFIN} set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p		11.2		
Maximum Noise-Figure Variation with AGC Gain Setting	Defined as ΔNF/ΔGain; for AGC range, defined as single-carrier power range of -69dBm to -59dBm			-0.5		dB/dB
RFIN Worst-Case VSWR across Band	f_{RFIN} = 950MHz to 2150MHz, 50Ω source			2.3:1		
Maximum Power of Spurious Downconversion Products	950MHz < f_{RFIN} < 2150MHz, 950MHz < f_{LO} < 2150MHz. Dominated by LO second-harmonic power causing downconversion of unwanted channel. Test conditions: f_{LO} = 1075.5MHz, f_{RFIN} = 2150MHz, P_{RFIN} = -69dBm			32.3		dBc
LO Leakage at RFIN	P_{LO} = -15dBm, 950MHz < f_{LO} < 2150MHz (Note 2)				-49	dBm
	P_{LO} = -15dBm, $P_{\overline{LO}}$ = -15dBm (differentially driven), 950MHz < f_{LO} < 2150MHz (Note 2)				-54	

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2102 EV kit circuit (Figure 1); V_{CC} = 5V; PSGND = open; MOD = GND; f_{RFIN} = 2150MHz; P_{RFIN} = -19dBm; f_{LO} = 2150.125MHz; P_{LO} = -15dBm driven single-ended into LO; AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p; IOUT, QOUT drives AC-coupled 100Ω load; 2kΩ from PSOUT to GND; T_A = +25°C; unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OSCILLATOR BUFFER, QUADRATURE GENERATOR, PRESCALER						
LO Input Frequency Range	(Note 1)		950		2150	MHz
LO Input Worst-Case VSWR over Band	f_{LO} = 950MHz to 2150MHz, 50Ω source into MAX2102 EV kit match circuit			1.75:1		
LO Input Power Level	(Note 3)		-15		-5	dBm
	Refers to power level driven into LO, $\overline{LO}$ (differentially driven) (Notes 3, 4)		-15			
RFIN to LO Input Isolation	(Notes 4, 5)		28			dB
IOUT, QOUT Phase Imbalance	950MHz < f_{RFIN} < 2150MHz; 950MHz < f_{LO} < 2150MHz; P_{RFIN} = -40dBm; f_{IOUT}, f_{QOUT} = 125kHz (Note 4)				3	degrees
Worst-Case Additional Phase Imbalance Over Temperature	T_A = +25°C to +70°C (Notes 4 and 8)			-0.1	0.6	degrees
	T_A = +25°C to +0°C (Note 4)			0.07	1	
IOUT, QOUT Amplitude Imbalance	950MHz < f_{RFIN} < 2150MHz; 950MHz < f_{LO} < 2150MHz; P_{RFIN} = -40dBm; f_{IOUT}, f_{QOUT} = 125kHz (Note 4)				0.5	dB
Prescaler Divide Ratio	T_A = 0°C to +70°C (Note 4)	MOD = low	64		64	
		MOD = high	65		65	
Prescaler Output Swing at PSOUT	2kΩ | | 10pF load		0.8			Vp-p
Prescaler Duty Cycle at PSOUT	PSOUT load = 2kΩ | | 5pF (Note 2)		35		65	%
BASEBAND AC CHARACTERISTICS						
IOUT, QOUT Clipping Level	P_{RFIN} = -50dBm; AGC = 4V, V_{CC} = 5.0V			2.7		Vp-p
Baseband Bandwidth (at IOUT, QOUT)	At -3dB attenuation			94		MHz
Baseband Gain Ripple (at IOUT, QOUT)	1kHz > $f_{IOUT, QOUT}$ > 25MHz, 950MHz < f_{RFIN} < 2150MHz, 950MHz < f_{LO} < 2150MHz (Notes 2, 6, 7)			0.45	0.85	dB
Baseband Group Delay Ripple (at IOUT, QOUT)	1kHz > $f_{IOUT, QOUT}$ > 25MHz, 950MHz < f_{RFIN} < 2150MHz, 950MHz < f_{LO} < 2150MHz (Notes 2, 6)			0.45		ns

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2102 EV kit circuit (Figure 1); V_{CC} = 5V; PSGND = open; MOD = GND; f_{RFIN} = 2150MHz; P_{RFIN} = -19dBm; f_{LO} = 2150.125MHz; P_{LO} = -15dBm driven single-ended into LO; AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p; IOUT, QOUT drives AC-coupled 100Ω load; 2kΩ from PSOUT to GND; T_A = +25°C; unless otherwise noted.)

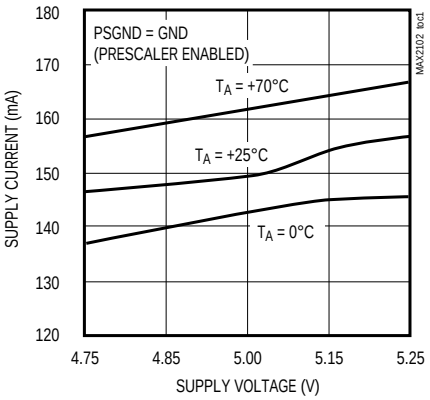
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IOUT, QOUT Output Impedance	(Note 2)		4.7	10	Ω
Maximum IOUT to QOUT Output Impedance Difference	(Note 2)		±1		Ω
Power-Supply Ripple Rejection (measured at IOUT, QOUT)	V_{CC} = 5V + 50mVp-p at 300kHz. Amplitude of 300kHz relative to 500mVp-p measured at IOUT, QOUT. Measured using MAX2102 EV kit.		32		dBc

Note 1: All specifications with guaranteed min/max limits are met within this frequency range. Contact factory for MAX2102 versions with expanded frequency range.
Note 2: Guaranteed by design and characterization.
Note 3: IOUT, QOUT Phase and Amplitude Imbalance specifications are met within this LO power range.
Note 4: Guaranteed by production test and/or design and characterization.
Note 5: Tested under two conditions: 1) Normal test: P_{RFIN} = -20dBm, and 2) Overdrive test: P_{RFIN} = -5dBm but AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p for P_{RFIN} = 30dBm.
Note 6: Includes contribution from front-end gain tilt and delay variations produced by varying f_{RFIN} by ±30MHz.
Note 7: 1kHz minimum frequency determined by 0.22µF offset-correction capacitors. Different value capacitors yield proportionally different low-frequency cutoffs. Group delay at low frequencies will also be affected. See *Applications Information* section.
Note 8: Negative numbers (-0.1°) indicate improvement in quadrature accuracy with increasing temperature.

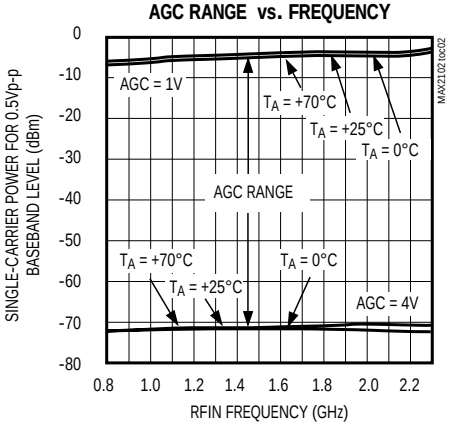
Typical Operating Characteristics

(MAX2102 EV kit circuit (Figure 1), V_{CC} = 5V, PSGND = open, MOD = GND, f_{RFIN} = 2150MHz, P_{RFIN} = -19dBm, f_{LO} = 2150.125MHz, P_{LO} = -15dBm driven single-ended into LO, AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p, IOUT, QOUT drives AC-coupled 100Ω load, 2kΩ from PSOUT to GND, T_A = +25°C, unless otherwise noted.)

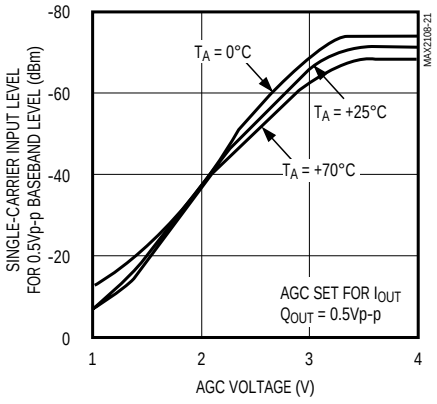
SUPPLY CURRENT vs. SUPPLY VOLTAGE



AGC RANGE vs. FREQUENCY



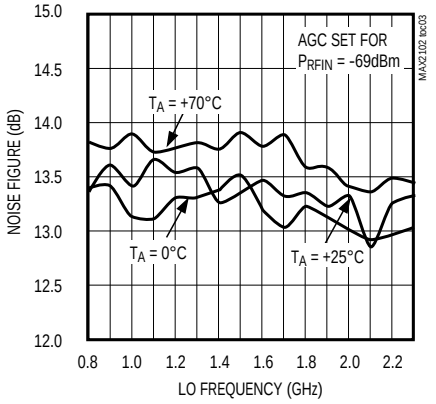
CARRIER LEVEL vs. AGC VOLTAGE



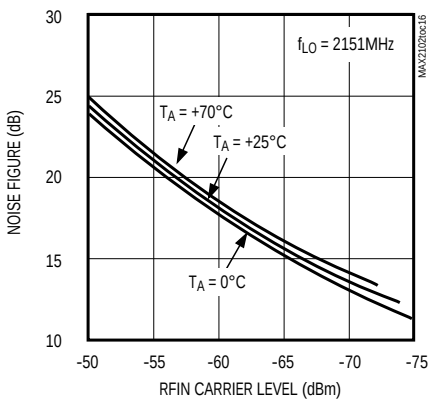
Typical Operating Characteristics (continued)

(MAX2102 EV kit circuit (Figure 1), V_{CC} = 5V, PSGND = open, MOD = GND, f_{RFIN} = 2150MHz, P_{RFIN} = -19dBm, f_{LO} = 2150.125MHz, P_{LO} = -15dBm driven single-ended into LO, AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p, IOUT, QOUT drives AC-coupled 100Ω load, 2kΩ from PSOUT to GND, T_A = +25°C, unless otherwise noted.)

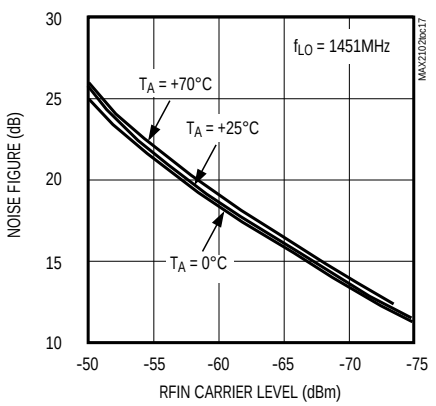
NOISE FIGURE vs. FREQUENCY



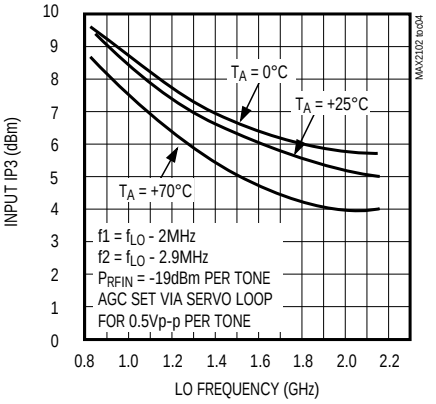
NOISE FIGURE vs. INPUT CARRIER LEVEL



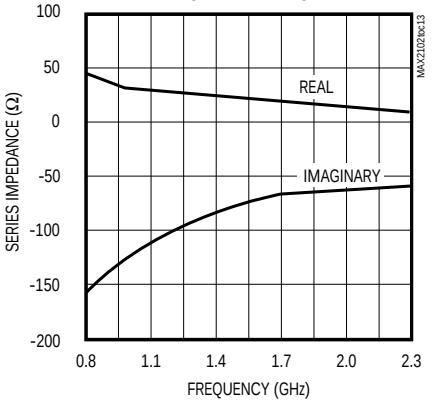
NOISE FIGURE vs. INPUT CARRIER LEVEL



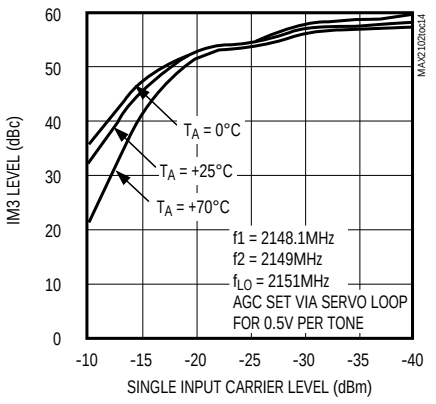
INPUT-REFERRED IP3 vs. FREQUENCY



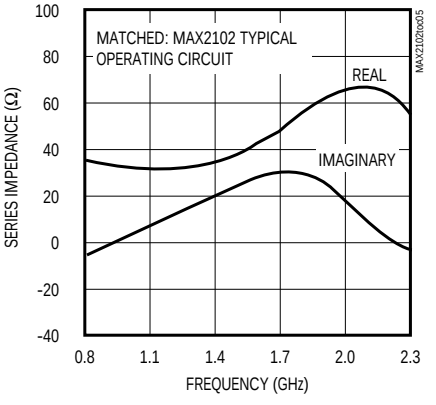
LO PORT IMPEDANCE vs. FREQUENCY (UNMATCHED)



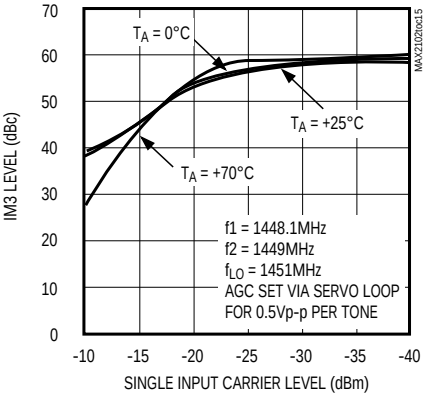
IM3 LEVELS vs. INPUT CARRIER POWER LEVEL



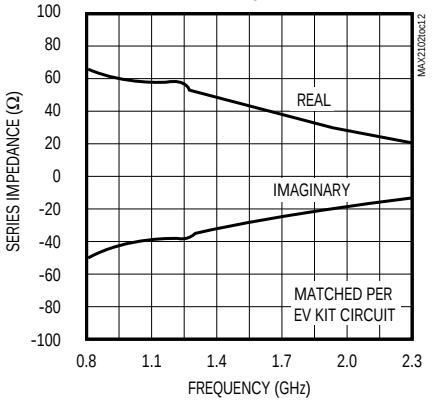
LO PORT IMPEDANCE vs. FREQUENCY



IM3 LEVELS vs. INPUT CARRIERS POWER LEVEL



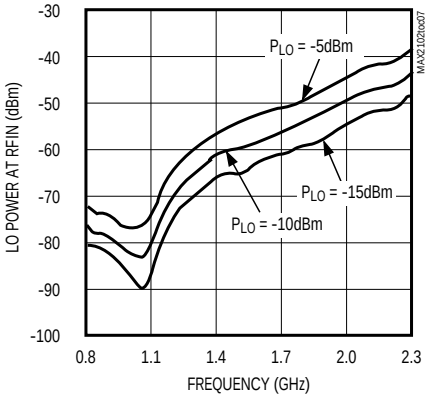
RFIN PORT IMPEDANCE vs. FREQUENCY



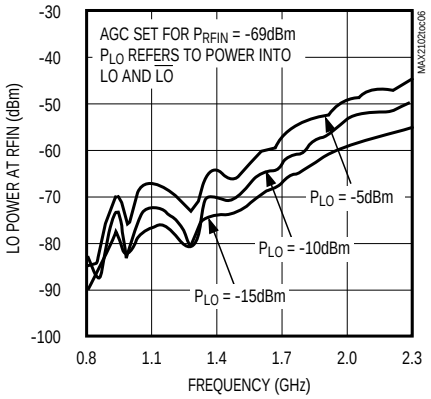
Typical Operating Characteristics (continued)

(MAX2102 EV kit circuit (Figure 1), V_{CC} = 5V, PSGND = open, MOD = GND, f_{RFIN} = 2150MHz, P_{RFIN} = -19dBm, f_{LO} = 2150.125MHz, P_{LO} = -15dBm driven single-ended into LO, AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p, IOUT, QOUT drives AC-coupled 100Ω load, 2kΩ from PSOUT to GND, T_A = +25°C, unless otherwise noted.)

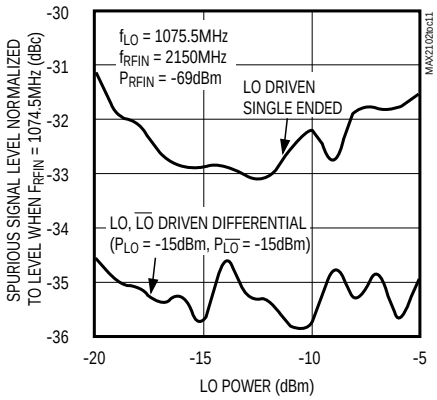
LO LEAKAGE AT RFIN vs. FREQUENCY (SINGLE-ENDED LO DRIVE)



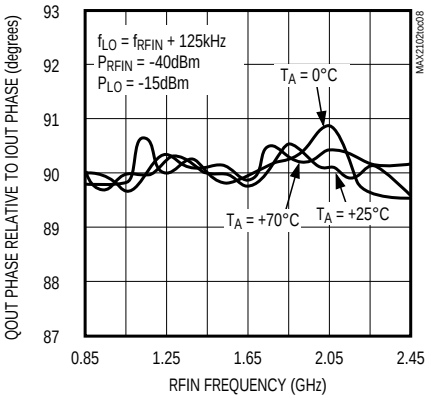
LO LEAKAGE AT RFIN vs. FREQUENCY (DIFFERENTIAL LO DRIVE)



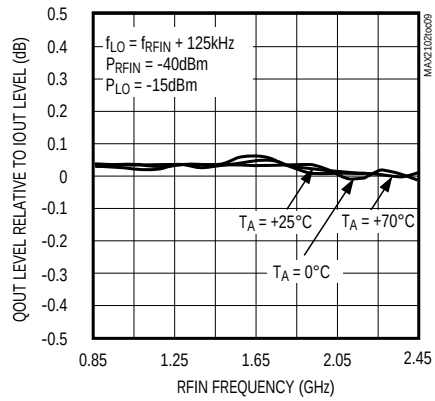
SPURIOUS DOWNCONVERSION DUE TO INTERNALLY GENERATED LO 2ND HARMONIC



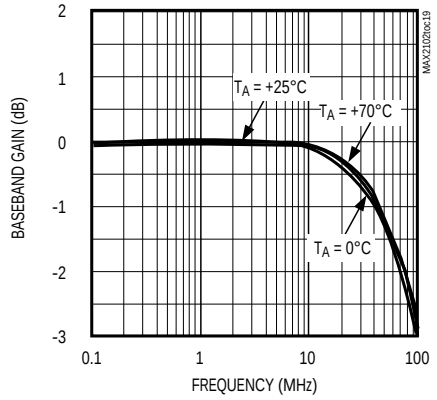
QUADRATURE PHASE IMBALANCE vs. FREQUENCY



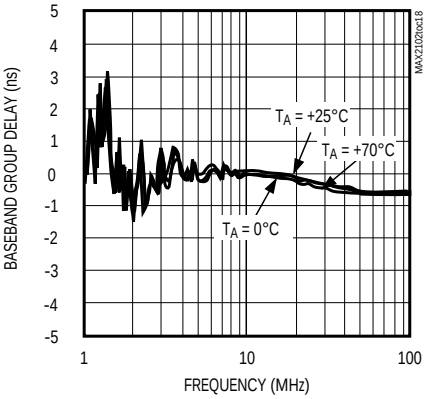
QUADRATURE GAIN IMBALANCE vs. FREQUENCY



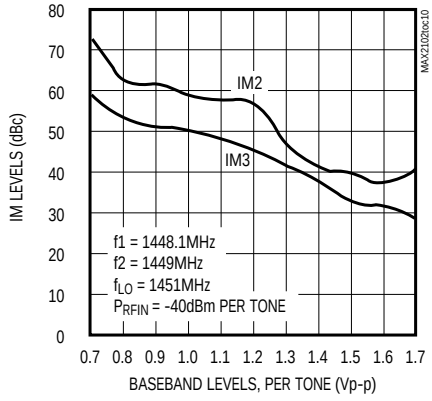
BASEBAND GAIN FLATNESS vs. FREQUENCY



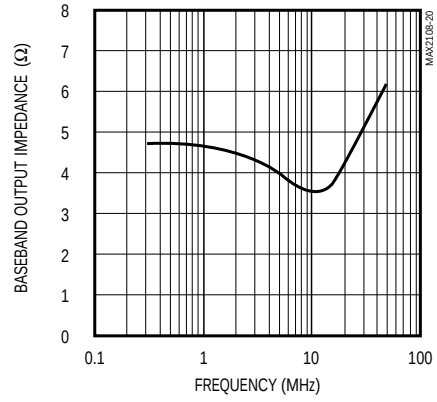
BASEBAND GROUP DELAY FLATNESS vs. FREQUENCY



BASEBAND IM LEVELS



BASEBAND OUTPUT IMPEDANCE vs. FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Baseband +5V Supply. Bypass with a 10pF capacitor from this pin to pin 3 (GND), as close to the IC as possible. Connect an additional 0.1µF capacitor in parallel with the 10pF capacitor (placement less critical).
2	IOUT	I Channel Baseband Output
3, 12	GND	Baseband Ground
4	V_{CC}	RF +5V Supply. Bypass with a 22pF capacitor from this pin to pin 11 (GND), as close to the IC as possible.
5	GND	Ground (substrate)
6	V_{CC}	RF +5V Supply. Bypass with a 22pF capacitor from this pin to pin 9 (GND), as close to the IC as possible.
7	RFIN	RF Noninverting Input. Couple through a 22pF capacitor directly to a 50Ω signal source.
8	$\overline{RFIN}$	RF Inverting Input. Connect to a 22pF series capacitor and a 51Ω resistor to ground.
9, 11, 19, 24	GND	RF Ground. Connect directly to the ground plane.
10	AGC	Automatic Gain-Control Input. Bypass this pin with a 1000pF capacitor close to the pin, to minimize coupling.
13	QOUT	Q Channel Baseband Output
14	V_{CC}	Baseband +5V Supply. Bypass with a 10pF capacitor from this pin to pin 12 (GND), as close to the IC as possible. Connect an additional 0.1µF capacitor in parallel with the 10pF capacitor (placement less critical).
15	QDC	Q Channel Offset-Correction Noninverting Input. Connect a 0.22µF (typ) capacitor between QDC and $\overline{QDC}$. This capacitor must be placed as close to the IC as possible. See *Layout Considerations* section.
16	$\overline{QDC}$	Q Channel Offset-Correction Inverting Input. Connect a 0.22µF (typ) capacitor between QDC and $\overline{QDC}$. This capacitor must be placed as close to the IC as possible. See *Layout Considerations* section.
17	$\overline{IDC}$	I Channel Offset-Correction Inverting Input. Connect a 0.22µF (typ) capacitor between IDC and $\overline{IDC}$. This capacitor must be placed as close to the IC as possible. See *Layout Considerations* section.
18	IDC	I Channel Offset-Correction Noninverting Input. Connect a 0.22µF (typ) capacitor between IDC and $\overline{IDC}$. This capacitor must be placed as close to the IC as possible. See *Layout Considerations* section.
20	V_{CC}	RF +5V Supply. Bypass with a 10pF capacitor from this pin to pin 19 (GND) as close to the IC as possible.
21	$\overline{LO}$	Local-Oscillator Complementary Input Port (Figure 1)
22	LO	Local-Oscillator Input Port (Figure 1)
23	V_{CC}	RF +5V Supply. Bypass with a 10pF capacitor from this pin to pin 24 (GND) as close to the IC as possible.
25	PSGND	Prescaler Ground. To disable the prescaler, leave this pin open.
26	PSOUT	Prescaler Output. Drives CMOS load. Connect 2kΩ from this pin to GND (if the prescaler is enabled).
27	MOD	Prescaler Modulus Control. Leave open when the prescaler is disabled.
28	V_{CC}	Prescaler +5V Supply. Bypass with a 1000pF capacitor. **Must be connected even if the prescaler is disabled.**

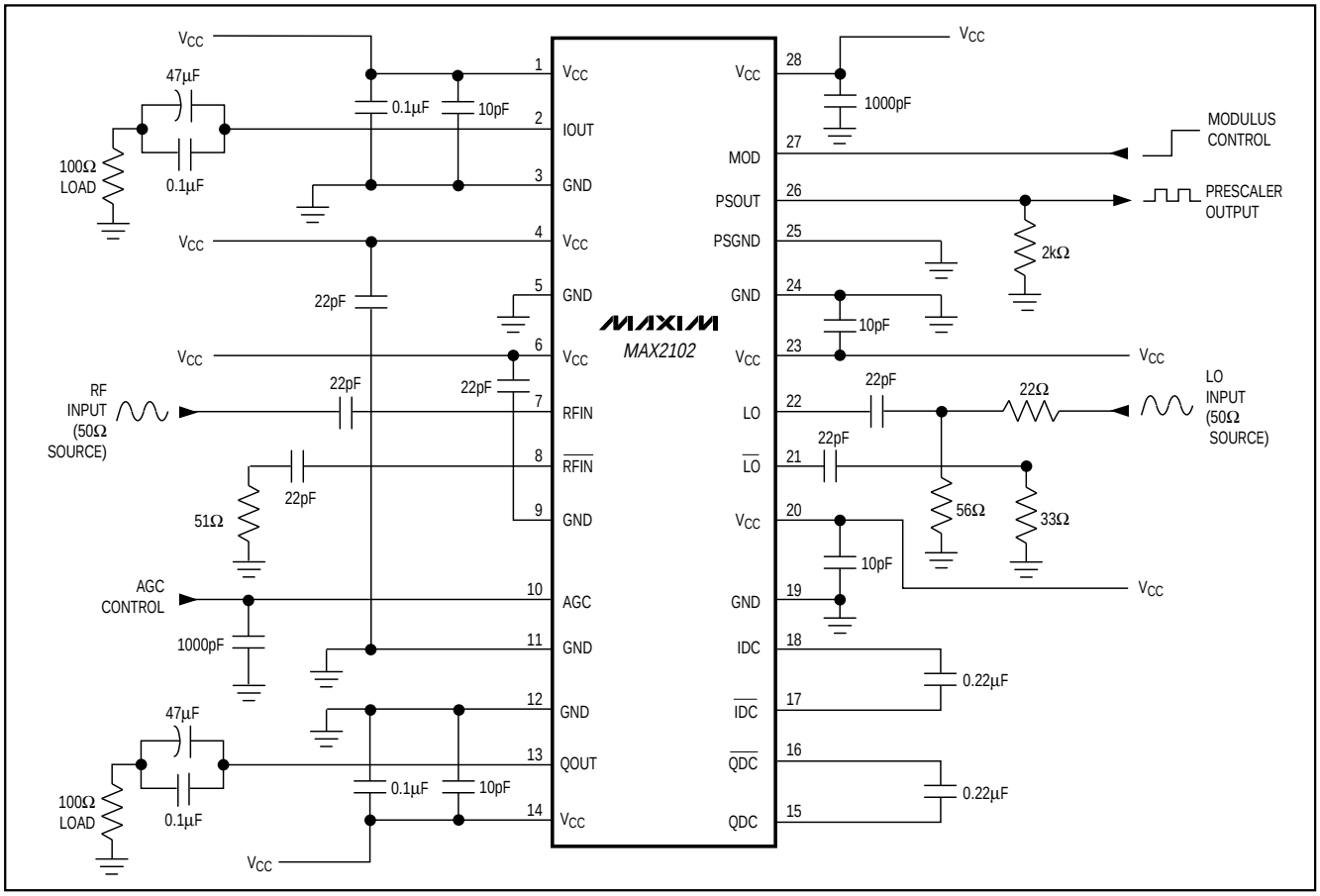


Figure 1. Typical Operating Circuit

Detailed Description

The MAX2102 downconverts signals in the range 950MHz to 2150MHz directly to baseband I/Q signals. It is targeted for digital DBS tuner applications where a direct downconversion provides a cost savings over prior-art multiple-conversion approaches. However, the MAX2102 is applicable to any system requiring a broadband I/Q downconversion.

Internally, the MAX2102 consists of a broadband front-end variable gain stage, a quadrature downconverter, an oscillator buffer, high-linearity I and Q baseband amplifiers, and offset correction amplifiers.

The front-end AGC dynamic range is over 50dB. Specifically, the AGC control can be adjusted so that a sine wave at RFIN ranging in power from -69dBm to -19dBm will produce a sine wave at IOUT and QOUT at 500mVp-p levels. The noise figure is lowest when the AGC is at its maximum gain setting (see *Typical Operating Characteristics*). The VSWR at RFIN is unaffected by the AGC setting.

The LO buffer accepts an external LO signal at LO, $\overline{LO}$, and internally limits the signals to provide a consistent on-chip LO level. The LO input drive level should be maintained within the specified limits (see *Applications Information* section).

The quadrature downconverter follows the front-end AGC. Two mixers are driven by the previous stage AGC amplifier output. The mixer LO ports are fed with the two LO signals, which are 90° apart in phase. These quadrature LO signals are generated on-chip using the LO signals from the LO buffer.

The resulting I/Q baseband signals are fed through separate I and Q channel baseband amplifiers. Robust output stages drive IOUT and QOUT. The outputs are capable of driving lowpass filters with 100Ω characteristic impedance (that is, the equivalent of an AC-coupled, 100Ω load). The baseband -3dB output bandwidth is over 90MHz.

Direct-Conversion Tuner IC for Digital DBS Applications

Applications Information

Front-End Tuner Circuitry for DBS Tuners

In a typical application, the signal path ahead of the MAX2102 will include a discrete LNA/buffer and a PIN-diode attenuator. Alternatively, a dual-gate GaAsFET can serve this function. This circuitry is usually required in order to meet system noise-figure requirements, may provide a buffered F-connector output, and may also be required to meet stringent LO leakage requirements. The PIN attenuator is typically controlled by the same voltage as the MAX2102 AGC control pin so that, overall, a single AGC line from the baseband processor can control the entire tuner.

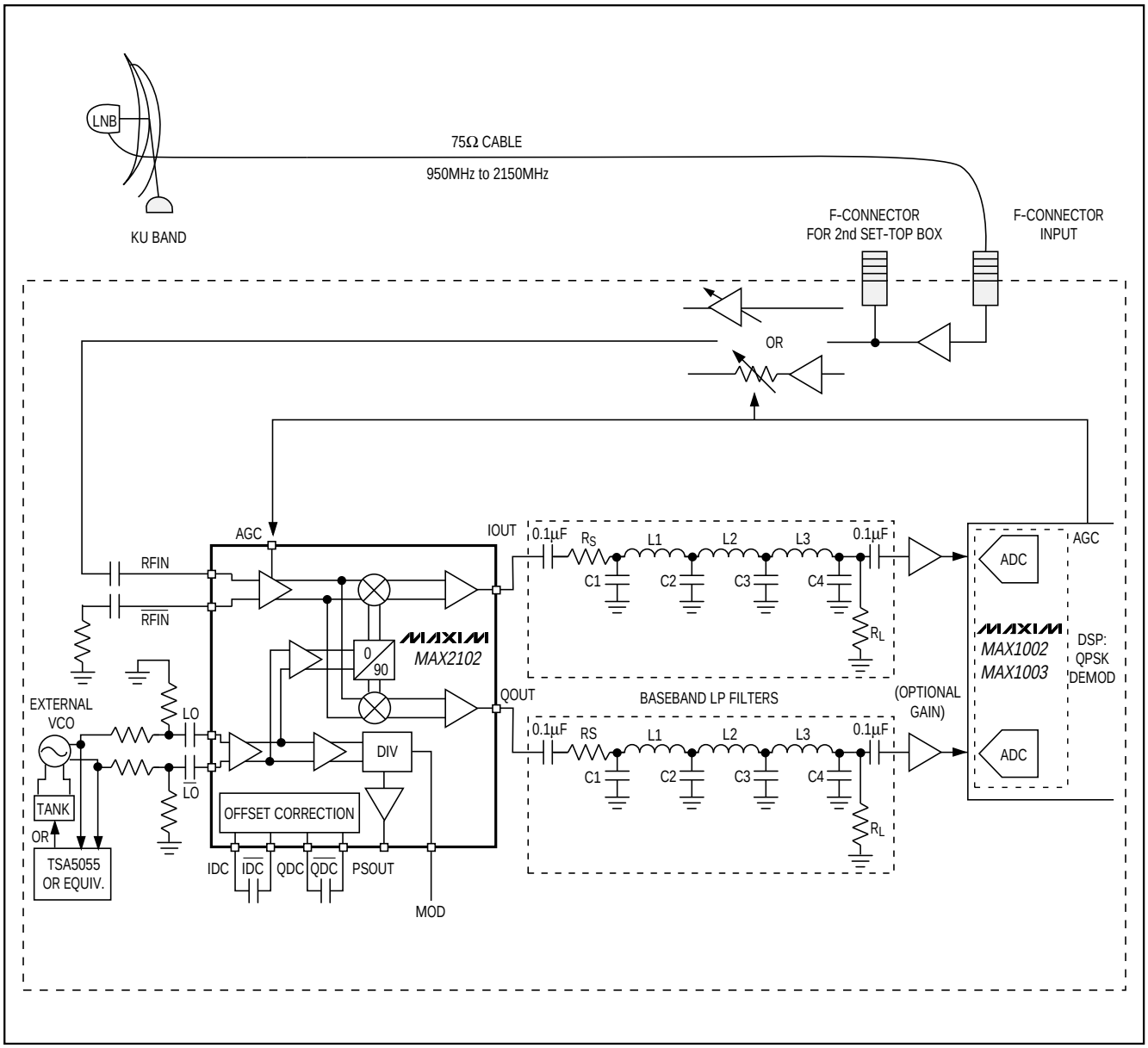


Figure 2. Typical Application

In some applications, a varactor-tuned preselection bandpass filter is added between the discrete LNA and the MAX2102. This is usually required only for very high-linearity tuners, such as those designed for SCPC (low-data-rate) applications. The filter provides a means of broadly filtering adjacent interferers, thus improving the intermodulation performance of the tuner. Additionally, the filter removes the RF interferer at twice the LO frequency, which would otherwise add to cochannel interference (the MAX2102 alone rejects this carrier to approximately 32.3dBc).

External Oscillator

Since the MAX2102 is a direct-conversion receiver, the external LO must tune to the same frequencies as the desired RF input signals.

The MAX2102 oscillator input port (LO, $\overline{LO}$) accepts either a single-ended or differential (balanced) LO signal. A differential LO offers reduced LO leakage to the RFIN port, as well as lower spurious downconversion levels of RF signals, which are at twice the LO frequency. Refer to Figure 3 for differential LO connections. For best performance, ensure that the LO and $\overline{LO}$ traces are symmetrical.

The LO drive levels should be maintained to within the specified limits. If the LO drive falls below the specified range, quadrature performance may be affected. Driving LO above the specified limits will cause a higher LO leakage level at RFIN; this may be acceptable in some applications. The MAX2102 offset-correction loop can withstand LO leakage levels corresponding to at least 0dBm of LO input power drive.

Prescaler

Typical stand-alone tuner applications will not use the MAX2102 prescaler function, but instead use a commercial synthesizer IC such as the Philips TSA5055, which has an internal prescaler. To disable the MAX2102 prescaler, disconnect the PSGND pin (leave open). The prescaler will cause an output spur in the baseband spectrum, to a level of about -20dBc (referred to 500mVp-p baseband output level), which may land within the desired signal bandwidth in some applications.

To use the MAX2102 prescaler, connect the PSGND pin to ground. In some applications, the prescaler may be toggled on and off using a MOSFET to switch PSGND to ground. PSGND should be forced to within

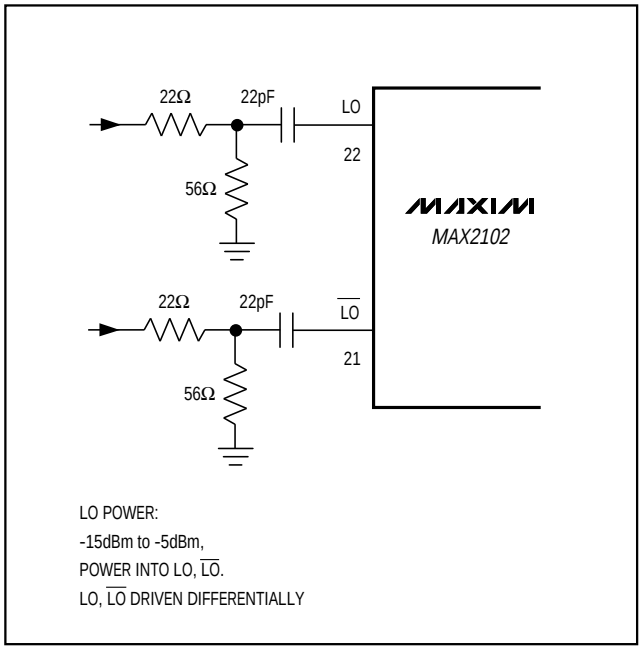


Figure 3. Differential LO Drive

100mV of ground, and the MOSFET must be capable of sinking 15mA. PSOUT is capable of driving a typical CMOS load of 10kΩ in parallel with 5pF. A 2kΩ pull-down resistor must be connected from PSOUT to GND.

The prescaler requires a stable level at the MOD pin 12ns before the falling edge of PREOUT to assert the desired modulus. The level at MOD must remain static until 3ns after this falling edge.

Baseband Amplifiers

The MAX2102 baseband amplifiers provide over 2Vp-p swing at IOUT and QOUT, and are capable of driving 100Ω. IOUT and QOUT must be AC-coupled to any lowpass filters. In a typical application, IOUT and QOUT drive a 5th- or 7th-order lowpass filter for ADC antialiasing purposes (see *Systems Considerations: Lowpass Filters in Direct-Conversion Tuners*). After the filters, in some cases, additional gain may be required. This can be accomplished with a pair of video-speed op amps, such as the MAX4216 dual video op amp. Alternatively, the MAX1002/MAX1003 dual ADC has built-in gain ahead of the ADCs, digitizing levels as low as 125mVp-p. Contact Maxim for more information about the MAX4216 or the MAX1002/MAX1003.

Direct-Conversion Tuner IC for Digital DBS Applications

Offset Correction

The internal offset-correction amplifiers remove the DC offsets present in the baseband amplifiers. The offset-correction loop effectively AC-couples the baseband signal path, yielding a -3dB highpass corner frequency according to the following:

$$f_{-3dB} = 100 / C_{DC} (\mu F)$$

where C_{DC} is the value of the capacitors, in microfarads, across QDC, $\overline{QDC}$ and IDC, $\overline{IDC}$.

For applications where the DC information must be maintained through the signal path, the offset correction can be disabled by connecting QDC, $\overline{QDC}$, IDC, and $\overline{IDC}$ directly to ground. Disabling the offset correction will effectively limit the input dynamic range of the MAX2102. Typical input dynamic range will be approximately -45dBm to -19dBm for single-ended LO drive, and -55dBm to -19dBm for differential LO drive.

Layout Considerations

Observe standard RF layout rules. A ground plane is essential; when connecting areas of ground plane between layers, use vias liberally. Remove the ground plane under the external VCO area to reduce parasitic capacitance. If a ground plane is used under the lowpass filters, note that the filter shape may be slightly offset due to parasitic capacitance.

In a direct-conversion receiver, LO leakage to the RF input connector is a major issue, since filtering of the LO is impossible (the LO operates at the same frequency as the RF input). The external VCO section should be housed in a separate shielded compartment, if possible. Use of a differential (balanced) LO will dramatically reduce LO leakage. Also, the use of coplanar waveguide transmission-line structures reduces LO leakage (used on the MAX2102 EV kit).

Observe the power-supply bypass capacitor connections in the *Pin Description* table, notably pins 1, 3, 4, 6, 9, 11, 12, 14, 19, 20, 23, and 24. Traces from these IC pins to the bypass capacitors must be kept to an absolute minimum. Where possible, make these connections on the top side of the board.

Minimize parasitic capacitance to ground around the offset-correction circuit (pins 15–18) by removing the ground plane beneath these pins and placing the offset-correction capacitors as close to the IC as possible.

The MAX2102 EV kit includes ferrite beads in series with power-supply leads. The beads may not be required for all applications.

Table 1. Suggested Component Values for Discrete Lowpass Filters (0.1dB Ripple Chebyshev Type)

ADC SAMPLING RATE (Msps)	FILTER TYPE	R_S (Ω)	C1 (pF)	L1 (nH)	C2 (pF)	L2 (nH)	C3 (pF)	L3 (nH)	C4 (pF)	R_L (kΩ)
40	0.1dB Chebyshev, f_C = 20MHz	100	39	910	120	1500	150	1500	120	10
60	0.1dB Chebyshev, f_C = 30MHz	100	22	620	82	910	100	1000	820	10
90	0.1dB Chebyshev, f_C = 45MHz	100	18	390	56	620	68	680	56	10

Note: Suggested types: inductors: Coilcraft 1008CS, tolerance = ±5%; capacitors: use tolerance = ±2%. Refer to Figure 2 for circuit diagram.

Power-Supply Sequencing

The MAX2102 has several +5V supply pins. The supply layout should be in a star format, with a bypass capacitor that dominates the rise time of the supply at the center of the star, to ensure that all pins see approximately the same voltage during power-up.

The prescaler V_{CC} (pin 28) must be connected to the same V_{CC} as the other V_{CC} pins, even if the prescaler is not used. Leaving PSGND open will disable the prescaler function and, in this state, the prescaler will not dissipate any power.

Systems Considerations: Lowpass Filters in Direct-Conversion Tuners

Typically, a 5th or 7th-order L-C lowpass filter is used for anti-aliasing the ADCs following the MAX2102. Figures 4 and 5 describe typical filtering requirements. Table 1 offers suggested component values for these lowpass filters.

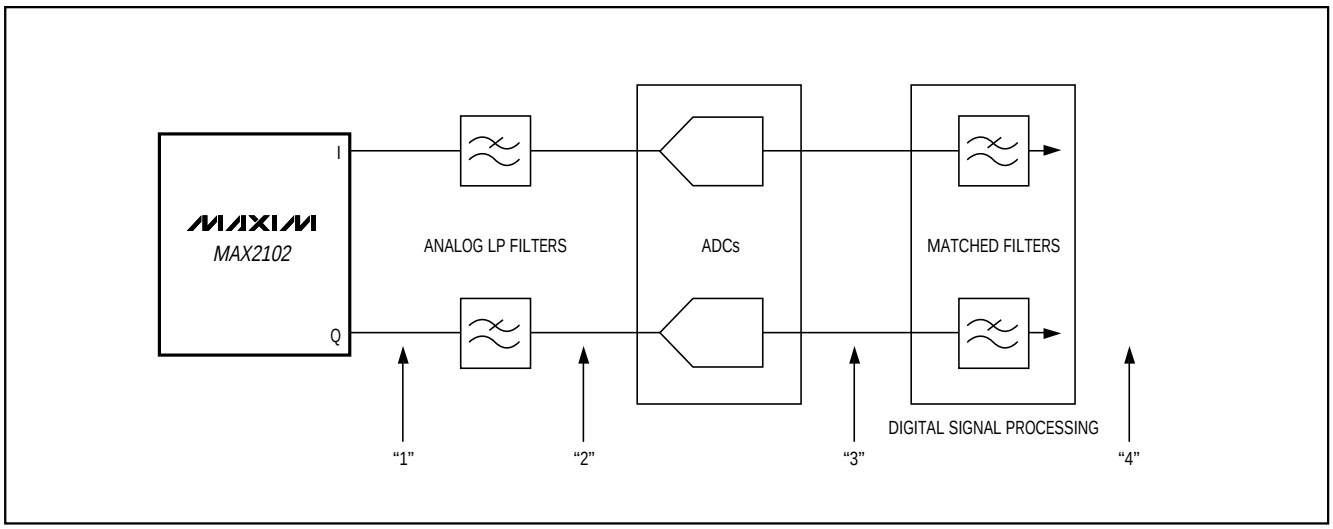


Figure 4. I, Q Signal Path

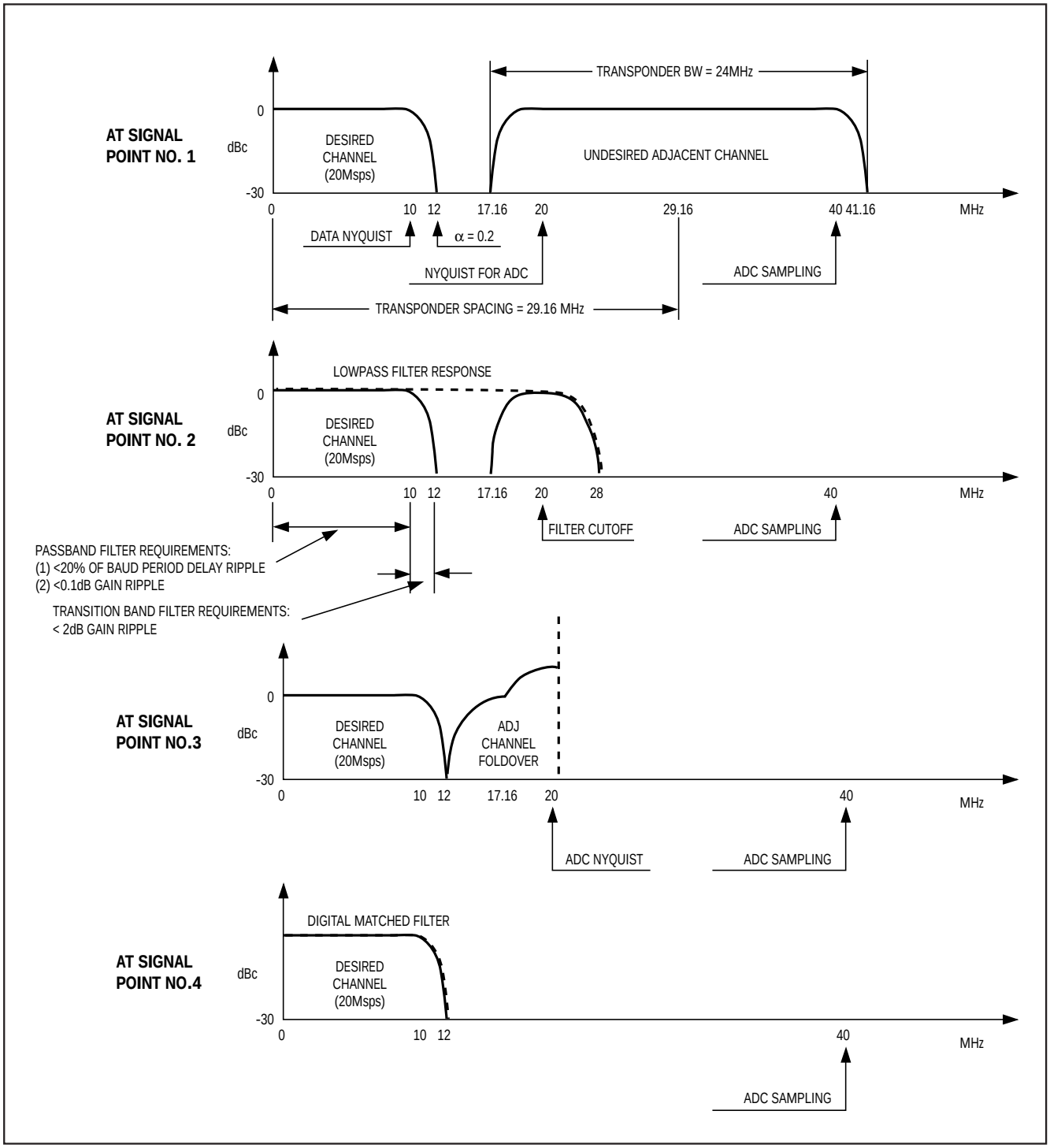
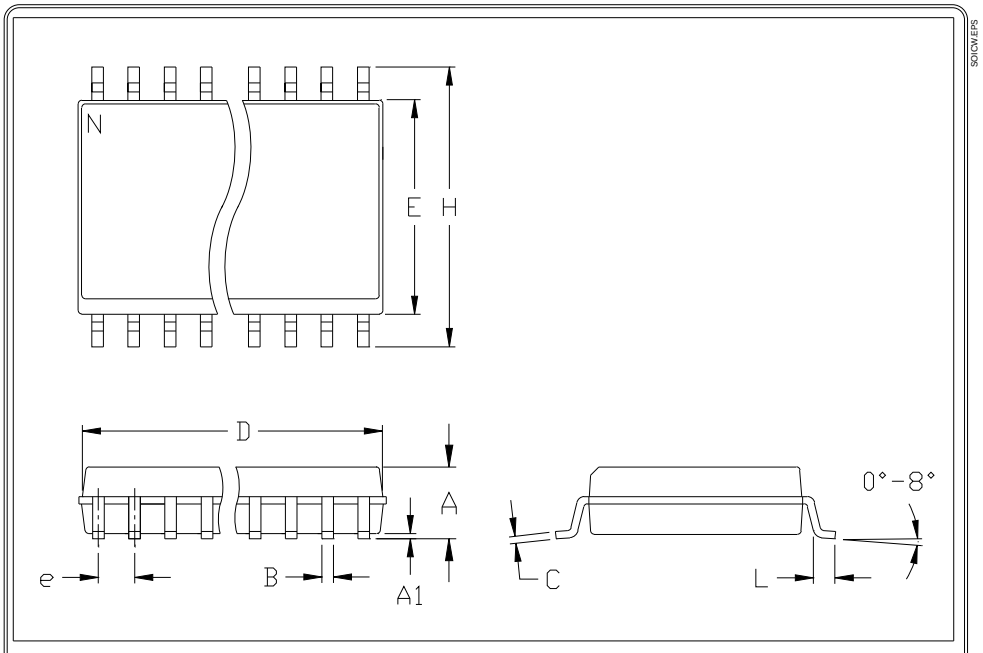


Figure 5. Lowpass Filtering Example Note: Data Rate = 40Mbps, Transponder BW = 24MHz, Transponder Spacing = 29.16MHz, Nyquist Filter: α = 0.2

Package Information



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS013-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM — 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: SOIC .300" — TITLE

1/1

21-0042 A — DOCUMENT CONTROL NUMBER REV

NOTES