

MAXIM

MAX1160 Evaluation Kit

General Description

The MAX1160 evaluation kit (EV kit) evaluates the performance of the MAX1160/MAX1161 monolithic, high-speed 10-bit analog-to-digital converters (ADCs). The ADCs must be ordered separately.

The MAX1160 and MAX1161 have a $\pm 2\text{V}$ analog input range and can digitize an analog input signal into 10-bit words at minimum update rates of 20MSPS and 40MSPS, respectively. The devices are pin compatible, and all input/output logic is TTL compatible.

EV Kit Applications

Evaluation of MAX1160/MAX1161

Engineering System Prototype Aid

Incoming Inspection Tool

Guide for System Layout

Features

- ♦ 20MSPS/40MSPS Conversion Rate
- ♦ On-Board Clock Drivers
- ♦ Data Output and Strobe Signal
- ♦ User-Selectable Capture Clock
- ♦ On-Board Reference Drivers

Ordering Information

| PART | TEMP. RANGE |
|---------------|--------------|
| MAX1160EVKIT* | 0°C to +70°C |

* Evaluates either MAX1160_CPI or MAX1161_CPI, which must be ordered separately.

Evaluates: MAX1160/MAX1161

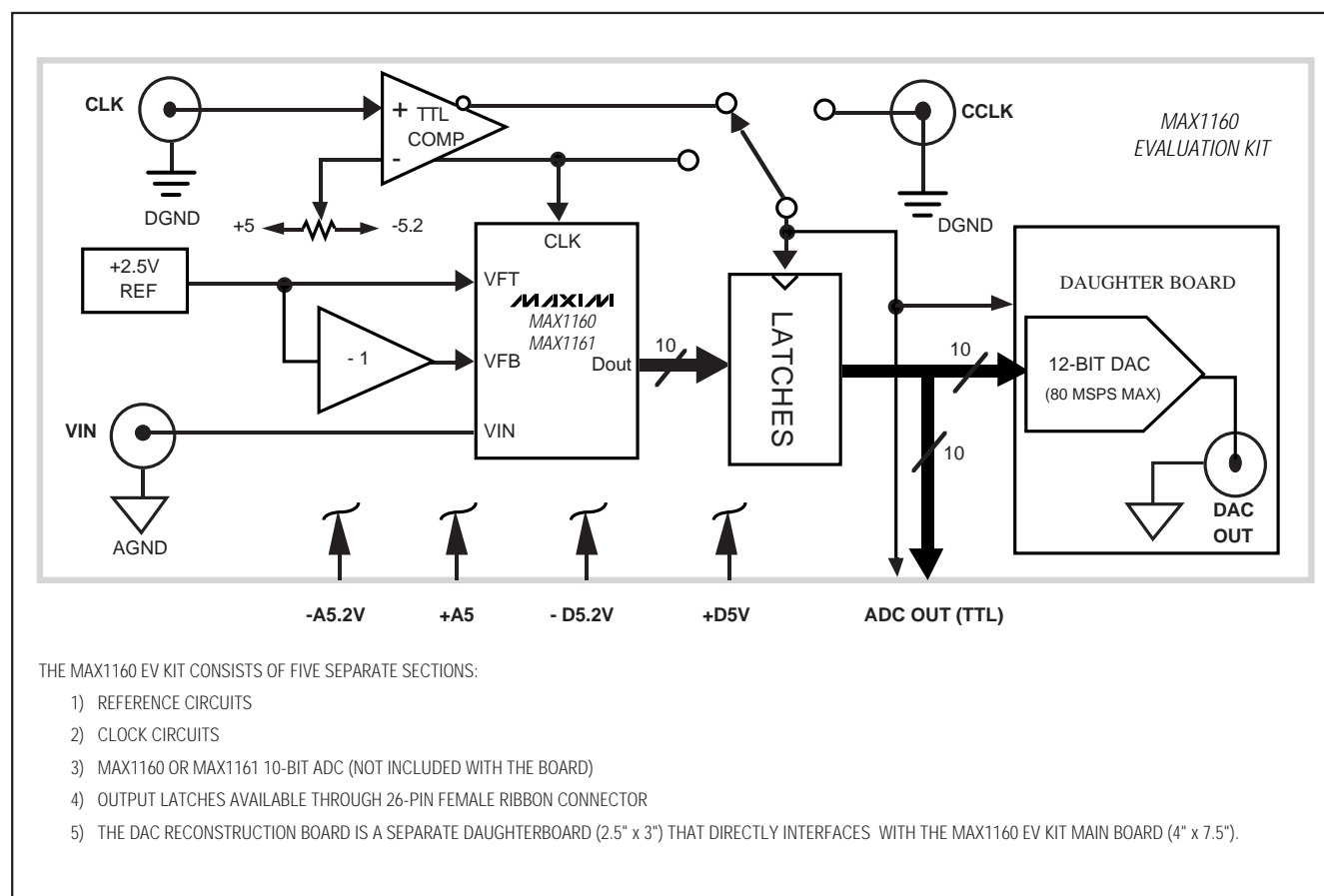


Figure 1. Functional Diagram

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MAX1160 EV Kit Component List

| DESIGNATION | QTY | DESCRIPTION |
|-----------------------------------|-----|---|
| C1–C7, C10 | 8 | 10 μ F, 25V, 0.10" tantalum capacitors |
| C20, C22–C28, C30, C31, C32 | 11 | 0.01 μ F chip capacitors |
| C21, C29 | 2 | 0.1 μ F chip capacitors |
| C50–C58 | 9 | 0.01 μ F, 10% ceramic capacitors |
| D1 | 1 | Lead-mounted hot-carrier diode |
| FB1, FB2, FB3 | 3 | Lead-mounted ferrite beads |
| P1 | 1 | 9-pin power connector Molex/09-18-5094 |
| P1/Receptacle | 1 | 9-pin power-connector, receptacle Molex/03-09-1093 |
| P2, P3 | 2 | Ribbon-plug connectors |
| PJ1, PJ2 | 2 | Probe connectors |
| R1, R2 | 2 | 10k Ω , 12-turns potentiometers |
| R3 | 1 | 2k Ω , 12-turns potentiometer |
| R10, R11, R12 | 3 | 51 Ω , 5%, 1/8W resistors |
| R20, R21 | 2 | 820 Ω , 5%, 1/8W resistors |
| R26, R27, R30 | 3 | 20k Ω , 5%, 1/8W resistors |

| DESIGNATION | QTY | DESCRIPTION |
|--------------------------------|-----|--|
| R28 | 1 | 1M Ω , 5%, 1/8W resistor |
| R32 | 1 | 5.1k Ω , 5%, 1/8W resistor |
| R33 | 1 | 10k Ω , 5%, 1/8W resistor |
| RN1, RN2 | 2 | 10k Ω , 708A-type 8-pin SIP resistors |
| TP1, TP2, TP3, AG, DG, STEP | 6 | 76 mil-diameter hole, test-point terminal |
| U1 | 1 | Device under test, 10-bit ADC |
| U2 | 1 | +2.5V precision voltage reference |
| U3 | 1 | Op amp, low noise |
| U5 | 1 | Single, fast TTL comparator, 8 DIP |
| U7, U8 | 2 | HEX D flip-flop, TTL, fast series |
| None | 3 | BNC connector |
| None | 8 | Crimp female terminal for P3 |
| None | 1 | Crimp male terminal for P3 |
| None | 4 | Nylon screw, 4-40, 3/16", round head |
| None | 4 | Nylon standoff, 1", round |
| None | 1 | SIP socket strip, 20SIP break-away |
| None | 1 | 28-pin DIP socket, 0.6" (U1) |

Daughterboard Component List

| DESIGNATION | QTY | DESCRIPTION |
|-------------|-----|--|
| C1, C2 | 2 | 10 μ F, 25V, 0.10" tantalum capacitors |
| C10–C16 | 7 | 0.1 μ F chip capacitors |
| C21–C25 | 5 | 0.1 μ F, 10% ceramic capacitors |
| D1 | 1 | 1.2V reference, 2-terminal IC |
| DB792 PCB | 1 | Printed circuit board |
| FB1, FB2 | 2 | Lead-mounted ferrite beads |
| P2, P3 | 2 | 26-pin, dual-row, vertical PCB-mount connectors |
| R1 | 1 | 10k Ω , 12-turns potentiometer |
| R2 | 1 | 7.5k Ω , 5%, 1/8W resistor |
| R3 | 1 | 22 Ω , 5%, 1/8W resistor |
| R4 | 1 | 10k Ω , 5%, 1/8W resistor |
| R5 | 1 | 15k Ω , 5%, 1/8W resistor |

| DESIGNATION | QTY | DESCRIPTION |
|-------------|-----|---|
| R6 | 1 | 20k Ω , 5%, 1/8W resistor |
| R7, R8 | 2 | 1k Ω , 5%, 1/8W resistors |
| R11, R12 | 2 | 150 Ω , 5%, 1/8W resistors |
| R20, R21 | 2 | 820 Ω , 5%, 1/8W resistors |
| R22 | 1 | 200 Ω , 5%, 1/8W resistor |
| TP1, AG, DG | 3 | 76-mil-diameter hole, test-point terminals |
| U9 | 1 | 100MHz, 12-bit TTL DAC |
| U10 | 1 | Low-noise op amp |
| U11 | 1 | Low-distortion op amp |
| None | 1 | BNC connector |
| None | 1 | Crimp male terminal for P3 |

MAX1160 Evaluation Kit

Evaluates: MAX1160/MAX1161

Detailed Description

Power Supplies

The MAX1160 evaluation kit (EV kit) requires four power-supply sources: analog -5.2V (-A5.2V), analog +5V (+A5V), and digital -5.2V (-D5.2V), and digital +5V (+D5V). P1 is the power connector. (See Figure 2.) Table 1 shows the recommended operating voltage range.

Power-Supply Hookups

Power Supplies and Grounding

The MAX1160/MAX1161 require two analog supply voltages: -A5.2V and +A5V. The +A5V supply is common to analog VCC (pins 18 and 25) and digital DVCC (pins 14 and 28). A ferrite bead in series with each supply (RF1 and RF2) reduces the transient noise injected into VCC. The bead (RF1 or RF2) to MAX1160/MAX1161 connections should not be shared with any other device. Bypass each power-supply pin as closely as possible to the device (0.1μF to AGND for each VEE and VCC pin and 0.01μF to DGND for the DVCC pin).

Total power dissipation is typically 1.9W, including the MAX1160/MAX1161 (1.1W typ).

Table 1. Recommended Power-Supply Operating Range

| POWER SUPPLY (V) | MIN (V) | TYP (V) | MAX (V) | TYP CURRENT (mA) |
|------------------|---------|---------|---------|------------------|
| -A5.2 | -4.95 | -5.20 | -5.45 | 60 |
| +A5 | +4.75 | +5.00 | +5.25 | 240 |
| -D5.2 | -4.95 | -5.20 | -5.45 | 15 |
| +D5 | +4.75 | +5.00 | +5.25 | 60 |

Table 2. Pin Assignments

| PIN | DESCRIPTION |
|-----|-------------------------------|
| 1 | Analog -5.2V |
| 2 | Analog -5.2V Return #1 (AGND) |
| 3 | Analog -5.2V Return #2 (AGND) |
| 4 | Analog +5V |
| 5 | Analog +5V Return (AGND) |
| 6 | Digital -5.2V Return (DGND) |
| 7 | Digital +5V |
| 8 | Digital +5V Return (DGND) |
| 9 | Digital -5.2V |

AGND and DGND are isolated on the MAX1160/MAX1161. Both -A5.2V and +A5V are the analog supply sources. As with most very-high-speed analog-to-digital converters (ADCs), grounding is critical. Therefore, the ground-plane technique is the one most desirable for the MAX1160/MAX1161. To use this method, split the AGND and DGND planes and tie them together at the device through an RF bead. The MAX1160 EV Kit has four layers: top signal, ground (AGND and DGND) planes, power plane, and bottom signal. The two ground planes are connected at the device through a ferrite bead (RF3). All three ferrite beads (RF1, RF2, RF3) are located close to the ADC.

Reference Circuit

The MAX1160/MAX1161 requires the use of two voltage references: VFT and VFB. VFT (+2.5V typ) is the force for the top of the voltage-reference ladder, and VFB (-2.5V typ) is the force for the bottom. Both voltages are applied across an internal 900Ω reference ladder. In addition, there are three reference-ladder taps: VST,

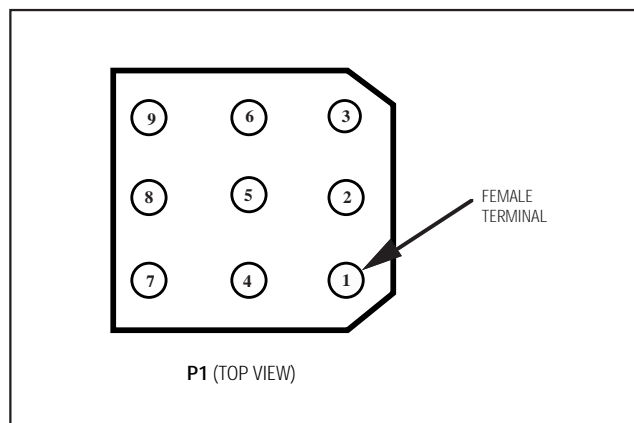


Figure 2. P1 Power-Supply Connector's Pin Assignment

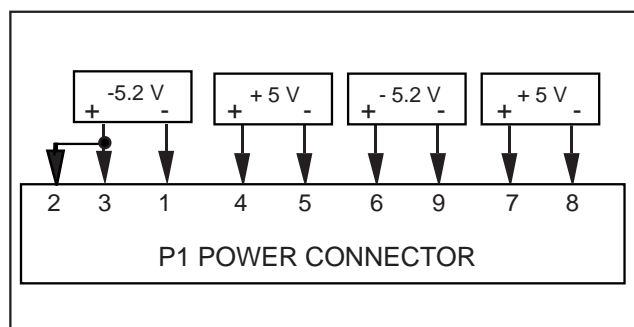


Figure 3. P1 Connector/Hookup

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VRM, and VSB. VST is the top of the reference-ladder tap (+2V); VRM is the middle point (0.0V typ); and VSB is (-2V). The voltages at VST and VSB are the full-scale input voltages expected of the device when VFT and VFB are driven to the recommended voltages (+2.5V and -2.5V, respectively). Use VST and VSB to monitor the actual full-scale input voltages ($\pm 2V$) by adjusting VFT and VFB (Table 3). These adjustments interact with one another; repeat them as needed until VST and VSB settle at the desired voltages. Do not drive VRM as is commonly done with a standard flash ADC converter. When not being used, decouple VST, VRM, and VSB with a 0.01 μF , surface-mount chip capacitor from each tap to AGND, to minimize high-frequency noise injection.

As shown in Figure 17, U2 is the +2.5V reference with $\pm 150mV$ of adjustable range (R1 potentiometer). U3 is an inverting amplifier. Its tolerance is 5% with $\pm 300mV$ of adjustable range (R2 potentiometer). Maxim recommends that VFT and VFB be operated to within $\pm 2\%$ (or $\pm 2.5V \pm 50mV$) to maintain accuracy within the specified limit. Before each MAX1160 EV kit board is shipped, VFT and VFB are adjusted to $\pm 2.5V$ ($\pm 5mV$), respectively. For each new MAX1160/MAX1161, readjust VST and VSB. All measurements must be referenced to the AGND test point. (See Table 3.)

Table 3. Reference Adjustment

| | VST | VSB |
|------------|------------|------------|
| Test Point | U1, pin 20 | U1, pin 23 |
| Min | 1.95V | -2.05V |
| Typ | 2.00V | -2.00V |
| Max | 2.05V | -1.95V |
| Adjust | R1 | R2 |

NOTE: The MAX1160/MAX1161 (especially reference taps VFT, VFB, VST, and VRM) are sensitive to electrostatic discharge (ESD).

Table 4. Output Coding

| ANALOG INPUT | D12 (OVERRANGE BIT) | DATA OUTPUT CODE |
|-------------------|---------------------|------------------|
| $< -2.0V$ | 0 | 00 0000 0000 |
| $-2.0V + 1LSB$ | 0 | 00 0000 0000 |
| 0V | 0 | 00 0000 0000 |
| $+2.0V - 1LSB$ | 0 | 11 1111 1110 |
| $> 2.0V + 1/2LSB$ | 1 | 11 1111 1111 |

NOTE: 0 indicates the flickering bit between logic 0 and 1.

Figure 4a shows one type of reference driver. Figure 4b shows another way to drive the reference circuits using force and sense. The alternate circuit provides better control of plus full-scale (+FS) and minus full-scale (-FS) errors by sensing VST and VSB to $\pm 2.0V$, respectively. VST and VSB are high-impedance nodes, requiring additional precaution when routing (PCB layout).

MAX1160/MAX1161 ADCs

The MAX1160 is a 10-bit ADC capable of digitizing an input signal with a 20Msps minimum update rate. The MAX1161 is pin compatible with the MAX1160, except it is faster: the sampling frequency is 40Msps. On both devices, the expected full-scale analog input range is from VST to VSB. The analog input is latched at CLK's leading edge. There are 11 digital TTL outputs. D0–D9 are the parallel TTL output bits, with D0 the least significant bit (LSB), D9 the most significant bit (MSB), and D10 the overrange bit. The data outputs are latched at CLK's rising edge, with a 14ns propagation delay. There is one clock latency between CLK and valid output data (Figure 5). The output code is straight binary.

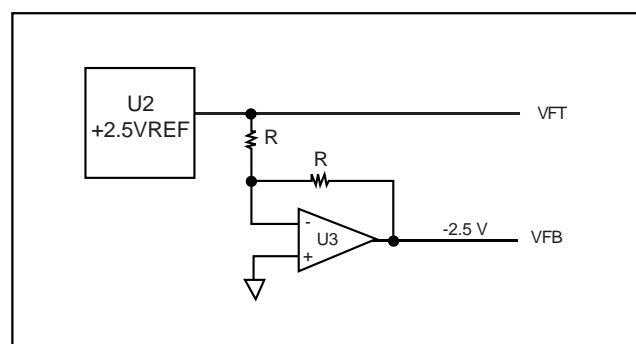


Figure 4a. Reference Driver

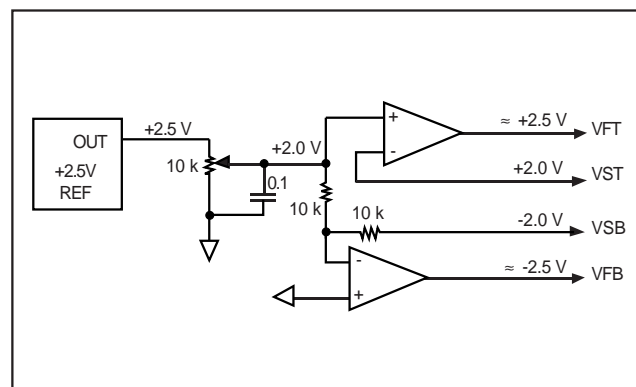


Figure 4b. Alternative Reference Driver

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Pin 21 is the analog input pin. Selecting the analog input driver for the MAX1160/MAX1161 is simpler than with most flash ADCs because the input impedance and input capacitance are typically $300k\Omega$ and $5pF$, respectively. For example, at $10MHz$ and $4Vp-p$ sine-wave input, the input driver source requires only $0.648mA$ of peak output current ($4\pi FC$).

The analog input is fed directly from a BNC (VIN). R10 (51Ω) is the analog input source termination mounted on a socket as a user-selectable termination. The analog input pin has no circuit protection. Its maximum rating is from VFT to VFB ($\pm 2.5V$). Use a voltage limiter to protect the input pin from permanent damage in applications with an analog input range greater than $\pm 2.5V$. (See the *Input and Latchup Protection* section.)

Input Clock Driver

CLK is the single-ended input clock to the MAX1160 EV kit; CLK IN is the input clock to the ADC; and CCLK is the capture clock used for the output latches (U7 and U8).

The MAX1160/MAX1161's clock input requires a TTL-logic level of $6ns$ or faster to reduce the noise. Fast TTL-family components (74FXX) fit well in this application. Finding a square-wave generator (TTL logic up to $40MHz$, fast slew

rate, and low jitter) is more difficult than finding a sine-wave, low-jitter generator. U5 (MAX9686, TTL-voltage comparator) provides most of the above requirements for driving the ADC (except the low-jitter generator). The CLK signal should be a sine-wave signal with an amplitude not to exceed $\pm 3V$ (input common-mode limitation of U5). R11 (51Ω) is the CLK source termination. Use R3 to adjust the CLK IN duty cycle. CLK IN is in phase with CLK and has a $6ns$ typical propagation delay. Due to the internal track/hold amplifier (THA), keep the positive clock (CLK IN) pulse width from $10ns$ to $300ns$ for the MAX1161 and from $20ns$ to $300ns$ for the MAX1160. When operating the ADC faster than $3Msps$, keep the clock duty cycle at approximately $50\% \pm 10\%$. Probe jack PJ1 is the monitoring test point for CLK IN. Use this test point when adjusting the clock duty cycle.

A falling edge at CLK IN (pin 17) causes the internal THA to go into track mode. Keep the MAX1160/MAX1161 in track mode at start-up or when the device is idle for an extended period of time. This setup prevents the internal THA from going into saturation due to droop. The EV kit provides a logic low to the ADC clock when the pulse generator (CLK) is removed from the evaluation board.

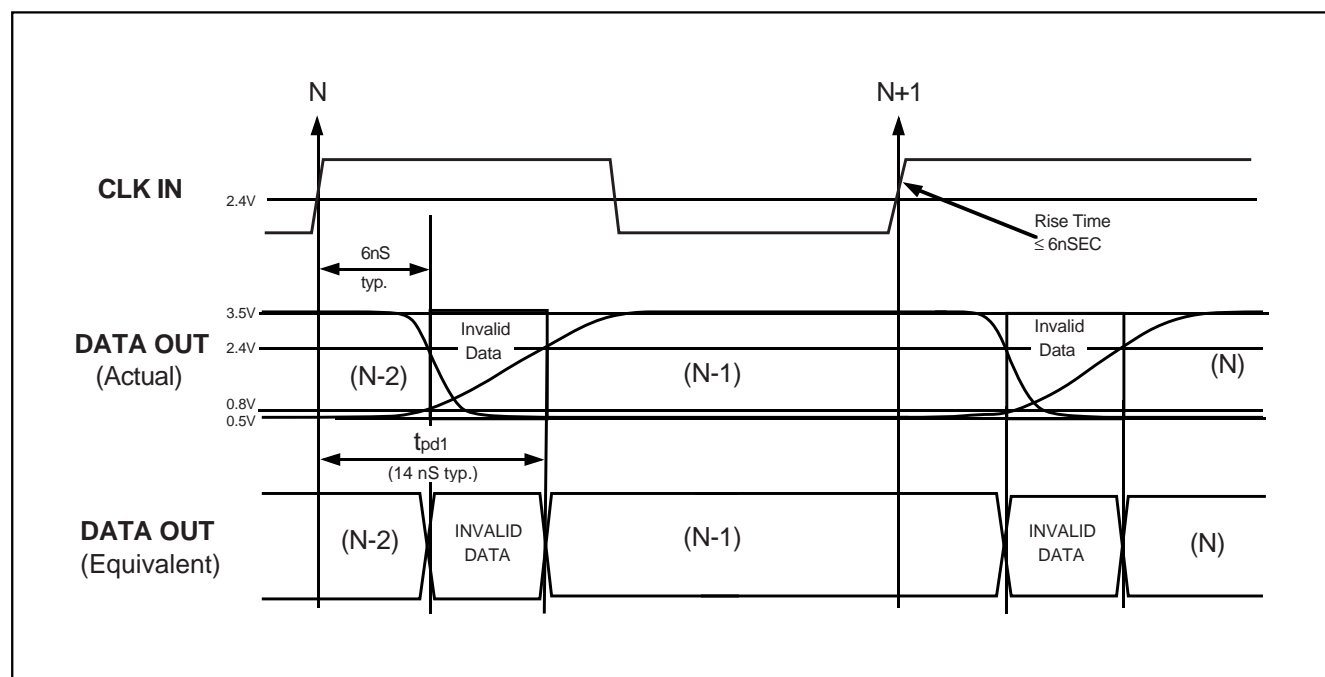


Figure 5. Digital Output Characteristic of the MAX1160/MAX1161

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TTL-Output Data Latches

The ADC's rise time (t_{RISE}) and fall time (t_{FALL}) are not symmetrical. The propagation delay, with respect to t_{RISE} at the 2.4V crossing, is typically 14ns; with respect to t_{FALL} at the 2.4V crossing, it is typically 6ns. Figure 5 shows the output characteristic of the MAX1160/MAX1161. The nonsymmetrical nature of the output creates approximately 8ns of invalid data.

In applications using a reconstruction DAC, the invalid data zone causes an unwanted glitch in the reconstruction signal if the DAC is directly interfaced with the MAX1160/MAX1161. To avoid this, buffer the ADC with edge-triggered latches.

U7 and U8 (74F174) are the output latches. The fast family TTL logic is very sensitive to electrostatic discharge (ESD). RN1 and RN2 are the 8-pin, 10k Ω SIP resistor networks. They protect U7 and U8 by providing the ESD path to DGND. The BNC connector (CCLK) is the capture clock, which has 51 Ω termination R12 on board. The data latches' outputs (D0–D9) are routed through the standard 26-pin female ribbon connector

(P2). SJ3, SJ4, and SJ5 are the solder-jumper options for the capture clock. **Only one of these jumpers must be connected:**

- When SJ3 is installed (as shipped from the factory), the ADC and the latches (U7 and U8) are clocked at the same time. With this configuration, the data seen at connector P2 contains another clock cycle of latency (a total of two cycles of latency, as shown in Figure 6).
- When SJ4 is installed, the capture clock must be supplied externally through CCLK. The setup time (t_s) and hold time (t_h) shown in Table 6 must be met when selecting this option.
- When SJ5 is installed, the buffers are latched at the falling edge of the CLK IN (MAX1160/MAX1161). With this option, the t_s and t_h requirements for the 74F174 latches must be met (Table 6). The placement of this capture clock edge is dependent on the clock pulse width and the sampling frequency. This option is not recommended above 25Msps.

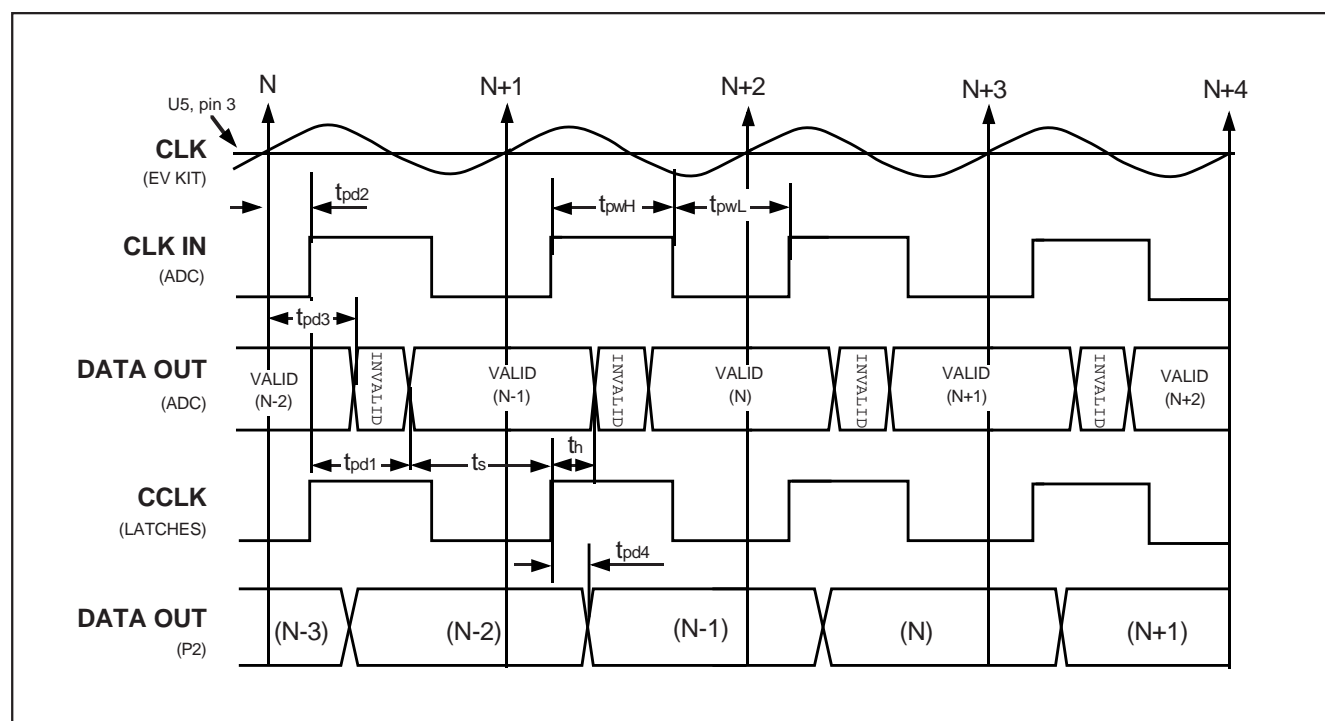


Figure 6. MAX1160 EV Kit Timing Diagram, CCLK = CLK IN

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Table 5. P2, Latched Output Data, 26-Pin Female Ribbon Connector

| P2 | FUNCTION | LOGIC | P2 | FUNCTION | LOGIC |
|----|----------|-------|----|----------|-------|
| 1 | CCLK | TTL | 14 | DGND | DGND |
| 2 | DGND | DGND | 15 | D4 | TTL |
| 3 | TTL/LOW | TTL | 16 | DGND | DGND |
| 4 | DGND | DGND | 17 | D5 | TTL |
| 5 | TTL/LOW | TTL | 18 | DGND | DGND |
| 6 | DGND | DGND | 19 | D6 | TTL |
| 7 | D0 (LSB) | TTL | 20 | DGND | DGND |
| 8 | DGND | DGND | 21 | D7 | TTL |
| 9 | D1 | TTL | 22 | DGND | DGND |
| 10 | DGND | DGND | 23 | D8 | TTL |
| 11 | D2 | TTL | 24 | DGND | DGND |
| 12 | DGND | DGND | 25 | D9 (MSB) | TTL |
| 13 | D3 | TTL | 26 | DGND | DGND |

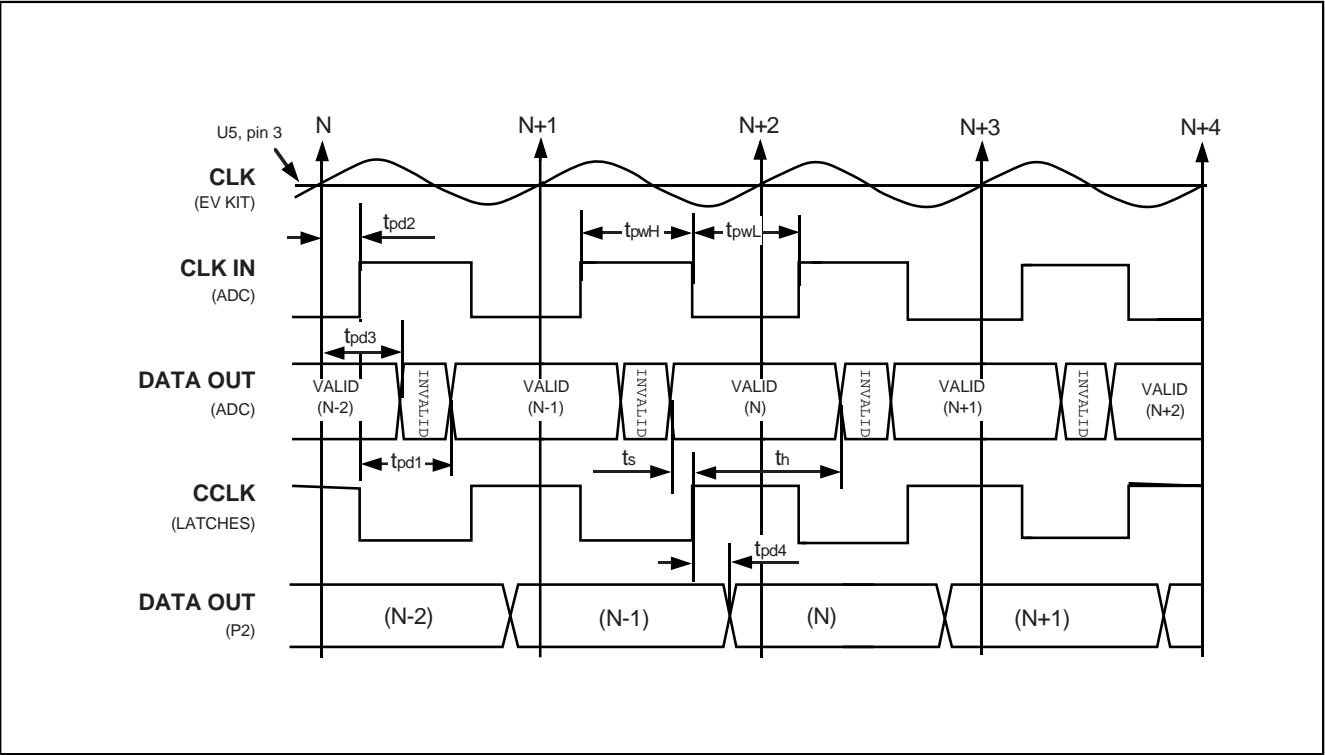


Figure 7. MAX1160 EV kit Timing Diagram , CCLK is 180° Out-of-Phase from CLK IN

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The latched digital outputs are routed through P2 (a 26-pin ribbon connector) (Table 5). The overrange bit (D10) can be viewed through test point TP3. D10 is not brought out through P2.

Acquisition-Time Specification

The acquisition time (t_{ACQ}) is defined as the hold-to-track, full-scale settling time for the internal THA. The clock input's logic low corresponds to track mode, and logic high is the hold mode for the internal THA. Figure 8 shows two types of acquisition time:

- T_{ACQ1} is the THA's settling time when it is in track mode and it is driven by the analog input switching.
- T_{ACQ2} is the amount of time it takes for the ADC's internal THA to reacquire the analog input when switching from hold to track (CLK IN from high to low), to within 1/2LSB.

Both T_{ACQ1} and T_{ACQ2} need the same amount of time (see the acquisition-time specification in the corresponding data sheet).

Place the low-to-high clock transition after both the analog input and the internal THA are settled. The analog

input must remain for at least 5ns (V_{IN} hold time) after the low-to-high clock transition. Keep the clock's positive pulse width (t_{pWH}) to within the recommended limit. (Refer to the specification in the corresponding data sheet.)

Timing Considerations

When Using an External Track/Hold

The signal-to-noise ratio (SNR) and the total harmonic distortion (THD) degrade as the analog input frequency increases. These parameters imply that the differential nonlinearity (DNL) and the integral nonlinearity (INL) degrade as well at high frequency. These degradations are mainly due to aperture jitter, analog input bandwidth limitation, and/or the ADC's slew-rate limitation. Below 1MHz, the MAX1160/MAX1161's SNR and THD are generally constant. To bring these accuracies up at high frequency, you might need to buffer the analog input using a THA.

The timing diagram shown in Figure 9 and the timing specifications listed in Table 7 address the critical timing necessary when driving the ADC from an external THA.

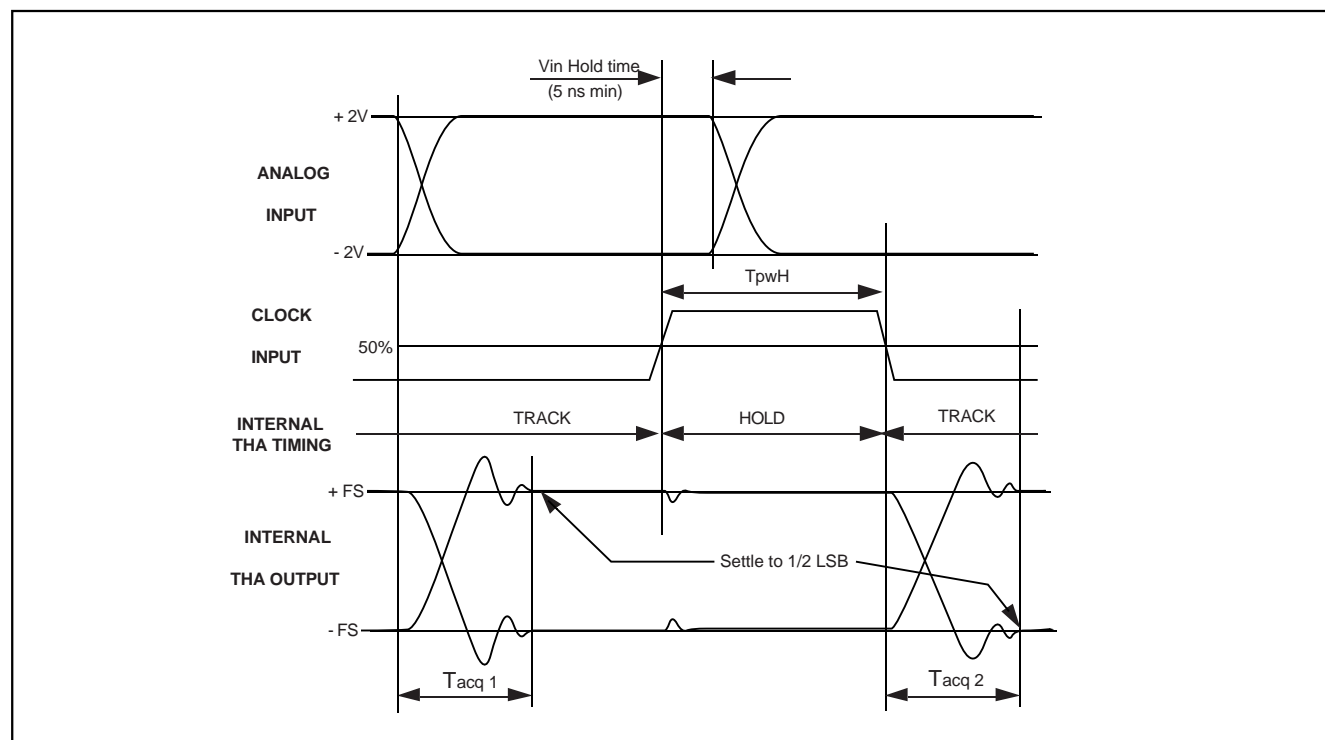


Figure 8. Acquisition Time

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Table 6. Timing Specification

| FUNCTION | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-----------|--|-----|-----|-----|------|
| t_{PD1} | MAX1160/MAX1161, CLK to Data Valid Propagation Delay | — | 14 | 18 | ns |
| t_{PD2} | MAX9686 Propagation Delay | — | 6 | 9 | ns |
| t_{PD3} | MAX1160/MAX1161, t_{FALL} Propagation Delay | 4.5 | 7 | 10 | ns |
| t_{PD4} | 74F174 Propagation Delay | 4.5 | 7 | 10 | ns |
| t_S | 74F174 Setup Time | 4.0 | — | — | ns |
| t_H | 74F174 Hold Time | 4.0 | — | — | ns |
| t_{PWH} | CLK Positive Pulse Width (MAX1160) | 20 | — | 300 | ns |
| t_{PWL} | CLK Negative Pulse Width (MAX1160) | 20 | — | — | ns |
| t_{PWH} | CLK Positive Pulse Width (MAX1161) | 10 | — | 300 | ns |
| t_{PWL} | CLK Negative Pulse Width (MAX1161) | 10 | — | — | ns |

Table 7. Critical Timing Specifications

| PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-----------|--|-----|-----|-----|------|
| t_{HTS} | THA, hold-to-track settling time | X | X | X | |
| t_{THS} | THA, track-to-hold settling time | X | X | X | |
| t_{ACQ} | ADC, acquisition time, 4V step | | 20 | | ns |
| t_{ACQ} | ADC, acquisition time $\leq 0.5V$ step | | 12 | | ns |
| t_{H1} | Hold time after the ADC rising clock | 5 | | | ns |

X = This limit depends on the THA chosen.

The settling time to 1/2LSB (1.953mV) is one of the principal requirements in a 10-bit THA. This includes both track-to-hold (t_{THS}) and hold-to-track (t_{HTS}) settling time. t_{HTS} varies with the step size (voltages) that the THA needs to swing. Place the ADC clock's rising edge after t_{THS} has settled. The MAX1160/MAX1161 require that the analog input be held for an additional 5ns (min) (t_{H1}) after the clock's rising edge. Figure 9 shows the ADC running at Nyquist; the sampling frequency is nearly twice the input frequency. In this example, the

ADC could have as much as a 4V step ($\pm FS$) from one conversion to the next. The acquisition time (t_{ACQ}) of the ADC must be met.

t_{ACQ} is the time necessary to allow the internal THA to track (CLK = low) and settle to 1/2LSB while the input changes to its new continuous level. The minimum acquisition time is 20ns for a 4V step and 12ns for a 0.5V or less step.

Being driven from an external THA, the ADC's maximum sampling rate can be determined from the combination of t_{THS} , t_{HTS} , and t_{ACQ} .

The pedestal and the droop of the THA shown in Figure 9 are not critical to the dynamic performance as long as they are constant with respect to the analog input range. They are seen as offset errors.

Low-Level Analog Input Signal

The MAX1160/MAX1161 require that the analog input (VIN) range be operated within $\pm 2V \pm 2\%$. Amplification and level shifting are necessary for a low-voltage-level VIN.

Figure 10 shows the typical analog driving circuit. AMP1 and AMP2 are optional. For applications in which noise is the major concern, use AMP1 (disregard AMP2) low-noise amplifier to gain up to $\pm 2V$ before getting to the THA. In other applications in which high-frequency VIN is the major concern, use AMP2 instead of AMP1 to amplify the THA signal to $\pm 2V$ before reaching the MAX1160/MAX1161. In the latter case, the low-level VIN provides a faster acquisition time for the THA.

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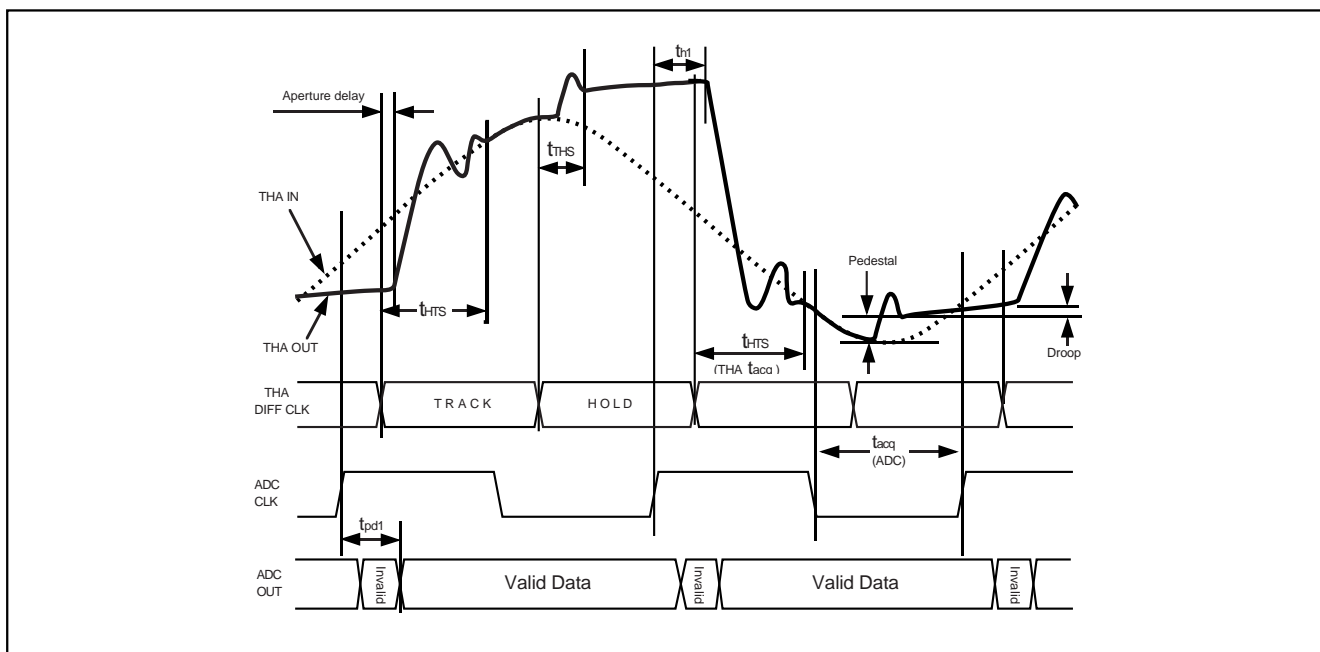


Figure 9. Critical Timing Between External THA and ADC

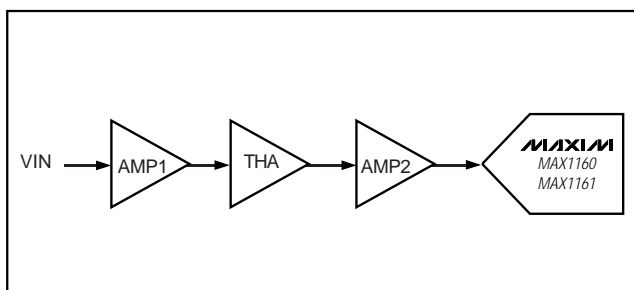


Figure 10. Driving Circuit Block Diagram

Uncommitted Prototype Space

Two areas are available for applications where additional circuits may be needed to interface with the MAX1160 EV kit (Figure 17). These two areas (labeled A and D in the PCB assembly) are electrically non-committed:

- Area A is located near VIN (BNC), and is intended for the analog interfacing circuit. It has one 16-pin DIP and one 8-pin SIP.
- Area D is located between P2 and P3, and is intended for the digital interfacing circuit. It has three 16-pin DIPs, three 8-pin SIPs, and one 37-pin D connector.

Both areas have the appropriate power supplies and grounds.

Daughterboard (Reconstruction DAC)

Figure 18 illustrates the daughterboard that interfaces directly to the MAX1160 EV kit main board via P2 and P3. It is suited for applications in which the reconstruction DAC is needed to evaluate ADC performance in the time domain. It is designed around a 12-bit TTL, digital-to-analog converter with an 80MSPS update rate, set up in bipolar operation. Figure 18 shows the detailed schematic.

Input and Latchup Protection

The MAX1160/MAX1161 are free from latchup when the recommended interfacing circuit is used (Figure 11).

The following information was considered in developing the interface circuit used in the MAX1160 EV kit:

- 1) Drive the input clock (pin 15) from a TTL logic source ($V_{IH} \leq 4.5V$). Fast TTL-logic family or equivalent is strongly recommended due to its fast rise time (6ns or faster). If the clock is driven from a high-current source (greater than 400mA), use a 100Ω resistor in series to current limit to roughly 45mA.
- 2) D1 is a Schottky or hot carrier diode (Motorola, 1N5817, or equivalent) installed between V_{EE} and AGND (reverse bias).

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- 3) Both VCC (pins 18 and 25) and DVCC (pins 14 and 28) are driven from the same +A5V supply.
- 4) Mount the ferrite beads (FB1 and FB2) as close to the device as possible. The bead to ADC connections should not be shared with any other device.
- 5) Bypass all reference and power-supply pins as close to the device pin as possible (chip capacitors C1–C11 are preferred: 0.1μF for VCC and VEE, and 0.01μF for DVCC and VREF).
- 6) The top reference (VFT) driver must be current limited to 20mA (max) if a different reference-driver circuit is used in place of the recommended circuit (Figure 11).
- 7) The limiter is required if the analog input's maximum peak-to-peak voltage exceeds ±2.5V. Incorporate this limiter within the analog input driver, or use the circuit shown in Figure 12. Another option is to add a 100Ω resistor in series to current limit the input. This last option adds another LSB error to both plus and minus full scale, compared to only 1/2LSB when using the circuit shown in Figure 12.

Evaluates: MAX1160/MAX1161

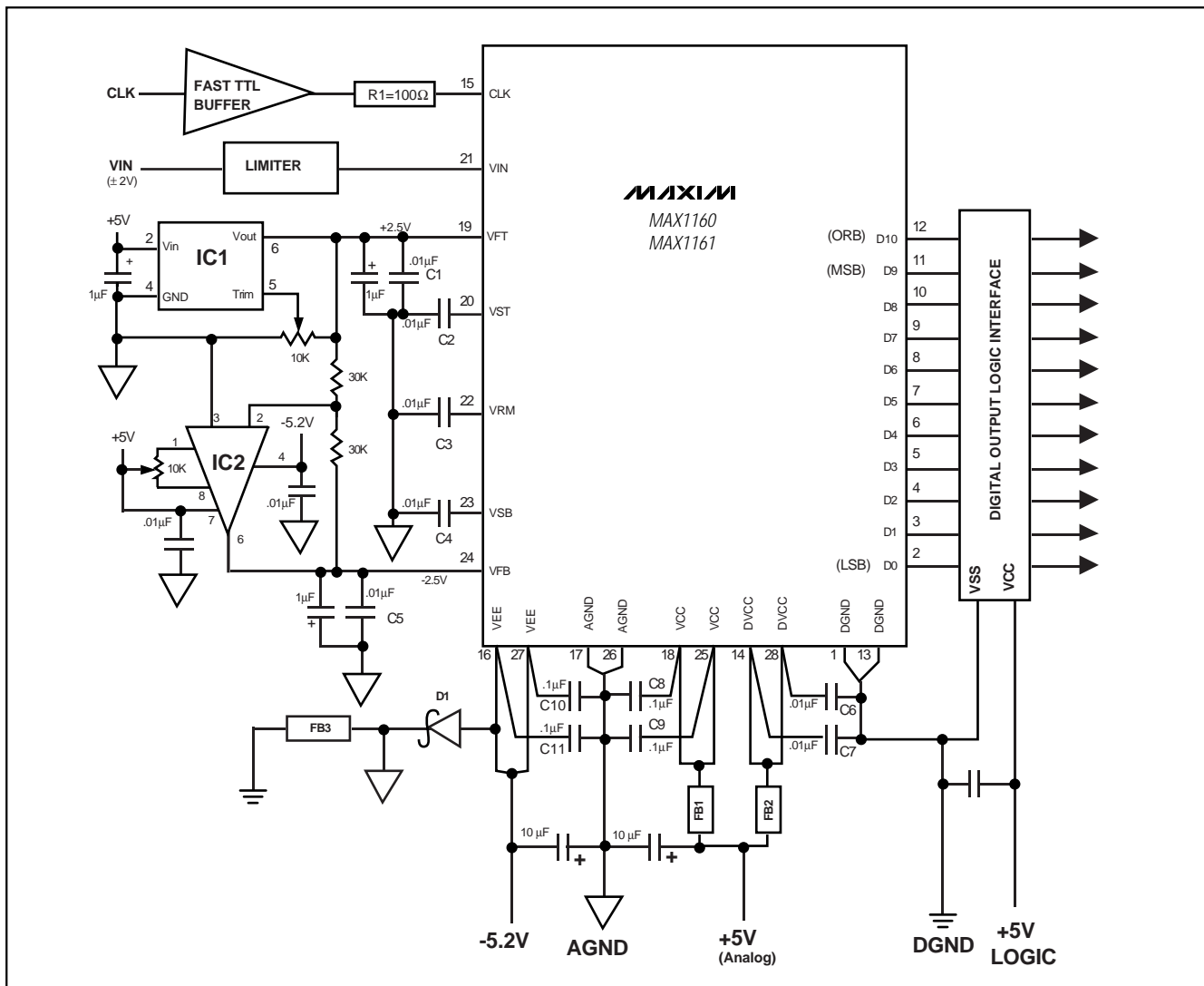


Figure 11. Typical Interfacing Circuit

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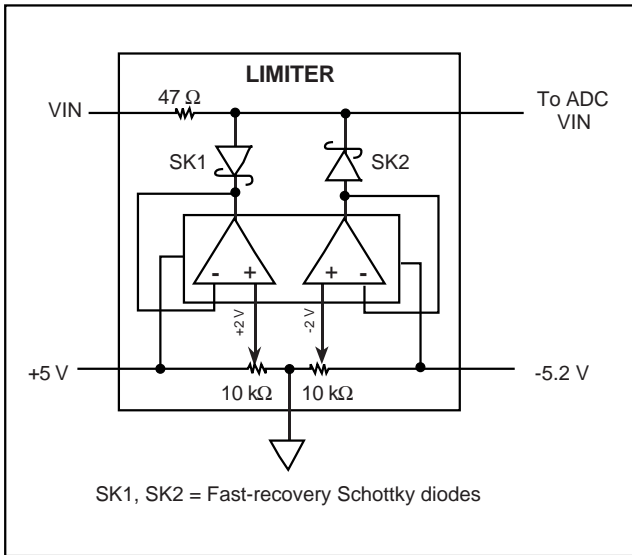


Figure 12. An Example of an Input Limiter

Characterization

Performance at speed is the main goal in evaluating any ADC, but it is beneficial to start from a relatively low speed and verify key parameters. It is also beneficial to predict performance at speed. If the device is noisy and/or has poor differential linearity at low frequency, the signal-to-noise ratio (SNR) at speed cannot be expected to be better. In addition, the low-frequency setup can be useful as a verification tool for the test setup.

At low frequency, there are numerous ways of characterizing the differential nonlinearity (DNL), integral nonlinearity (INL), transition noise, synchronous noise, non-monotonicity, power-supply sensitivity, and power-supply currents.

The missing-codes test, INL, DNL, and the gain-error tests are based on statistical results. They can be performed using the histogram technique. SNR and THD are tested by using the fast-Fourier transform (FFT) method.

The MAX1160 EV kit was designed to provide optimum capability in fulfilling the above characterization needs.

Equipment Hookup and Testing

Synchronous testing is recommended in characterizing the MAX1160/MAX1161. These testing techniques significantly reduce testing time (especially dynamic testing). In Figure 13, all three signals (VIN, CLK, and CCLK) are synchronized. Generator 1 is the analog input. Generator 2 is the sampling clock (sine wave).

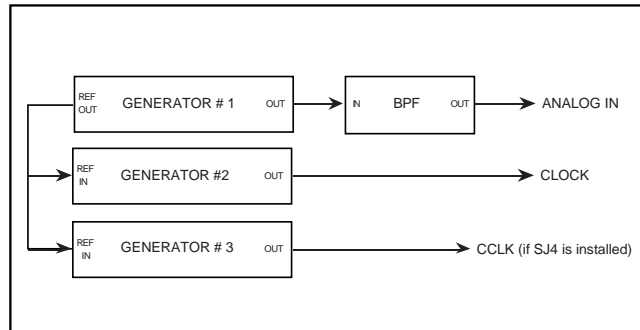


Figure 13. Synchronous Equipment Hookup

Generator 3 (needed only if solder jumper option SJ4 is used) is the capture clock (TTL). A phase-adjustment option for generator 3 is necessary to place the edge of the capture clock at the proper setup time. R11 and R12 are 51Ω and serve as termination resistors for generator 2 and generator 3, respectively (Figure 17).

Signal-Generator Selection

Two parameters are important in selecting generators 1 and 2:

- 1) The output sine wave must have at least 76dB or better of SNR. An appropriate bandpass filter (BPF) between the analog input and the generator will help improve SNR.
- 2) The sampling clock jitter or aperture jitter can originate both inside and outside the ADC. Aperture jitter or the uncertainty of clock-edge placement can significantly degrade effective bits performance.

This jitter is translated into the ADC amplitude error, and is proportional to the analog input slew rate. Consider the selection of an acceptable clock generator. For a sinusoidal input, the uncertainty of clock-edge placement from cycle to cycle due to equipment jitter affects ADC performance, especially the SNR.

$$\text{SNR (max)} = \{20\log[1 / (2\pi f_{\text{IN}} t_J)] + 3.02\}\text{dB}$$

where: f_{IN} = analog input frequency

and t_J = the aperture jitter in RMS units

Low-Frequency Performance Check

This section describes one approach to visual evaluation of DNL, nonmonotonicity, synchronous noise, and transition noise. Use DAC OUT (from the daughter-board, Figure 18) as the monitoring point to view the quality of the quantization signal. Another common approach is to use a three-bit reconstruction DAC generated from three LSBs (Figure 17). When jumpers SJ9, SJ10, and SJ11 are installed, R30–R33 form a three-bit DAC (Figure 14).

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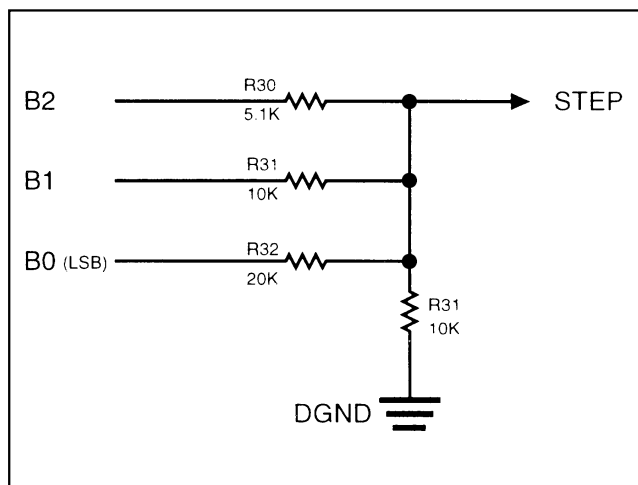


Figure 14. Three-Bit Reconstruction DAC

This three-bit reconstruction DAC's output can be viewed through the test point STEP with the oscilloscope. For this test, use a function generator for generators 1 and 2, and set up for a ramp output. Replace the BPF with an RC lowpass filter (1k and 0.01μF) to eliminate all high-frequency components. Set this ramp signal's slew rate to 1LSB per n conversions (sampling period) for a desired (1 / n) test resolution. A minimum of n = 10 is recommended for this application. The peak-to-peak voltage and the ramp-input period are then dependent on the selection of the number of steps (LSBs) within one ramp's period. Note that R10 (51Ω) may need to be removed. Set CLK and CCLK to the same relatively low frequency (approximately 1MHz or slower). Make adjustments to meet the tpwH and ts specifications. (See Figures 5 and 6; also see Table 6.)

The following formulas summarize the criteria for selecting the analog ramp-input signal:

Ramp peak-to-peak voltage: $V_{p-p} = m(FSR / 1024)$

Ramp period: $t = (m)(n) / f_s$

where: m = desired number of steps (LSBs) per ramp's period

f_s = sampling frequency

FSR = full-scale range (the MAX1160/MAX1161's FSR is typically 4V)

n = desired test resolution or the number of conversions / LSB

Figure 15 shows the relationship between the analog input ramp signal and the resulting three-bit reconstruction DAC. It shows 16 LSBs of peak-to-peak input voltage (i.e., two eight-level steps) per period. For an ideal ADC and an ideal ramp input, its digital output code changes state by 1LSB every (n)th conversion (dash line in the transfer curve). Any error in the ADC makes the corresponding output codes change state before or after the (n)th conversion. This error translates into smaller or larger respective step width. The DNL is judged visually by comparing the actual step size with respect to the ideal step with $\pm(1/n)$ LSB of accuracy. In this case, the ideal step is the average of the step size. Other errors (transition noise and nonmonotonicity) can be resolved similarly. Figure 15 also gives the identification of each error from the actual transfer curve.

Example:

- 1) The MAX1160 is operated at 500kHz (sampling frequency).
- 2) One-tenth of the test resolution is desired.
- 3) The scope is externally triggered to the ramp input. Three retraces of eight-level steps (or 24 total steps) per ramp's period are selected.

What peak-to-peak voltage (V_{p-p}) and ramp input signal period (t) are required to drive the MAX1160?

Answer:

- 1) $f_s = 500\text{kHz}$
- 2) $n = 10$
- 3) $m = 24$, then $V_{p-p} = m(FSR / 1024) = 24(4 / 1024) = 94\text{mV}$
 $t = (m)(n) / f_s = (24)(10) / 5,000,000 = 480\mu\text{s}$

Note that the above input signal covers only 24 parts in 1024 of the FSR. To identify all errors through the full-scale range, slowly sweep the ramp input from -FS to +FS and observe the output steps for transition noise, DNL, and nonmonotonicity as indicated in the transfer curve (Figure 15). Most generators do not have DC offset covering the +2.5V to -2.5V range. You may need to construct an additional circuit using a summing amplifier to DC-offset the above ramp-input signal.

Synchronous noise is the distortion of the device's performance when the sampling frequency varies. (Normally, the DNL can be clearly observed.) This is usually caused by the digital signals being coupled back internally into the analog input signal. This problem is common for

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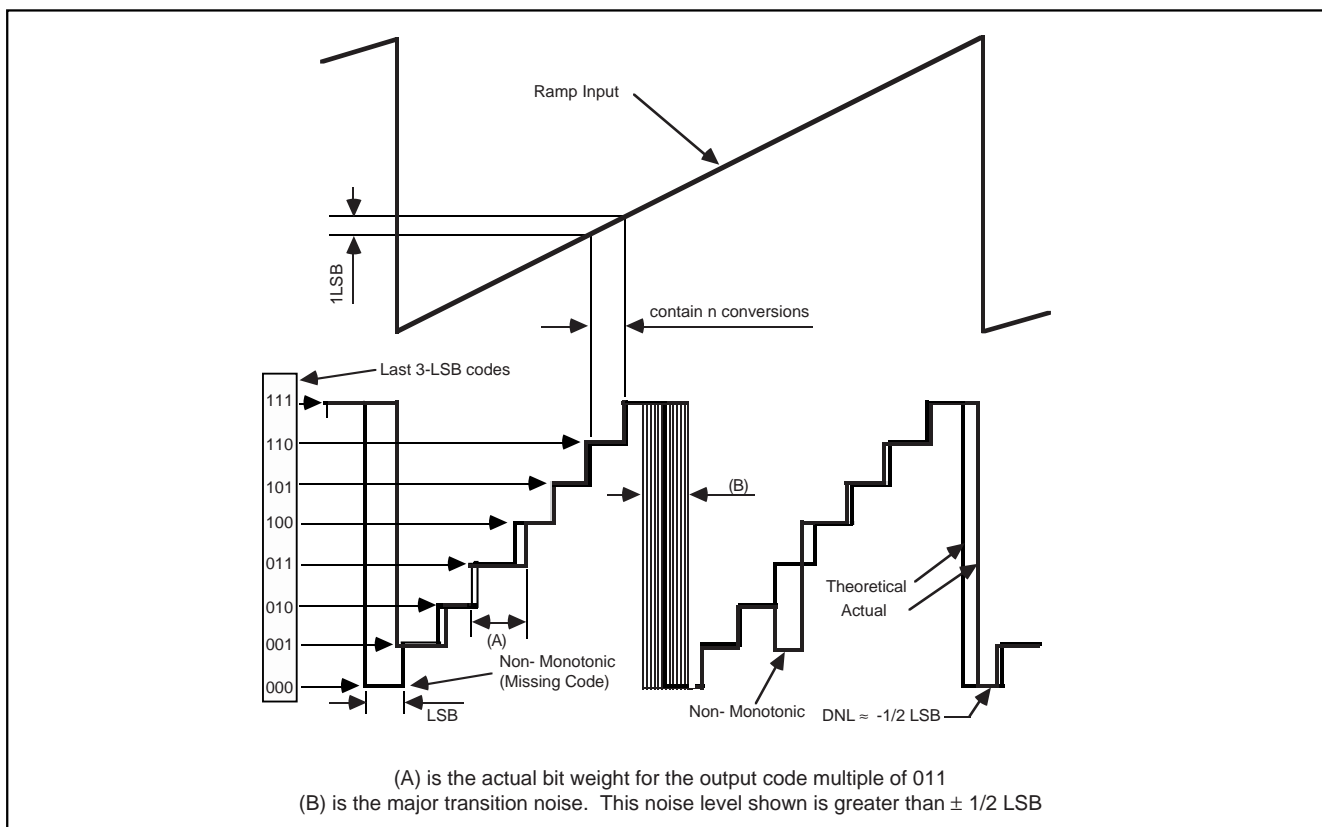


Figure 15. Three-Bit Reconstruction DAC Waveform Using Analog Input Ramp

ADCs that use the successive-approximation register (SAR) architecture. An ADC with this type of symptom presents some weak performances at a specific sampling frequency (within the specified sampling rate), but shows better results when the sampling frequency is varied up or down from that weak spot. To verify synchronous noise using this setup, slowly change the sampling frequency and observe the transfer curve, especially the changes in DNL.

Advantages:

- 1) Many tests (as stated above) can be extracted from this simple test setup.
- 2) The missing code and the transition noise can be more accurately identified than with any other standard test method.
- 3) Setup is quick and relatively accurate.

Disadvantages:

- 1) Accuracy depends on individual judgement and is limited to interpretation of the oscilloscope display.
- 2) The transfer curve does not show the exact code, but rather a multiple of the last three bits. To overcome this problem, probe every bit using an oscilloscope, or install LEDs at each output (P3 connector) to signal each output bit's state.

Dynamic Testing

Figure 16 is the recommended functional diagram for dynamic testing the MAX1160/MAX1161 using the MAX1160 EV kit. A common practice is to use the DAC OUT signal to analyze the ADC's dynamic performances (SNR and THD) through a spectrum analyzer. This method of testing presents some uncertainties. The DAC must be glitch free, and its dynamic accuracy (DNL and INL) must be far better than the ADC under test. Any errors in the DAC are added to the total SNR and/or THD.

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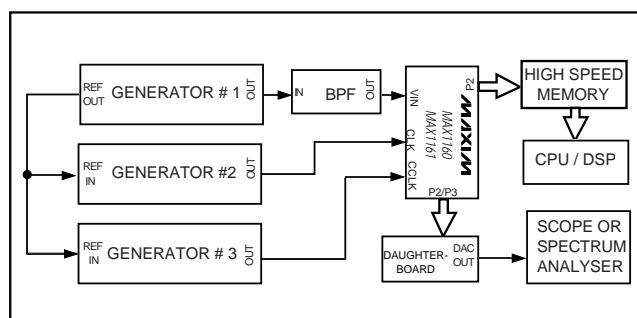


Figure 16. Dynamic Testing Test Setup

It is preferable to perform these tests using digital-signal processing (DSP). Numerous standard software packages are available to service this application. The MAX1160 EV kit provides the data outputs through P2 (Table 6). The reconstruction DAC output can be obtained from the daughterboard.

In many cases, the capture memory is much slower than the available valid data of the ADC under test. It is then necessary to decimate the capture clock at a rate of $f_s / 2^n$. The beat frequency can be achieved by changing the analog input frequency slightly by Δf_{IN} . For a 4096-point FFT, the beat frequency of $\Delta f_{IN} = f_c / 4096$ is added to (or subtracted from) the analog input frequency. 4096 data points are filled in one test period where the input is at $f_{IN} \pm (f_c / 4096)$ and the output is updated at $1/f_c$ interval. Select f_{IN} as the multiple (integer) of f_c to achieve complete system synchronization. Both capture memory and the DAC run at a relatively low update rate ($f_s / 2^n$). The daughterboard can update to 80MSPs.

Calibration

For every new MAX1160/MAX1161 installed, VST and VSB voltages must be recalibrated.

Check for installation of jumpers SJ2B, SJ2C, and SJ3.

I) Equipment Needed

- 1) Four DC power supplies: +A5V, -A5.2V, +D5V, and -D5.2V
- 2) Function generator
- 3) DVM with 5.5-digit precision
- 4) Oscilloscope

II) Equipment Setup/Hookup

- 1) Ensure that the U1 socket does not contain the ADC at this point.
- 2) Connect all four power supplies as shown in Table 1 and Figures 2 and 3.
- 3) Connect the function generator to CLK BNC.
- 4) Set the CLK to 3MHz, sinewave, $\pm 2V$.
- 5) Connect VIN to AGND.

III) References Calibration

- 1) Monitor TP1 with respect to AGND test point with DVM.
- 2) Adjust R1 for +2.500V at TP1.
- 3) Monitor TP2 with respect to AGND test point with DVM.
- 4) Adjust R2 for -2.500V at TP2.
- 5) Turn all power off.
- 6) Install the ADC into the U1 socket (repeat this procedure for all new devices).
- 7) Turn all power back on.
- 8) Monitor U1, pin 22 (VST) with respect to AGND test point with DVM.
- 9) Adjust R1 for +2.000V at VST.
- 10) Monitor U1, pin 27 (VSB) with respect to AGND test point with DVM.
- 11) Adjust R2 for -2.000V at VSB.
- 12) Repeat the procedure from number 8 until VST and VSB reach the desired voltages ($\pm 2.000V$ respectively).

IV) Clock-Circuit Calibration

- 1) Monitor PJ1 with the oscilloscope on channel 1 (externally sync to the generator).
- 2) Observe the TTL clock and adjust R3 for approximately 50% of duty cycle.

V) Latches (U7 and U8) Test

- 1) Remove R10.
- 2) Connect VIN to TP1.
- 3) Monitor P2, odd-numbered pins (7–25) with the oscilloscope, and observe TTL logic high on all pins.
- 4) Connect VIN to TP2.
- 5) Monitor P2, odd-numbered pins (7–25) with the oscilloscope, and observe TTL logic low on all pins.

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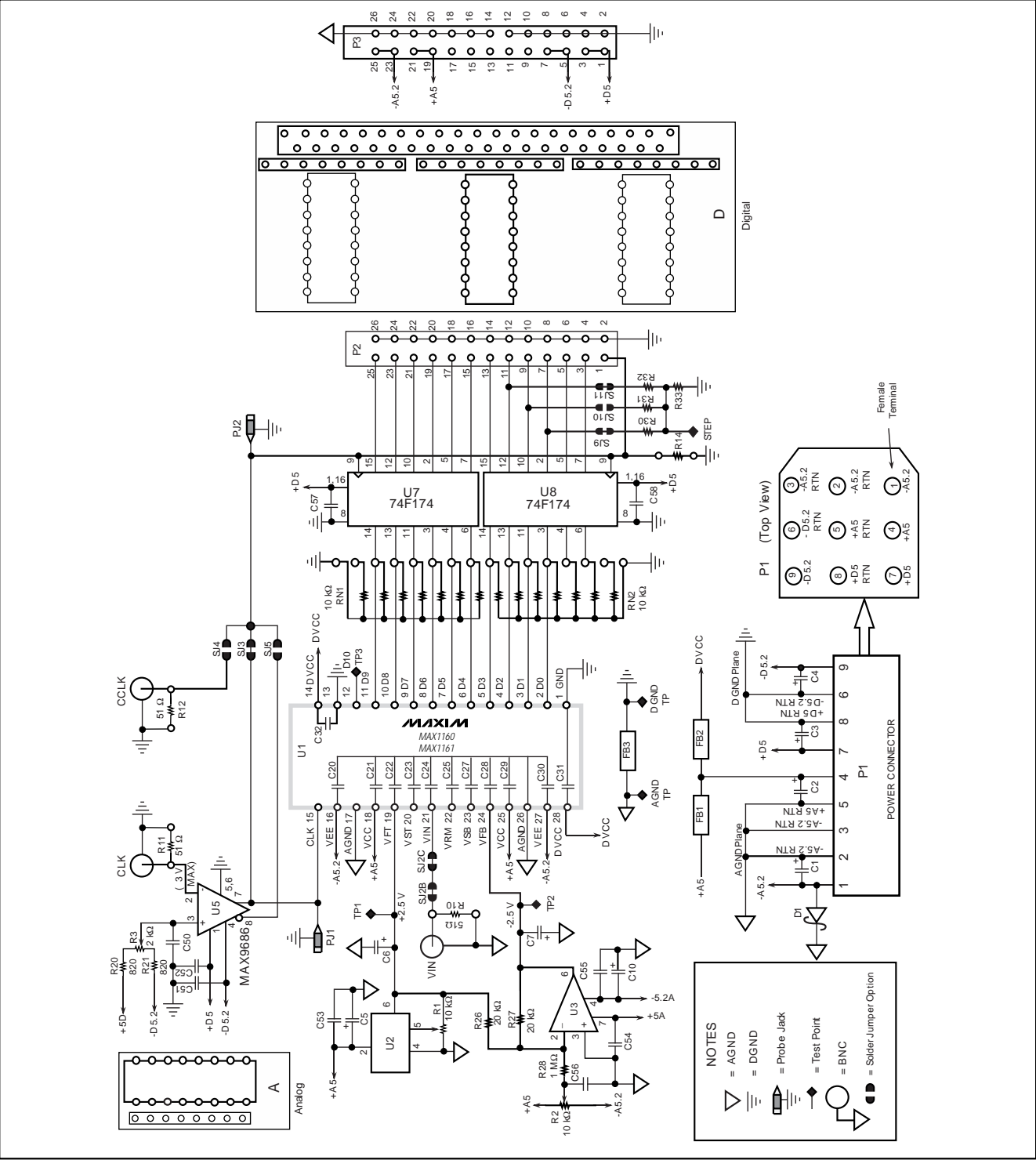


Figure 17. MAX1160 EV Kit Detailed Schematic

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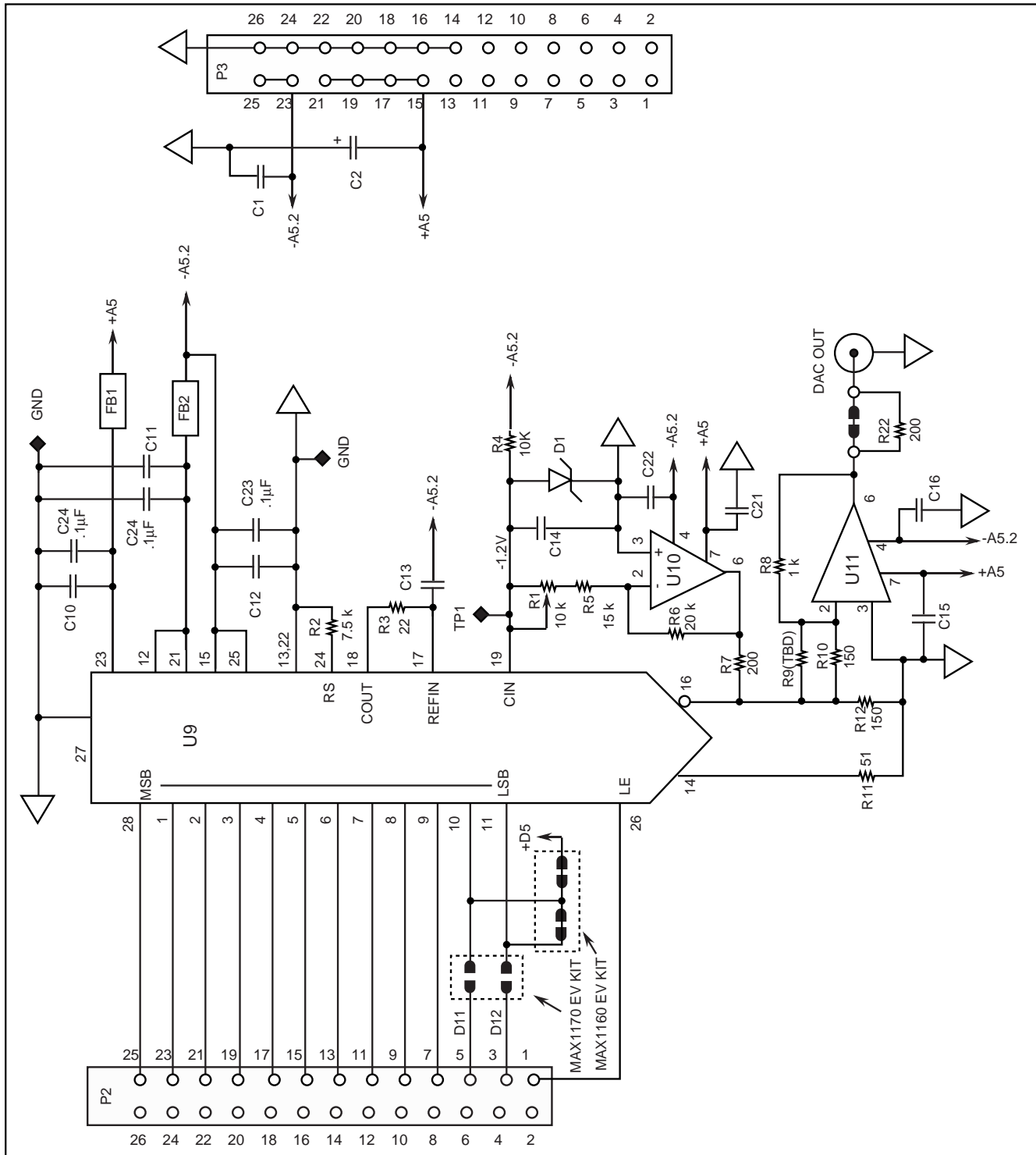


Figure 18. Daughterboard EV Kit Detailed Schematic

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NOTES

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