19-1191; Rev 0; 6/97

MAX1170 Evaluation Kit

Evaluates: MAX1170/MAX1171/MAX1172

General Description

The MAX1170 evaluation kit (EV kit) evaluates the performance of the MAX1170/MAX1171/MAX1172 monolithic, 12-bit high-speed analog-to-digital converters (ADCs). The ADCs must be ordered separately.

The MAX1170/MAX1171/MAX1172 have ±2V analog input ranges. They can digitize an analog input signal into 12-bit words at minimum update rates of 10Msps, 20Msps, and 30Msps, respectively.

Features

- **Up to 30Msps Conversion Rate**
- **On-Board Clock Drivers**
- **Data Output and Strobe Signal**
- **User-Selectable Capture Clock**
- **On-Board Reference Drivers**

EV Kit Applications

Evaluation of MAX1170/MAX1171/MAX1172

Engineering System Prototype Aid

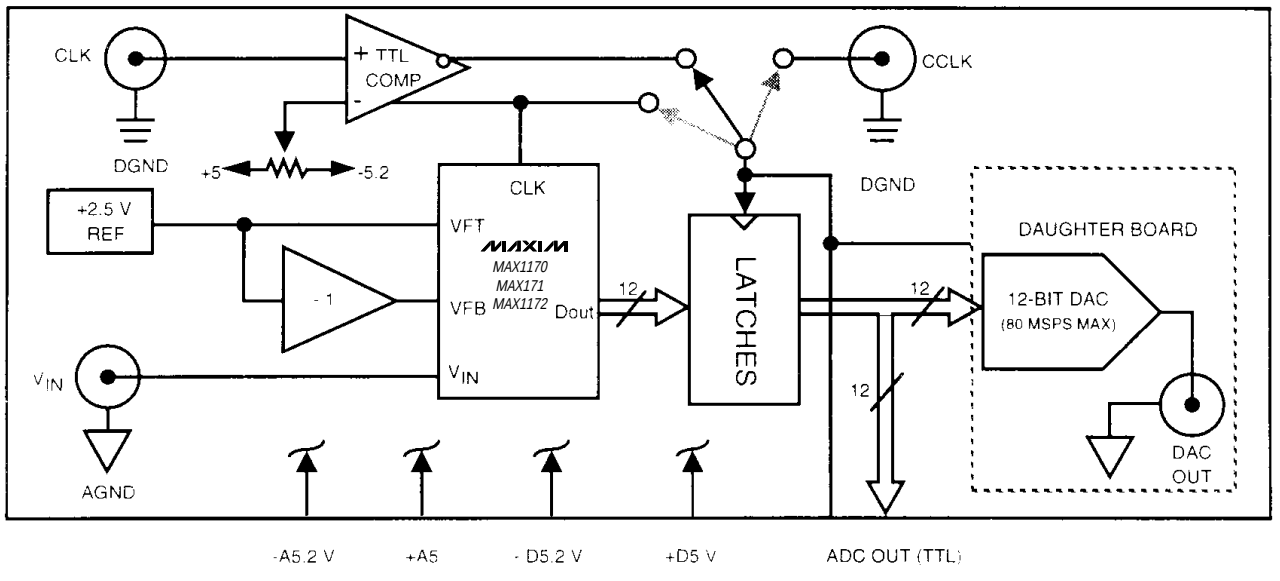
Incoming Inspection Tool

Guide for System Layout

Ordering Information

PART	TEMP. RANGE
MAX1170EVKIT*	0°C to +70°C

**Evaluates either MAX1170CDJ, MAX1171CDJ, or MAX1172CDJ, which must be ordered separately.*



THE MAX1170 EV KIT CONSISTS OF FIVE SEPARATE SECTIONS:

1) REFERENCE CIRCUITS
2) CLOCK CIRCUITS
3) MAX1170, MAX1171, OR MAX1172 12-BIT ADC (NOT INCLUDED WITH THE BOARD)
4) OUTPUT LATCHES AVAILABLE THROUGH A 26-PIN FEMALE RIBBON CONNECTOR
5) THE DAC RECONSTRUCTION BOARD IS A SEPARATE DAUGHTERBOARD (2.5" x 3.0") THAT INTERFACES DIRECTLY WITH THE MAX1170 EV KIT MAIN BOARD (4" x 7.5")

Figure 1. Functional Diagram

MAX1170 EV Kit Component List

DESIGNATION	QTY	DESCRIPTION
C1–C7, C10	8	10µF, 25V, 0.10" tantalum capacitors
C20, C30	2	0.1µF chip capacitors
C21–C29, C31, C32	11	0.01µF chip capacitors
C50–C58	9	0.01µF, 10% ceramic capacitors
D1	1	Lead-mounted hot-carrier diode
FB1, FB2, FB3	3	Lead-mounted ferrite beads
None	1	Printed circuit board
P1	1	9-pin power connector
P1/Receptacle	1	9-pin power-connector, receptacle
P2, P3	2	Ribbon-plug connectors
PJ1, PJ2	2	Probe connectors
R1, R2	2	10kΩ, 12-turns potentiometers
R3	1	2kΩ, 12-turns potentiometer
R10, R11, R12	3	51Ω, 5%, 1/8W resistors
R20, R21	2	820Ω, 5%, 1/8W resistors
R26, R27, R30	3	20kΩ, 5%, 1/8W resistors
R28	1	1MΩ, 5%, 1/8W resistor

DESIGNATION	QTY	DESCRIPTION
R32	1	5.1kΩ, 5%, 1/8W resistor
R33	1	10kΩ, 5%, 1/8W resistor
RN1, RN2	2	10kΩ, 708A-type, 8-pin SIP resistors
TP1, TP2, TP3, AG, DG, STEP	6	76-mil-diameter hole test-point terminals
U1	1	Device under test: 12-bit ADC
U2	1	+2.5V precision voltage reference
U3	1	Low-noise op amp
U5	1	Single, fast-TTL comparator (8 DIP)
U7, U8	2	Fast TTL, hex D flip-flops
None	3	BNC connector, receptacles
None	1	0.600" socket (32 DIP)
None	1	Break-away socket strips (20 SIP)
None	4	1" round nylon standoffs
None	4	3/16", 4-40, round-head nylon screws
None	1	Crimp male terminal for P3
None	8	Crimp female terminals for P3

Daughterboard Component List

DESIGNATION	QTY	DESCRIPTION
C1, C2	2	10µF, 25V, 0.10" tantalum capacitors
C10–C16	7	0.1µF chip capacitors
C21–C25	5	0.1µF, 10% ceramic capacitors
D1	1	1.2V reference, 2-terminal IC
DB792 PCB	1	Printed circuit board
FB1, FB2	2	Lead-mounted ferrite beads
P2, P3	2	26-pin, dual-row, vertical PCB-mount connectors
R1	1	10kΩ, 12-turns potentiometer
R2	1	7.5kΩ, 5%, 1/8W resistor
R3	1	22Ω, 5%, 1/8W resistor
R4	1	10kΩ, 5%, 1/8W resistor
R5	1	15kΩ, 5%, 1/8W resistor

DESIGNATION	QTY	DESCRIPTION
R6	1	20kΩ, 5%, 1/8W resistor
R7	1	1kΩ, 5%, 1/8W resistor
R8	1	1kΩ, 5%, 1/8W resistor
R11, R12	2	150Ω, 5%, 1/8W resistors
R20, R21	2	820Ω, 5%, 1/8W resistors
R22	1	200Ω, 5%, 1/8W resistor
TP1, AG, DG	3	76-mil-diameter hole, test-point terminals
U9	1	100MHz, 12-bit TTL DAC
U10	1	Low-noise op amp
U11	1	Low-distortion op amp
—	1	BNC connector
—	1	Crimp male terminal for P3

Detailed Description

Power Supplies

The MAX1170/MAX1171/MAX1172 require four power-supply sources: analog -5.2V (-A5.2V), analog +5V (+A5V), digital -5.2V (-D5.2V), and digital +5V (+D5V). P1 is the power connector (Figure 2). Table 1 shows the recommended operating voltage range.

Power Supplies and Grounding

The MAX1170/MAX1171/MAX1172 require two analog supply voltages: -A5.2V and +A5V. The +A5V supply is common to analog VCC (pins 20 and 29) and digital DVCC (pins 16 and 32). A ferrite bead in series with each supply (RF1 and RF2) reduces the transient noise injected into VCC. The bead to MAX1170/MAX1171/MAX1172 connections should not be shared with any other device. Bypass each power-supply pin as closely as possible to the device (0.1µF to AGND for each VEE and VCC pin, and 0.01µF to DGND for DVCC).

Total power dissipation for the MAX1170 EV kit is typically 1.9W.

Table 1. Recommended Power-Supply Operating Range

POWER SUPPLY (V)	MIN (V)	TYP (V)	MAX (V)	TYPICAL CURRENT (mA)
-A5.2	-4.95	-5.20	-5.45	60
+A5	+4.75	+5.00	+5.25	240
-D5.2	-4.95	-5.20	-5.45	15
+D5	+4.75	+5.00	+5.25	60

Table 2. Pin Assignments

PIN	DESCRIPTION
1	Analog -5.2V
2	Analog -5.2V Return #1 (AGND)
3	Analog -5.2V Return #2 (AGND)
4	Analog +5V
5	Analog +5V Return (AGND)
6	Digital -5.2V Return (DGND)
7	Digital +5V
8	Digital +5V Return (DGND)
9	Digital -5.2V

AGND and DGND are isolated on the MAX1170/MAX1171/MAX1172. Both -A5.2V and +A5V are the analog supply sources. As with all very-high-speed ADCs, grounding is critical. Therefore, the ground-plane technique is best. To use this method, split and tie the AGND and DGND ground planes together at the device through an RF bead.

The MAX1170 EV kit is a four-layer printed circuit board: top signal, ground (AGND and DGND) plane, power plane, and bottom signal. The two ground planes are connected at the device through a ferrite bead (RF3). All three ferrite beads (RF1, RF2, and RF3) are located close to the ADC.

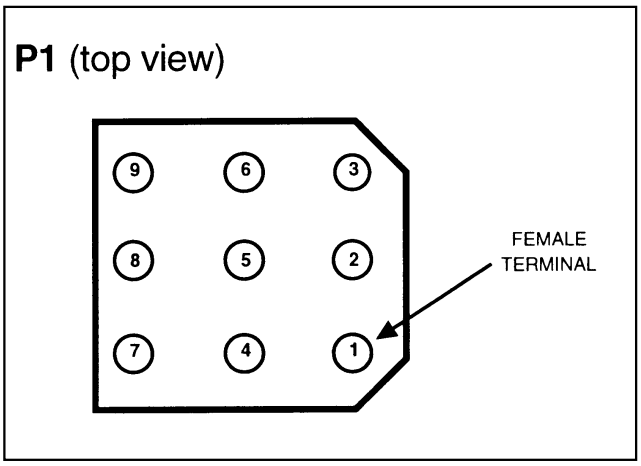


Figure 2. P1 Power-Supply Connector's Pin Assignment

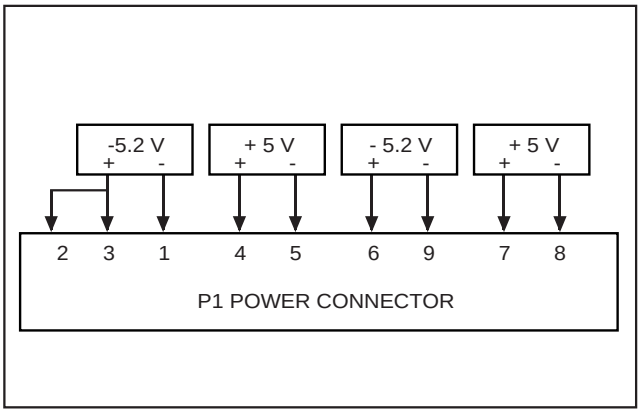


Figure 3. P1 Connector/Hookup

Reference Circuit

The MAX1170/MAX1171/MAX1172 require the use of two voltage references: VFT and VFB. VFT (+2.5V typ) is the force for the top of the voltage-reference ladder, and VFB (-2.5V typ) is the force for the bottom of the voltage-reference ladder. Both voltages are applied across an internal 900Ω reference-ladder resistance. In addition, there are five reference-ladder taps: VST, VRT3, VRT2, VRT1, and VSB. VST (+2V) is the top of the reference-ladder tap; (+2V), VRT3 (+1.0V typ) is the top half of the ladder; VRT2 (0V typ) is the middle point; VRT1 (-1.0V) is the bottom half; and VSB (-2V) is the bottom of the reference-ladder tap. The voltages at VST and VSB are the full-scale input voltages expected of the device when VFT and VFB are driven to the recommended voltages (typically +2.5V and -2.5V, respectively). Use VST and VSB (±2V) to monitor the actual full-scale input voltages by adjusting VFT and VFB (Table 3). These adjustments interact with one another; repeat them several times as needed until VST and VSB settle at the desired voltages. Do not drive the three taps (VRT1, VRT2, and VRT3), as is commonly done with a standard flash ADC converter. When not being used, decouple with a 0.01µF, surface-mount chip capacitor from each tap to AGND, to minimize high-frequency noise injection.

Table 3. Reference Adjustment

	VST	VSB
Test Point	U1, pin 21	U1, pin 27
Min	+1.950V	-2.050V
Typ	+2.000V	-2.000V
Max	+2.050V	-1.950V
Adjust	R1	R2

NOTE: The MAX1170/MAX1171/MAX1172 (especially all reference taps) are sensitive to electrostatic discharge (ESD).

Table 4. Output Coding

ANALOG INPUT	D12 (OVERRANGE BIT)	DATA OUTPUT CODE
<-2.0V	0	0000 0000 0000
-2.0V + 1LSB	0	0000 0000 000Ø
0V	0	ØØØØ ØØØØ ØØØØ
+2.0V - 1LSB	0	1111 1111 111Ø
>+2.0V + 1/2LSB	1	1111 1111 1111

NOTE: Ø indicates the flickering bit between logic 0 and 1.

As shown in Figure 17, U2 is the +2.5V reference with ±0.6% of adjustable range (R1 potentiometer). U3 is set up as an inverting amplifier. Its tolerance is 5% with ±300mV of adjustable range (R2 potentiometer). Maxim recommends that you operate VFT and VFB to within ±2% (or ±2.5V ±50mV) to maintain accuracy within the specified limit. Before each MAX1170 EV kit board is shipped, the references are adjusted to ±2.5V ±5mV. For each new MAX1170/MAX1171/MAX1172, readjust VST and VSB. All measurements must be referenced to the AGND test point provided.

Figure 17 shows one type of reference driver. Figure 4 shows another way to drive the reference circuits using force and sense. This circuit provides better control on the plus full-scale (+FS) and minus full-scale (-FS) errors by sensing VST and VSB to ±2.0V, respectively. However, VST and VSB are not low-impedance nodes; thus, they require additional precaution when routing (PCB layout).

ADCs

The MAX1170 is a 12-bit ADC capable of digitizing an input signal with a 10Msps update rate. The MAX1171/MAX1172 ADCs are pin compatible with the MAX1170, but digitize two and three times faster, respectively. On all devices, the expected full-scale analog input range is from VST to VSB. The analog input is latched at CLK's leading edge. There are 13 digital TTL outputs. D0–D11 are the parallel TTL output bits, with D0 the least significant bit (LSB), D11 the most significant bit (MSB), and D12 the overrange bit. The data outputs are latched at CLK's rising edge, with a 14ns typical propagation delay. There is one clock latency between CLK and valid output data (Figure 5). The output code is straight binary.

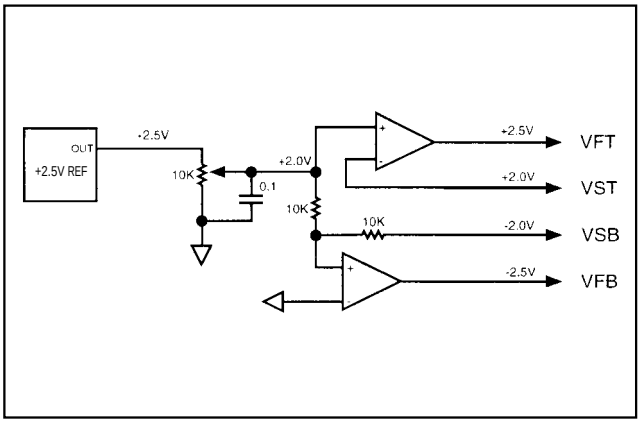


Figure 4. Alternative Reference Driver

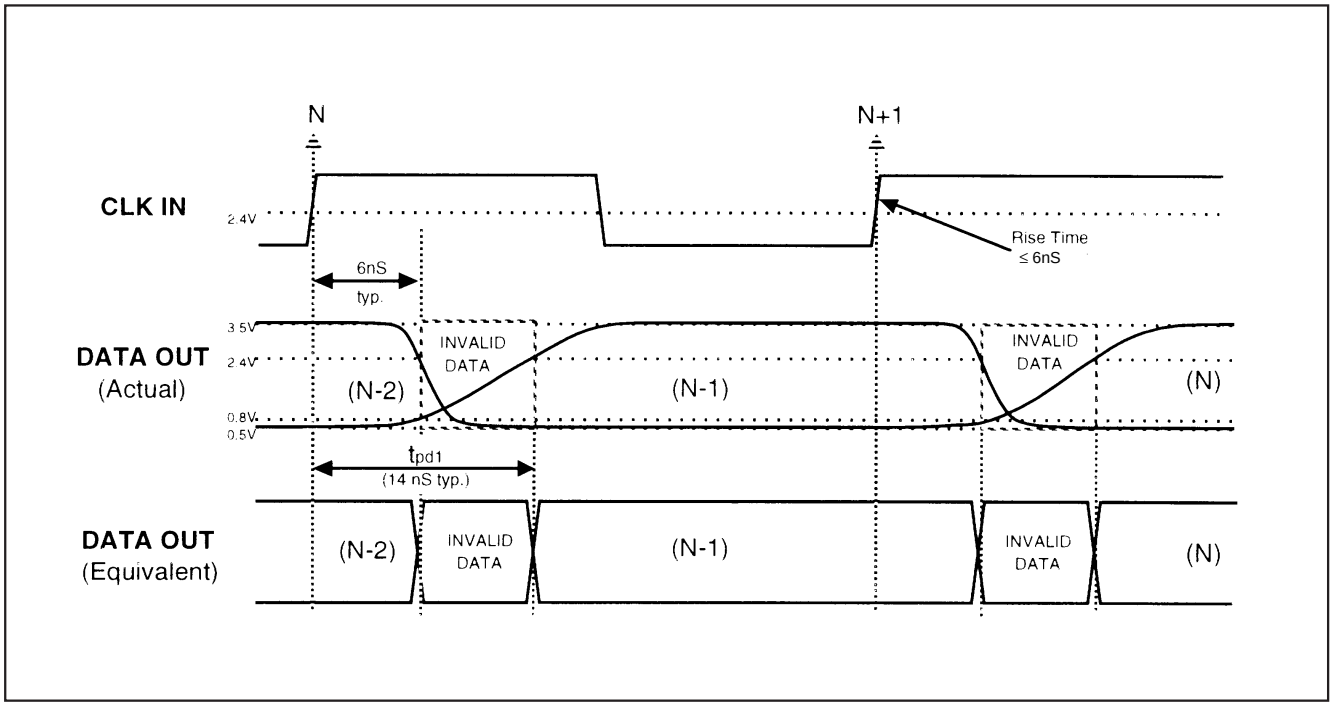


Figure 5. Digital Output Characteristic of the MAX1170/MAX1171/MAX1172

Pin 24 is the analog input pin. Selecting the analog input driver is simpler than with most flash ADCs because the input impedance and input capacitance are typically 300kΩ and 5pF, respectively. For example, at 5MHz and 4Vp-p sine-wave input, the input driver source requires only 0.324mA of peak output current (4πFC).

The analog input is fed directly from a BNC (VIN). R10 (51Ω) is the analog input source termination mounted on a socket as a user-selectable termination. The analog input pin has no circuit protection. Its maximum rating is from VFT to VFB (±2.5V). Use a voltage limiter to protect the input pin from permanent damage in applications with an analog input range greater than ±2.5V (see the *Input and Latchup Protection* section).

Input Clock Driver

CLK is the single-ended input clock to the MAX1170 EV kit; CLK IN is the input clock to the ADC; and CCLK is the capture clock used for the output latches (U7 and U8).

The MAX1170/MAX1171/MAX1172's clock input requires TTL-logic level with a 6ns or faster rise time to reduce noise. Fast TTL-family components (74FXX) fit well in this application. Finding a square-wave generator (TTL logic up to 30MHz, fast slew rate, and low jitter) is more difficult than finding a sine-wave, low-jitter generator. U5 (MAX9686, TTL voltage comparator) provides most of the above requirements for driving the ADC (except the low-jitter generator). The CLK signal should be a sine-wave signal with an amplitude not to exceed ±3V (input common-mode limitation of U5). R11 (51Ω) is the CLK source termination. Use R3 to adjust the CLK IN duty cycle. CLK IN is in phase with CLK and with a 6ns typical propagation delay. Due to the internal track/hold amplifier (THA), keep the positive clock (CLK IN) pulse width from 15ns to 300ns for the MAX1172, 20ns to 300ns for the MAX1171, and 30ns to 300ns for the MAX1170. When operating the ADC faster than 3Msps, keep the clock duty cycle at approximately 50% ±10%. Probe jack PJ1 is the monitoring test point for CLK IN. Use this test point when adjusting the clock duty cycle.

A falling edge at CLK IN (pin 17) causes the internal THA to go into track mode. Keep the MAX1170/MAX1171/MAX1172 in track mode at startup time or when the device is idle for an extended period of time. This setup prevents the internal THA from going into saturation due to droop. The EV board provides a logic low to the ADC clock when the pulse generator (CLK) is removed from the evaluation board.

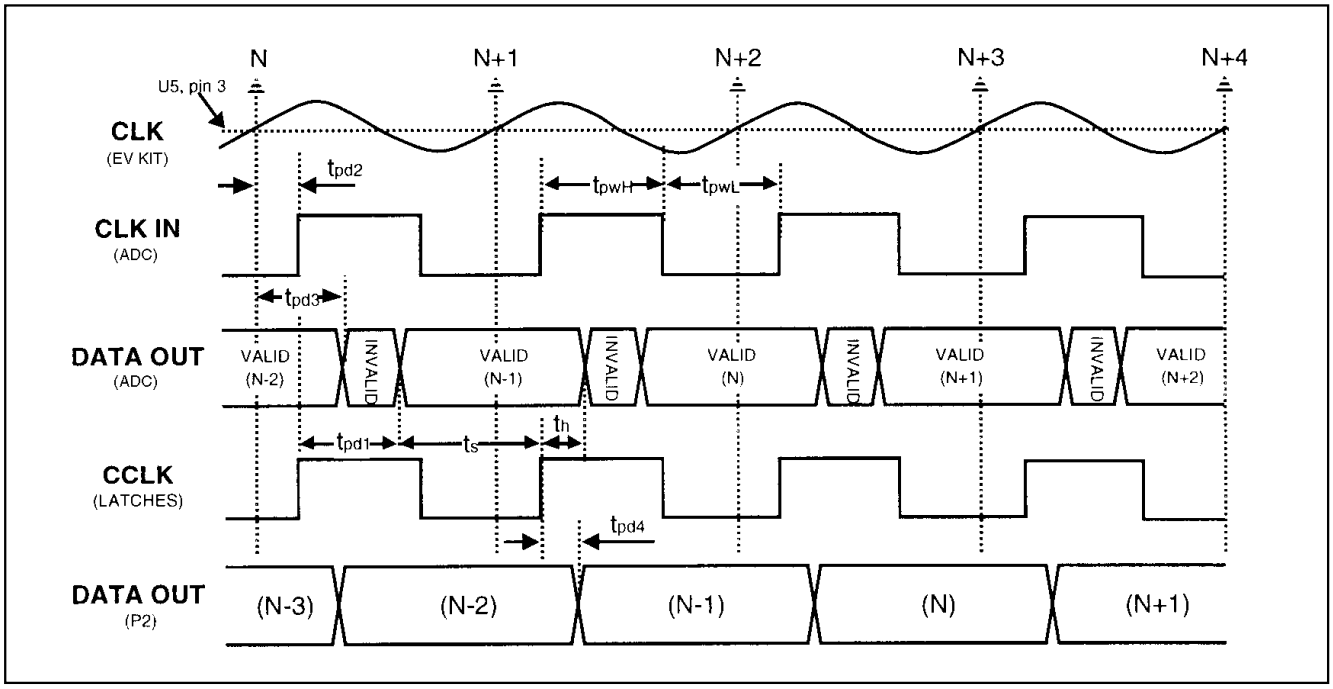


Figure 6. MAX1170 EV Kit Timing Diagram, CCLK = CLK IN

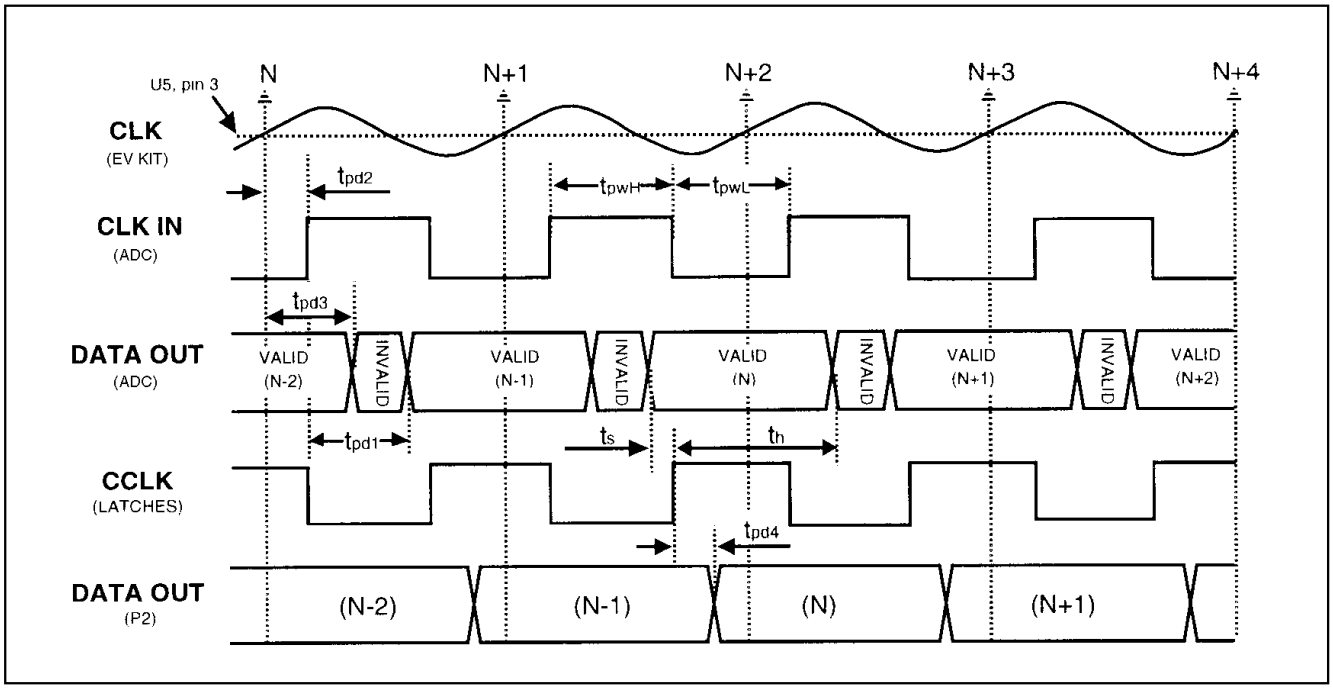


Figure 7. MAX1170 EV Kit Timing Diagram, CCLK is 180° Out-of-Phase from CLK IN

TTL Output Data Latches

The ADC's rise time (t_{RISE}) and fall time (t_{FALL}) are not symmetrical. The propagation delay, with respect to t_{RISE} at the 2.4V crossing, is typically 14ns; with respect to t_{FALL} at the 2.4V crossing, it is typically 6ns. Figure 5 illustrates the output characteristic of the MAX1170/MAX1171/MAX1172. The nonsymmetrical nature of the outputs creates approximately 8ns of invalid data.

In applications using a reconstruction DAC, the invalid data zone causes an unwanted glitch in the reconstruction signal if the DAC is directly interfaced with the MAX1170/MAX1171/MAX1172. To avoid this, buffer the ADC with edge-triggered latches, such as 74F174.

The BNC connector (CCLK) is the 50Ω input capture clock. The data latches' outputs (D0–D11) are routed through the standard 26-pin female ribbon connector (P2). SJ3, SJ4, and SJ5 are the solder-jumper options for the capture clock. Only one of these jumpers must be connected:

- When SJ3 is factory installed, the ADC and the latches (U7 and U8) are clocked at the same time. With this configuration, the data at connector P2 contains another clock cycle of latency (a total of two cycles of latency, as shown in Figure 6).
- When SJ4 is installed, the capture clock must be supplied externally through CCLK. The setup time (t_S) and hold time (t_H) shown in Table 6 must be met when selecting this option.
- When SJ5 is installed, the buffers are latched at the falling edge of the CLK IN (MAX1170/MAX1172). With this option, the t_S and t_H requirements for the 74F174 latches must be met (Table 6). The placement of this capture clock edge is dependent on the clock pulse width and the sampling frequency. This option is not recommended above 25Msps.

The latched digital outputs are routed through P2 (a 26-pin ribbon connector) (Table 5). The overrange bit (D12) can be viewed through test point TP3. D12 is not brought out through P2.

Table 5. P2, Latched Output Data, 26-Pin Female Ribbon Connector

P2	FUNCTION	LOGIC
1	CCLK	TTL
2	DGND	DGND
3	D0 (LSB)	TTL
4	DGND	DGND
5	D1	TTL
6	DGND	DGND
7	D2	TTL
8	DGND	DGND
9	D3	TTL
10	DGND	DGND
11	D4	TTL
12	DGND	DGND
13	D5	TTL
14	DGND	DGND
15	D6	TTL
16	DGND	DGND
17	D7	TTL
18	DGND	DGND
19	D8	TTL
20	DGND	DGND
21	D9	TTL
22	DGND	DGND
23	D10	TTL
24	DGND	DGND
25	D11 (MSB)	TTL
26	DGND	DGND

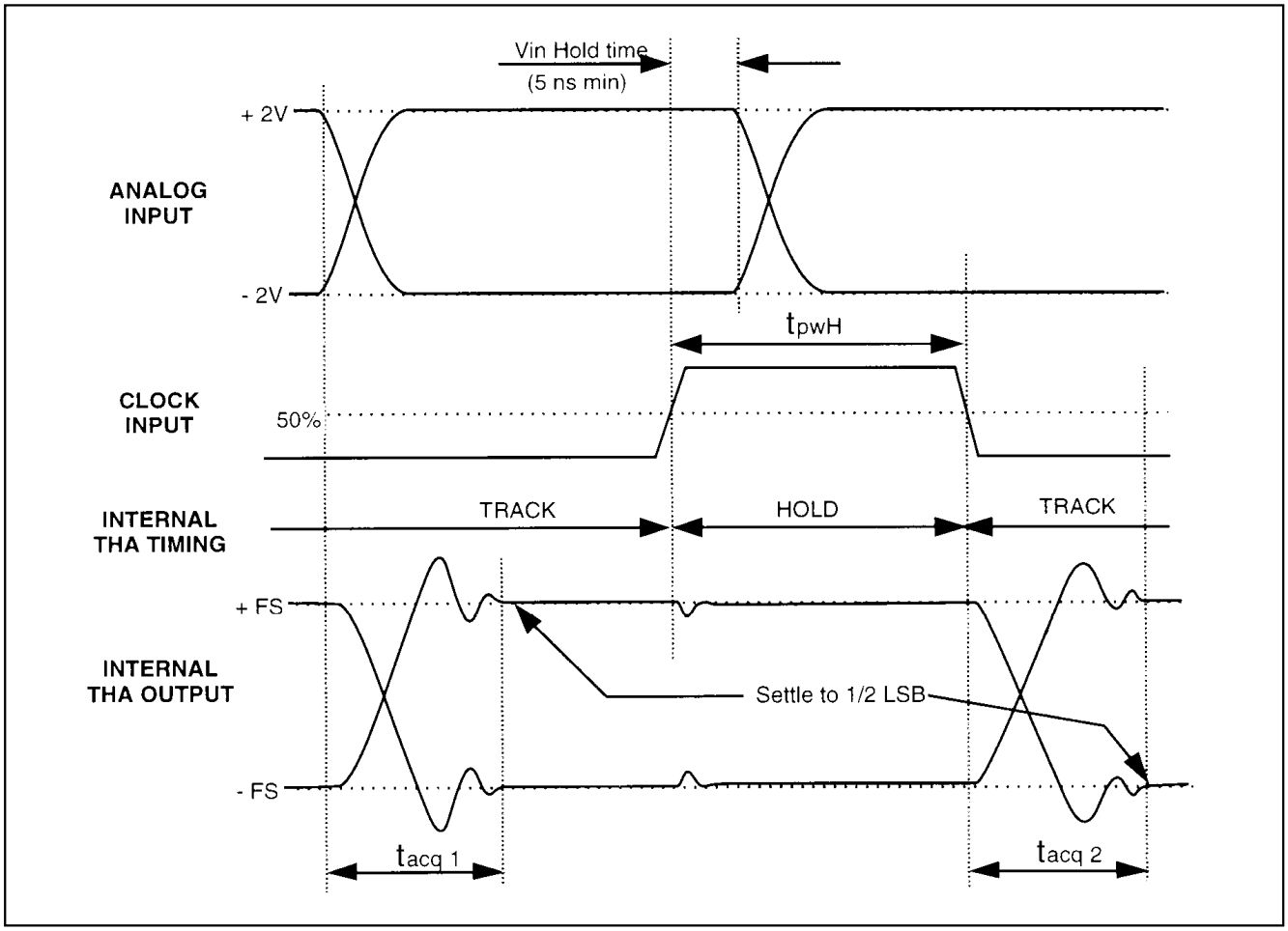


Figure 8. Acquisition Time

Acquisition Time Specification

The acquisition time (t_{ACQ}) is defined as the hold-to-track, full-scale settling time for the internal THA. The clock input's logic low corresponds to track mode, and logic high is the hold mode for the internal THA. Figure 8 shows two types of acquisition time:

- t_{ACQ1} is the THA's settling time when it is in track mode and it is driven by the analog input switching.
- t_{ACQ2} is the amount of time it takes for the ADC's internal THA to reacquire the analog input when switching from hold to track (CLK IN from high to low), to within 1/2LSB.

Both t_{ACQ1} and t_{ACQ2} need the same amount of time (see the acquisition-time specification in the corresponding data sheet).

Place the low-to-high clock transition after both the analog input and the internal THA are settled. The analog input must remain for at least 5ns (VIN hold time) after the low-to-high clock transition. Keep the clock positive pulse width (t_{PWH}) to within the recommended limit (refer to the specification in the corresponding data sheet).

Timing Considerations When Using an External Track/Hold

The signal-to-noise ratio (SNR) and the total harmonic distortion (THD) degrade as the analog input frequency increases. These parameters imply that the differential nonlinearity (DNL) and the integral nonlinearity (INL) degrade as well at high frequency. However, these degradations are mainly due to aperture jitter, analog input bandwidth limitation, and/or the ADC's slew-rate

Table 6. Timing Specification

FUNCTION	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{PD1}	MAX1170/MAX1171/MAX1172, CLK to Data Valid Propagation Delay	—	14	18	ns
t_{PD2}	MAX9686 Propagation Delay	—	6	9	ns
t_{PD3}	MAX1170/MAX1171/MAX1172, t_{FALL} Propagation Delay	4.5	7	10	ns
t_{PD4}	74F174 Propagation Delay	4.5	7	10	ns
t_S	74F174 Setup Time	4.0	—	—	ns
t_H	74F174 Hold Time	4.0	—	—	ns
t_{PWH}	CLK Positive Pulse Width (MAX1170)	30	—	300	ns
t_{PWL}	CLK Negative Pulse Width (MAX1170)	30	—	—	ns
t_{PWH}	CLK Positive Pulse Width (MAX1171)	20	—	300	ns
t_{PWL}	CLK Negative Pulse Width (MAX1171)	20	—	—	ns
t_{PWH}	CLK Positive Pulse Width (MAX1172)	15	—	300	ns
t_{PWL}	CLK Negative Pulse Width (MAX1172)	15	—	—	ns

Table 7. Critical Timing Specifications

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{HTS}	THA, hold-to-track settling time	*	*	*	ns
t_{THS}	THA, track-to-hold settling time	*	*	*	
t_{ACQ}	ADC, acquisition time, 4V step		20		ns
t_{ACQ}	ADC, acquisition time		12		ns
t_{H1}	Hold time after the ADC rising clock	5			ns

**This limit depends on the external THA chosen.*

limitation. Below 1MHz, the MAX1170/MAX1171/MAX1172's SNR and THD are generally constant. To bring these accuracies up at high frequency, you might need to buffer the analog input using a THA.

The timing diagram shown in Figure 9, and the timing specifications listed in Table 7, address the critical timing necessary when driving the ADC from an external THA.

The settling time to 1/2LSB (488µV) is one of the principal requirements in a 12-bit THA. This includes both track-to-hold (t_{THS}) and hold-to-track (t_{HTS}) settling times. t_{HTS} varies with the step size (voltage) that the THA needs to swing. Place the ADC clock's rising edge after t_{THS} has settled. The MAX1170/MAX1171/MAX1172 require that the analog input be held for an additional 5ns minimum (t_{H1}) after the clock's rising edge. Figure 9 shows the ADC running at Nyquist; the sampling frequency is nearly twice the input frequency. In this example, the ADC could have as much as a 4V step (±FS) from one conversion to the next.

t_{ACQ} is the time necessary to allow the internal THA to track (CLK = low) and settle to 1/2LSB while the input changes to its new continuous level. The minimum acquisition time is 20ns for a 4V step and 12ns for a 0.5V or less step.

Being driven from an external THA, the ADC's maximum sampling rate can be determined from the combination of t_{THS}, t_{HTS}, and t_{ACQ}.

The pedestal and the droop of the THA shown in Figure 9 are not critical to the dynamic performance as long as they are constant with respect to the analog input range. They are seen as offset errors.

Low-Level Analog Input Signal

The MAX1170/MAX1171/MAX1172 require that the analog input (VIN) range be operated within ±2V ±2%. Amplification and level shifting are necessary for a lower-voltage-level VIN.

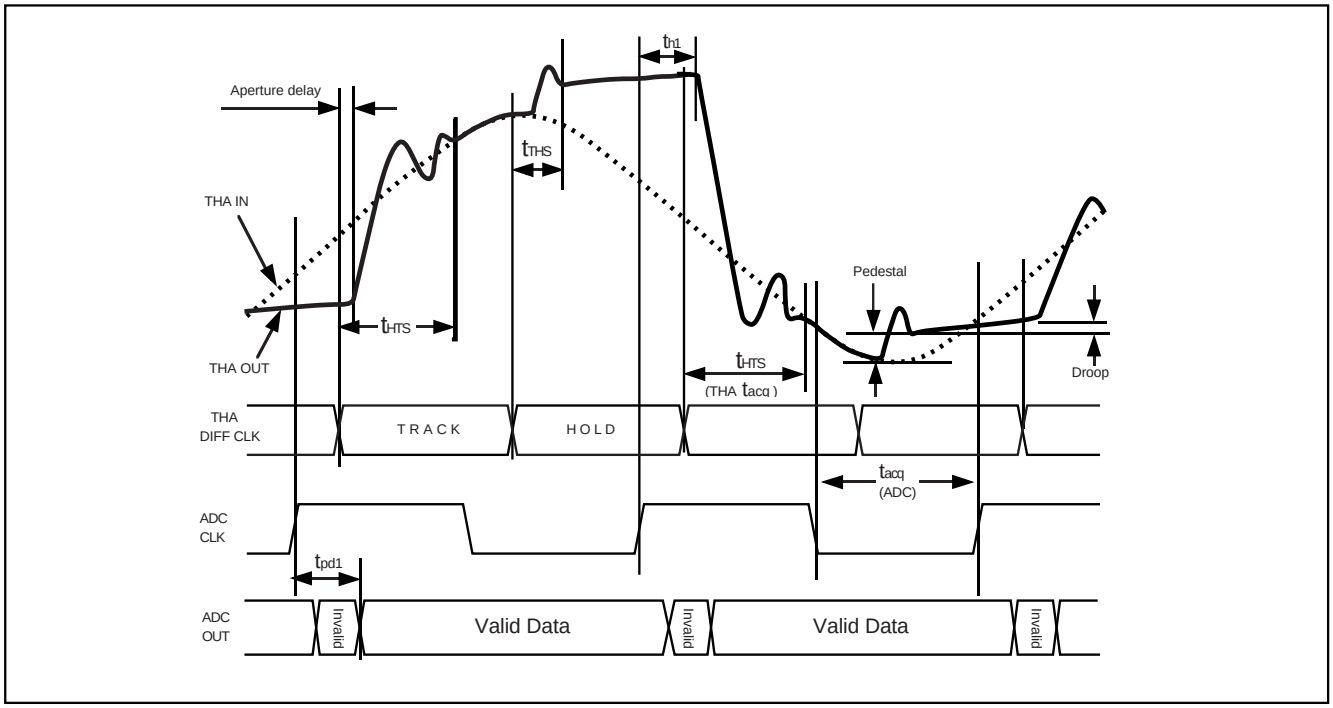


Figure 9. Critical Timing Between External THA and ADC

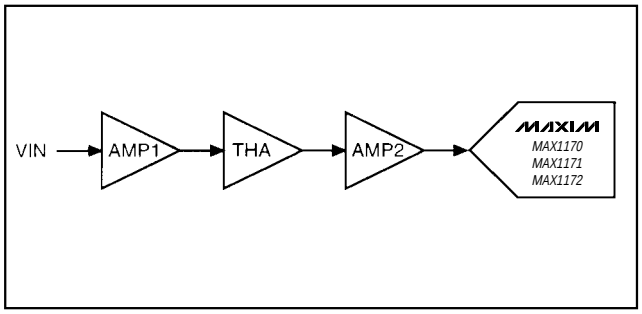


Figure 10. Driving Circuit Block Diagram

Figure 10 shows the typical analog driving circuit. AMP1 and AMP2 are optional. For applications in which noise is the major concern, use AMP1 (disregard AMP2) low-noise amplifier to gain up to ±2V before getting to the THA. In other applications in which high-frequency VIN is the major concern, use AMP2 instead of AMP1 to amplify the THA signal to ±2V before reaching the MAX1170/MAX1171/MAX1172. In the latter case, the low-level VIN provides a faster acquisition time for the THA.

Uncommitted Prototype Area

Two areas are available for applications where additional circuits might be needed to interface with the MAX1170 EV kit (Figure 17). These two areas (labeled A and D in the PCB assembly) are electrically non-committed.

- Area A is located near VIN (BNC), and is intended for the analog interfacing circuit. It has one 16-pin DIP and one 8-pin SIP.
- Area D is located between connectors P2 and P3, and is intended for the digital interfacing circuit. It has three 16-pin DIPs, three 8-pin SIPs, and one 37-pin D connector.

Both areas have the appropriate power supplies and grounds.

Daughterboard (Reconstruction DAC)

Figure 18 is the daughterboard that interfaces directly to the MAX1170 EV kit main board via P2 and P3. It is suited for applications in which the reconstruction DAC is needed to evaluate ADC performance in the time domain. It is designed around a 12-bit TTL, digital-to-analog converter with an 80Msps update rate, set up in

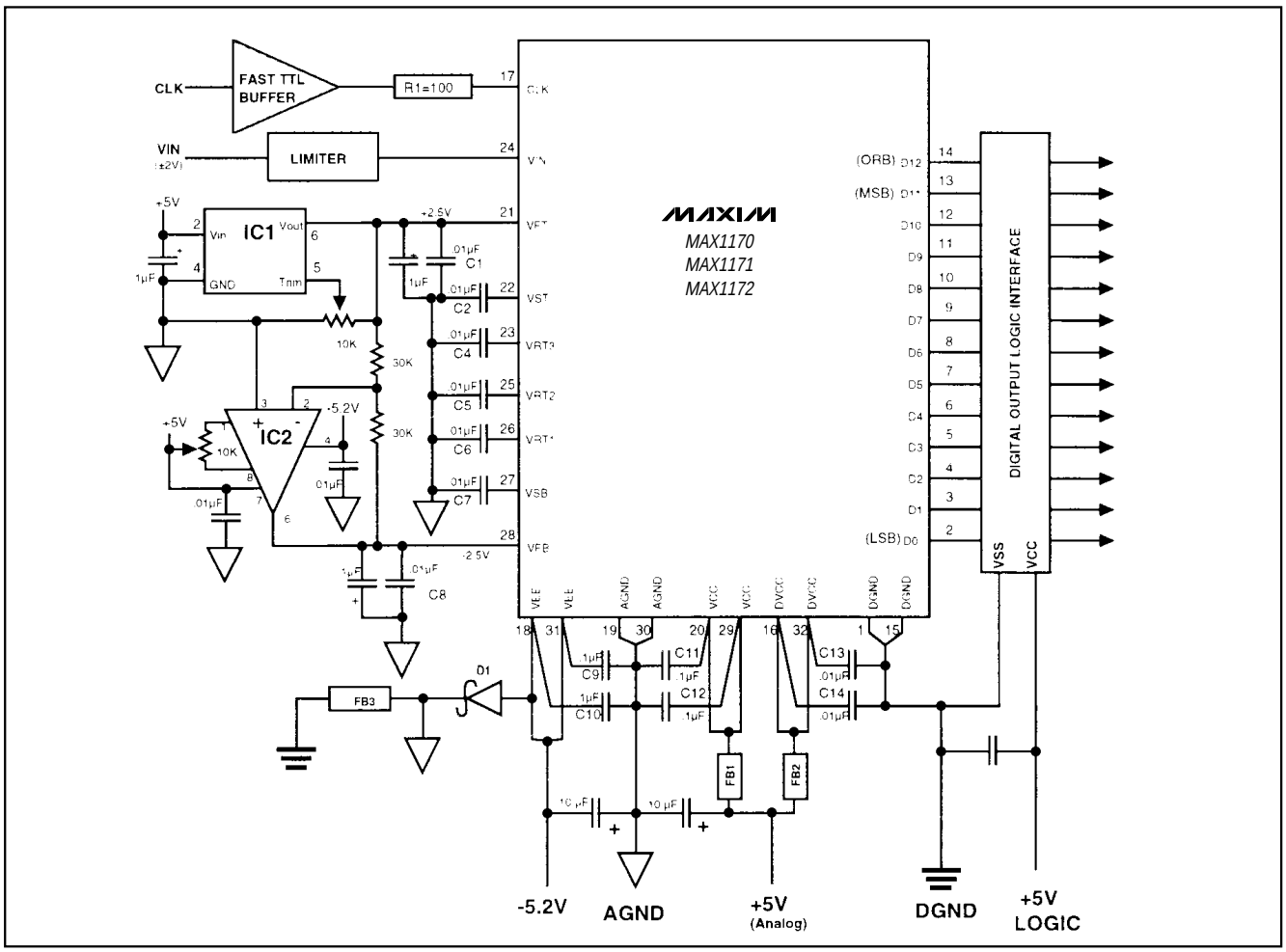


Figure 11. Typical Interfacing Circuit

bipolar operation. The detailed schematic is shown in Figure 18.

Input and Latchup Protection

The MAX1170/MAX1171/MAX1172 are free from latchup when the recommended interfacing circuit is used (Figure 11).

The following information was considered in developing the interface circuit used in the MAX1170 EV kit:

1) Drive the input clock (pin 17) from a TTL logic source (VIH ≤ 4.5V). Fast TTL-family logic or equivalent is strongly recommended due to its 6ns or faster rise time. If the clock is driven from a high-current source (greater than 400mA), use a 100Ω resistor in series to current limit to roughly 45mA.
2) D1 is a Schottky or hot-carrier diode (Motorola, 1N5817, or equivalent) installed between VEE and AGND (reverse bias).
3) Both VCC (pins 20 and 29) and DVCC (pins 16 and 32) are driven from the same +A5V supply.
4) Mount the ferrite beads (FB1 and FB2) as close to the device as possible. The bead to the ADC connections should not be shared with any other device.
5) All reference and power-supply pins must be bypassed as close to the device pin as possible (chip capacitors C1–14 are preferred: 0.1µF for VCC and VEE, and 0.01µF for DVCC).
6) The top reference (VFT) driver must be current limited to 20mA (max) if a different reference-driver

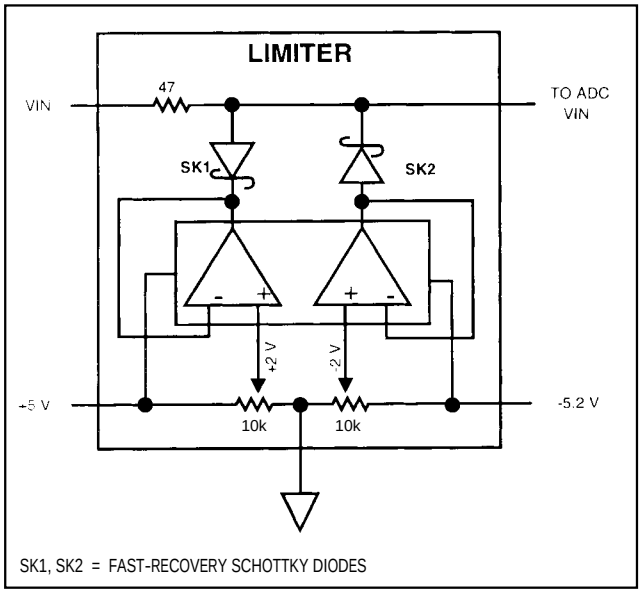


Figure 12. Example of an Input Limiter

circuit is used in place of the recommended circuit (Figure 11).

7) The limiter is required if the analog input's maximum peak-to-peak voltage exceeds ±2.5V. Incorporate this limiter within the analog input driver, or use the circuit shown in Figure 12. Another option is to add a 100Ω resistor in series to current limit the input. This last option adds another LSB error to both plus and minus full scale, compared to only 1/2LSB when using the circuit shown in Figure 12.

Characterization

Performance at speed is the main goal in evaluating any ADC, but it is beneficial to start from a relatively low speed and verify key parameters. It is also beneficial to predict performance at speed. If the device is noisy and/or has poor differential linearity at low frequency, the signal-to-noise ratio (SNR) at speed cannot be expected to be better. In addition, the low-frequency setup can be useful as a verification tool for the test setup.

At low frequency, there are numerous ways to characterize the differential nonlinearity (DNL), integral nonlinearity (INL), transition noise, synchronous noise, nonmonotonicity, power-supply sensitivity, and power-supply currents.

The missing-codes test, INL, DNL, and the gain-error tests are based on statistical results for high-frequency or dynamic testing. These tests can be performed using the histogram technique. SNR and total harmonic distortion (THD) are tested by using the fast-Fourier transform (FFT) method.

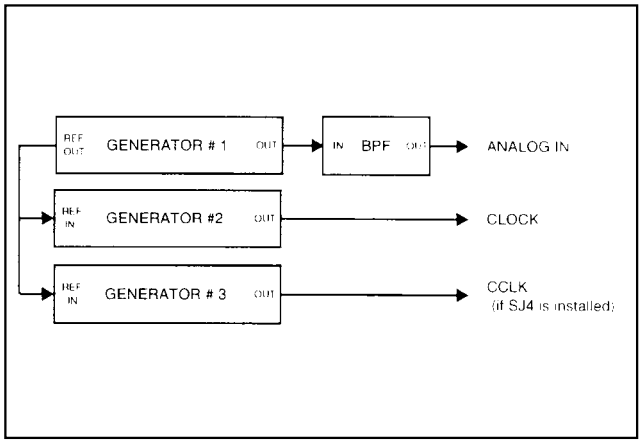


Figure 13. Synchronous Equipment Hookup

The MAX1170 EV kit was designed to provide optimum capability in fulfilling the above characterization needs.

___Equipment Hookup and Testing

Synchronous testing is recommended in characterizing the MAX1170/MAX1171/MAX1172. These techniques significantly reduce testing time (especially dynamic testing). In Figure 13, all three signals (VIN, CLK, and CCLK) are synchronized. Generator 1 is the analog input. Generator 2 is the sampling clock (sine wave, ±3Vp-p maximum). Generator 3 (needed only if solder jumper option SJ4 is used) is the capture clock (TTL). A phase-adjustment option for generator 3 is necessary to place the edge of the capture clock at the proper setup time. R11 and R12 are 51Ω, and serve as termination resistors for generators 2 and 3, respectively (Figure 17).

Signal-Generator Selection

Two parameters are important when selecting generators 1 and 2:

1) The output sine wave must have at least 76dB or better of SNR. An appropriate bandpass filter (BPF) between the analog input and the generator will help improve SNR.

2) The sampling clock jitter or aperture jitter can originate both inside and outside the ADC. Aperture jitter or the uncertainty of clock edge placement can significantly degrade effective bits performance.

This jitter is translated into the ADC amplitude error, and is proportional to the analog input slew rate. Consider the selection of an acceptable clock generator. For a sinusoidal input, the uncertainty of clock-edge placement from cycle to cycle due to equipment jitter affects ADC performance, especially SNR.

SNR (max) = {20log[1 / ($2\pi f_{IN} t_J$)] + 3.02}dB

where: f_{IN} = analog input frequency

and t_J = the aperture jitter in RMS units.

Low-Frequency Performance Check

This section describes an approach to visual evaluation of DNL, nonmonotonicity, synchronous noise, and transition noise. Use DAC OUT (daughterboard, Figure 18) as the monitoring point to view the quality of the quantization signal. Another common approach is to use a 3-bit reconstruction DAC generated from three LSBs (Figure 17). When jumpers SJ9, SJ10, and SJ11 are installed, R30–R33 form a three-bit DAC (Figure 14).

This three-bit reconstruction DAC's output can be viewed through the test point STEP with the scope. For this test, use a function generator for generators 1 and 2 and set up for a ramp output. Replace the BPF with an RC lowpass filter (1kΩ and 0.01µF) to eliminate all high-frequency components. Set this ramp signal's slew rate to 1LSB per n conversions (sampling period) for a desired 1/n test resolution. An n =10 minimum is recommended for this application. The peak-to-peak voltage and the ramp input period are then dependent on the selection of the number of steps (LSBs) within one ramp's period. Note that R10 (51Ω) may need to be removed. Set CLK and CCLK to the same relatively low frequency (approximately 1MHz or slower). Make adjustments to meet the t_{PWH} and t_S specifications. (See Figures 5 and 6; also see Table 6.)

The following formulas summarize the criteria for selecting the analog ramp input signal:

Ramp peak-to-peak voltage: Vp-p = m(FSR / 1024)

Ramp period: t = (m)(n) / f_S

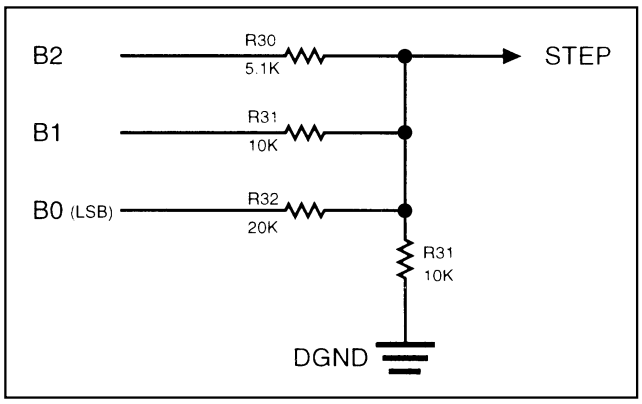


Figure 14. Three-Bit Reconstruction DAC

where: m = desired number of steps (LSBs) per ramp period

f_S = sampling frequency

FSR = full-scale range (the MAX1170's FSR is typically 4V)

n = desired test resolution or the number of conversions / LSB

Example:

1) The MAX1170 is operated at 500kHz (sampling frequency).
2) One-tenth of the test resolution is desired.
3) The scope is externally triggered to the ramp input. Three retraces of eight-level steps (or 24 total steps) per ramp's period are selected.

   What peak-to-peak voltage (Vp-p) and the ramp input signal period (T) are required to drive the MAX1170?

Answer:

1) f_S = 500kHz
2) n = 10
3) m = 24, then Vp-p = m(FSR / 4096) = 24(4 / 4096) = 23mV
   and T = (m)(n) / f_S = (24)(10) / 5,000,000 = 480µs

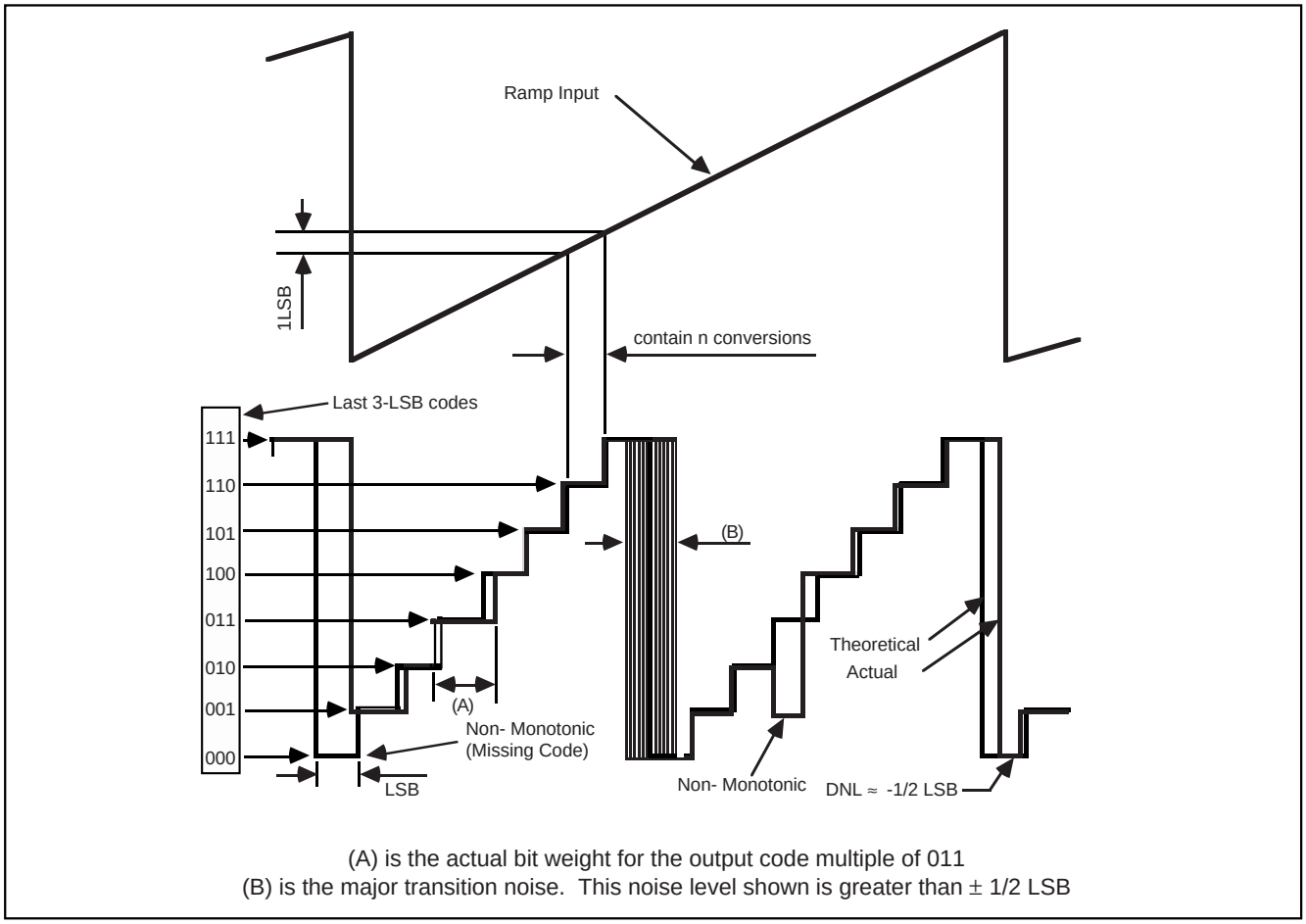


Figure 15. Three-Bit Reconstruction DAC Waveform Using Analog Input Ramp

Figure 15 shows the relationship between the analog input ramp signal and the resulting three-bit reconstruction DAC. It shows 16 LSBs of peak-to-peak input voltage (i.e., two eight-level steps) per period. For an ideal ADC and an ideal ramp input, its digital output code changes state by 1LSB every (n)th conversion (dash line in the transfer curve). Any error in the ADC makes the corresponding output codes change their state before or after the (n)th conversion. This error translates into smaller or larger respective step width. The DNL is judged visually by comparing the actual step size with respect to the ideal step with ±(1/n)LSB of accuracy. In this case, the ideal step is the average of the step size. Other errors (transition noise, nonmonotonicity) can be resolved similarly. Figure 15 also gives the identification of each error from the actual transfer curve.

Note that the above input signal only covers 24 parts in 1024 of the FSR. To identify all errors through the full-scale range, sweep the ramp input from -FS to +FS slowly and observe the output steps for transition noise, DNL, and nonmonotonicity, as indicated in the transfer curve (Figure 15). Most generators do not have DC offset covering the +2.5V to -2.5V range. You may need to construct an additional circuit using a summing amplifier to DC-offset the above ramp input signal.

Synchronous noise is the distortion of the device's performance (normally, the DNL can be clearly observed) when the sampling frequency varies. This is usually caused by the digital signals being coupled back internally into the analog input signal. This problem is common for ADCs using the successive-approximation register (SAR) architecture. An ADC with this type of symptom presents some weak performances at a

specific sampling frequency (within the specified sampling rate), but shows better results when the sampling frequency is varied up or down from that weak spot. To verify synchronous noise using this setup, slowly change the sampling frequency and observe the transfer curve, especially the changes in DNL.

Advantages

1) Many tests (as stated above) can be extracted from this simple test setup.
2) The missing code and transition noise can be more accurately identified than with any other standard test method.
3) Setup is quick and relatively accurate.

Disadvantages

1) Accuracy depends on the individual's judgment, and is limited to the interpretation of the oscilloscope's display.
2) The transfer curve does not show the exact code, but rather a multiple of the last three bits. To overcome this problem, probe every bit using an oscilloscope, or install LEDs at each output P3 connector to signal each output bit's state.

Dynamic Testing

Figure 16 is the recommended functional diagram suitable for dynamic testing of the MAX1170/MAX1171/MAX1172 using the MAX1170 EV kit. A common practice is to use the DAC OUT signal to analyze the ADC's dynamic performances (SNR and THD) through a spectrum analyzer. This method of testing presents some uncertainties. The DAC must be glitch-free, and its dynamic accuracy (DNL and INL) must be far better than the ADC under test. Any errors in the DAC are added to the total SNR and/or THD.

It is preferable to perform these tests using digital-signal processing (DSP). Numerous standard software packages are available to service this application. The MAX1170 EV kit provides the data outputs through P2 (Table 5). The reconstruction DAC output can be obtained from the daughterboard.

In many cases, the capture memory is much slower than the available valid data of the ADC under test. It is then necessary to decimate the capture clock at a rate of $f_S / 2^n$. The beat frequency can be achieved by changing the analog input frequency slightly by an amount of Δf_{IN}. For a 4096-point FFT, the beat frequency of $\Delta f_{IN} = f_C / 4096$ is added to (or subtracted from)

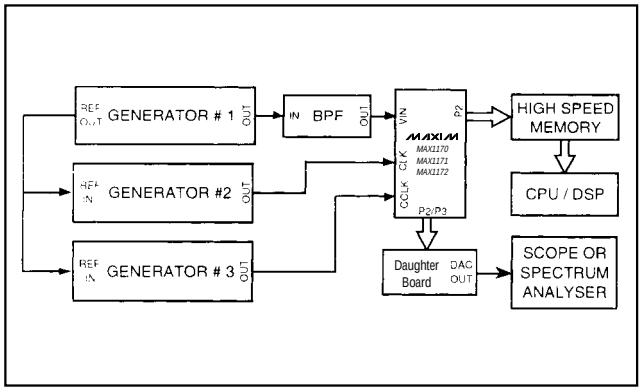


Figure 16. Dynamic Testing Test Setup

the analog input frequency. 4096 data points are filled in one test period where the input is at $f_{IN} \pm (f_C / 4096)$ and the output is updated at a $1 / f_C$ interval. Select f_{IN} to be the multiple (integer) of f_C to achieve complete system synchronization. Both capture memory and the DAC run at a relatively low update rate ($f_S / 2^n$). The daughterboard can update up to 80Msps.

Calibration

For every new MAX1170/MAX1171/MAX1172 installed, VST and VSB voltages must be recalibrated. Check for installation of the following jumpers: SJ2B, SJ2C, and SJ3.

I) Equipment Needed

1) Four DC power supplies: +A5V, -A5.2V, +D5V, and -D5.2V
2) Function generator
3) DVM with 5.5-digit precision
4) Oscilloscope

II) Equipment Setup/Hookup

1) Ensure that the U1 socket does not contain the ADC at this point.
2) Connect all four power supplies as shown in Table 1 and Figures 2 and 3.
3) Connect the function generator to CLK BNC.
4) Set the CLK to 3MHz, sinewave, ±2V.
5) Connect VIN to AGND.

III) References Calibration

1) Monitor TP1 with respect to AGND test point with DVM.
2) Adjust R1 for +2.500V at TP1.
3) Monitor TP2 with respect to AGND test point with DVM.
4) Adjust R2 for -2.500V at TP2.
5) Turn all power off.
6) Install the ADC into the U1 socket (repeat this procedure for all new devices).
7) Turn all power back on.
8) Monitor U1, pin 22 (VST) with respect to AGND test point with DVM.
9) Adjust R1 for +2.000V at VST.
10) Monitor U1, pin 27 (VSB) with respect to AGND test point with DVM.
11) Adjust R2 for -2.000V at VSB.
12) Repeat the procedure from number 8 until VST and VSB reach the desired voltages (±2.000V, respectively).

IV) Clock-Circuit Calibration

1) Monitor PJ1 with scope on channel 1 (externally sync to the generator).
2) Observe the TTL clock and adjust R3 for approximately 50% of duty cycle.

V) Latches (U7 and U8) Test

1) Remove R10.
2) Connect VIN to TP1.
3) Monitor P2, odd-numbered pins (3–25) with scope and observe TTL logic high on all pins.
4) Connect VIN to TP2.
5) Monitor P2, odd-numbered pins (3-25) with scope and observe TTL logic low on all pins.

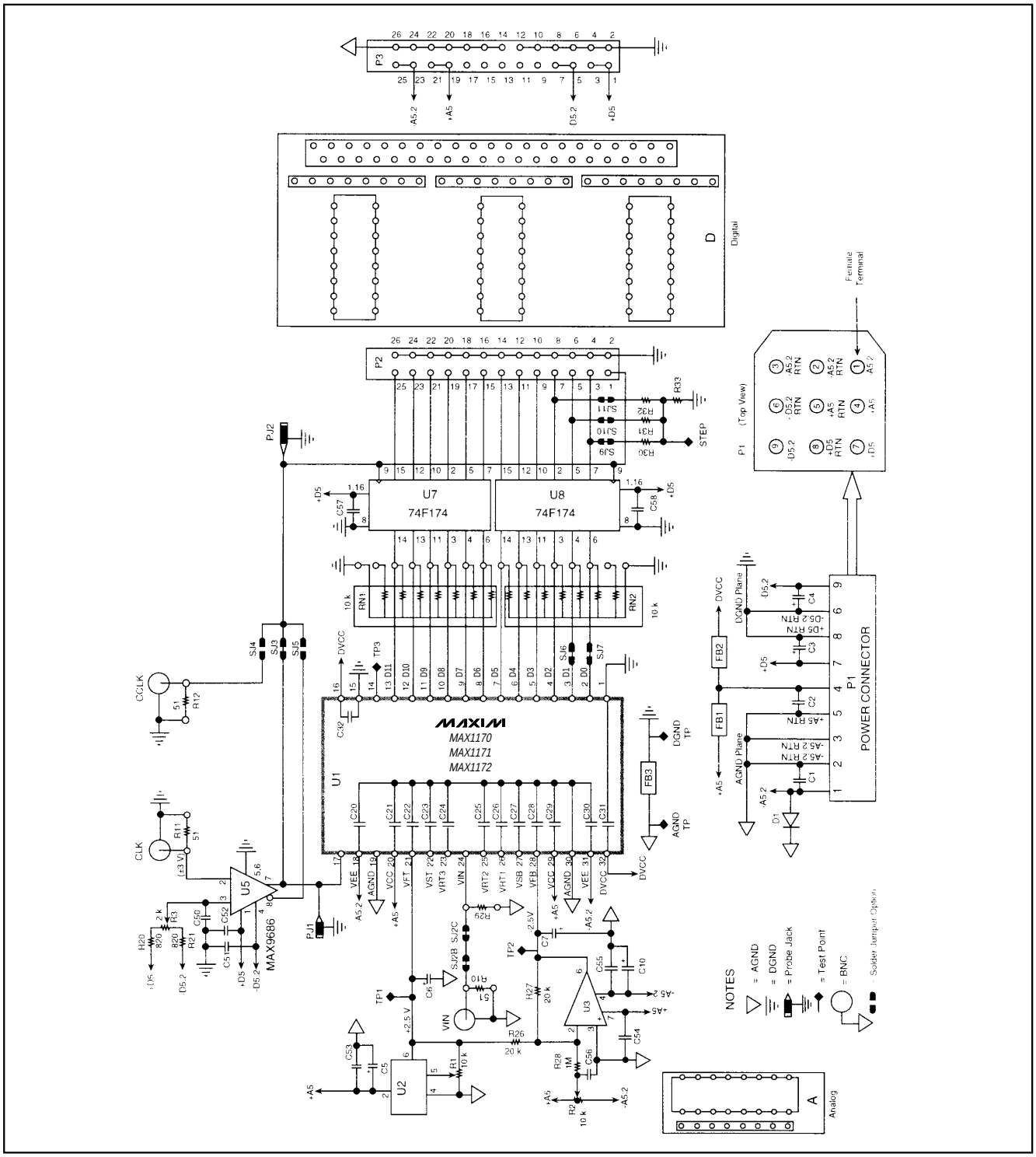


Figure 17. MAX1170 EV Kit Detailed Schematic

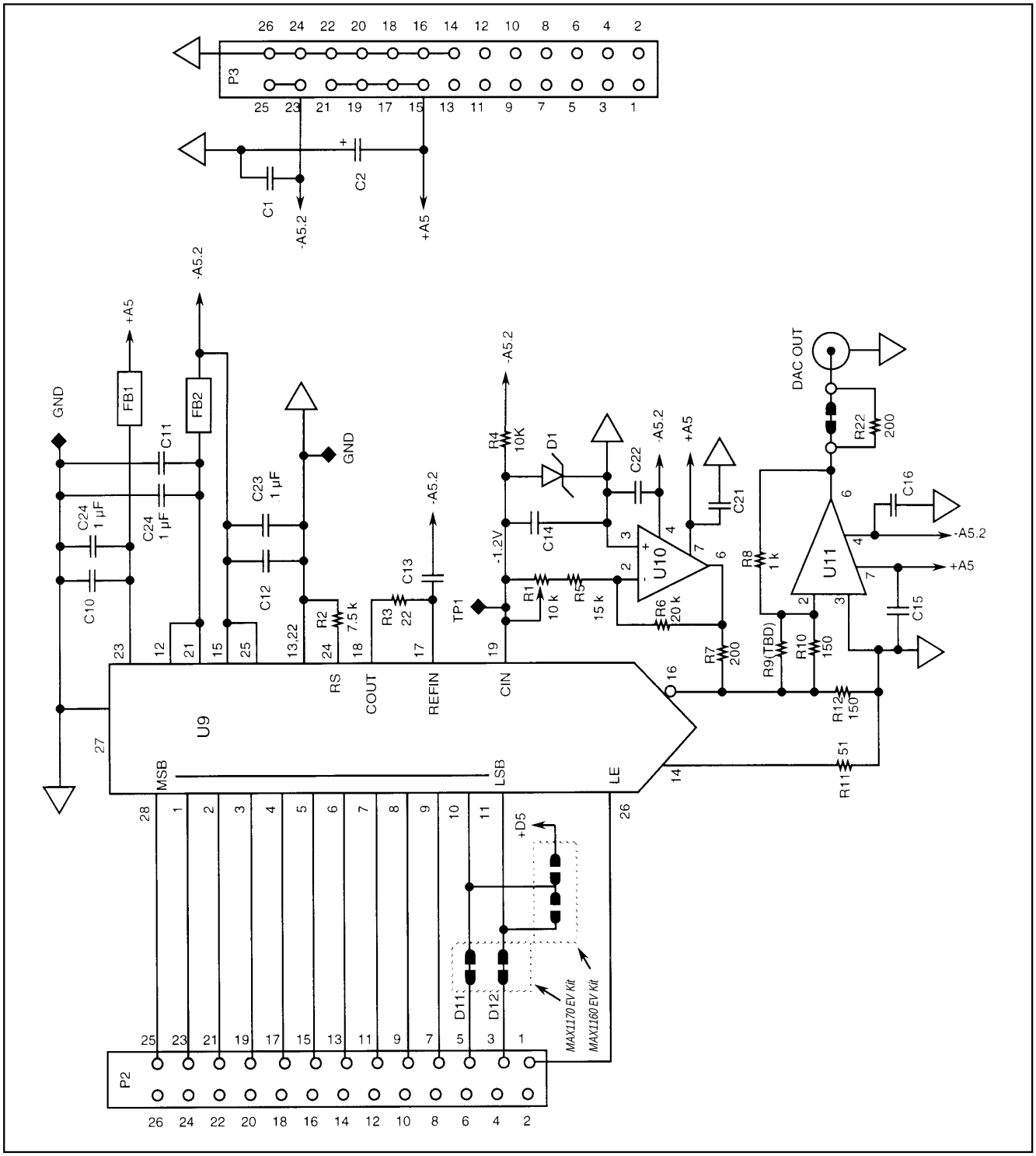


Figure 18. Daughterboard EV Kit Detailed Schematic

NOTES

NOTES