19-1199; Rev 0; 3/97

MAXIM

MAX1150/MAX1151 Evaluation Kit

General Description

The MAX1150/MAX1151 evaluation kit (EV kit) is a tool for device characterization and demonstration of the performance of the MAX1150/MAX1151 8-bit analog-to-digital converters (ADCs). Guaranteed minimum sample rates for the devices are 500Msps for the MAX1150 and 750Msps for the MAX1151. The evaluation kit contains the ADC, reference circuitry, full-speed and selectable decimated digital data outputs, and an on-board reconstruction DAC.

The MAX1150/MAX1151 EV kit comes with the MAX1150AIZS or MAX1151AIZS in an 80-pin, MQUAD, surface-mount package directly soldered to the board for optimum performance. The MAX1150/MAX1151 EV kit operates at clock rates up to 750Msps.

Applications

Evaluation of MAX1150/MAX1151 8-bit ADCs

Engineering System Prototype Aid

Guide for MAX1150/MAX1151 Interface Circuitry Design

Guide for MAX1150/MAX1151 PC Board Layout Design

Features

- **750Msps Maximum Conversion Rate (MAX1151)**
- **On-Board Reconstruction DAC**
- **On-Board Reference Circuit**
- **Full-Speed Digital Output Through a High-Speed Connector**
- **Decimated Digital-Data Output**
- **Selectable-Decimation, Divide-by-32/64/128 Options**
- **On-Board Gray-to-Binary Conversion**

Special Requirements

The MAX1150/MAX1151 require adequate heatsinking and air flow for optimum performance.

Ordering Information

PART	TEMP. RANGE
MAX1150EVKIT	0°C to +70°C
MAX1151EVKIT	0°C to +70°C

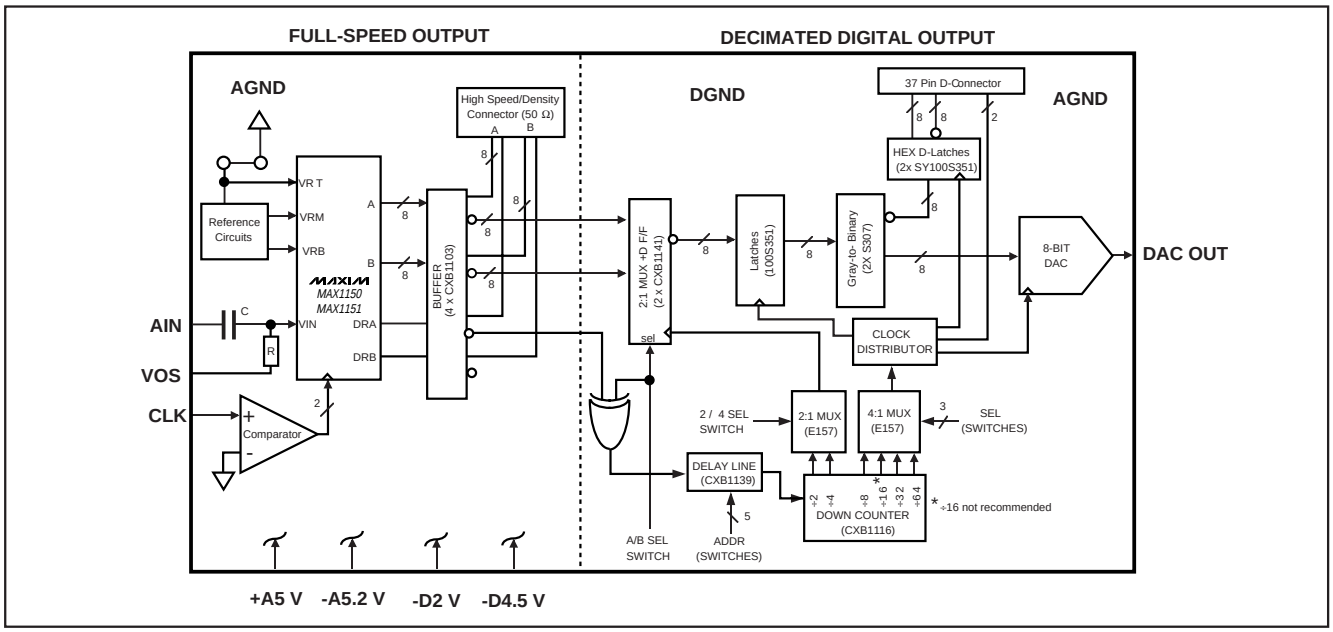


Figure 1. Block Diagram

Component List

DESIGNATION	QTY	DESCRIPTION
C1–C19, C99	20	10µF, 25V, 0.10" tantalum capacitors
C20	1	0.1µF ceramic capacitor
C21–C48, C51–C95	73	0.1µF chip capacitors
C131–C145	15	0.100pF chip capacitors
D1, D2	2	Si diodes
D3	1	3.9V, lead-mount zener diode
FB1–FB5, FB7 FB8, FB9	8	Ferrite beads Digi-Key P98208BK, or equivalent
P1	1	50Ω, controlled-impedance, high-speed, high-density, 40-pin vertical connector AMP 121286-3
P1 (cabling)	1	50Ω, controlled-impedance, 1'-long, high-speed, high-density, 40-pin cable assembly AMP 340003-1
P3	1	37-D connector
Q1	1	PNP transistor
R1	1	2k, 12-turns potentiometer
R2	1	200Ω, 12-turns potentiometer
R4	1	10k, 12-turns potentiometer
R7	1	1k, 1/8W, 5% resistor
R8	1	51Ω, 1/8W, 5% resistor
R9	1	470Ω, 1/8W, 5% resistor
R10, R19, R20, R22	4	120Ω, 1/8W, 5% resistors
R11	1	3kΩ, 1/8W, 5% resistor
R12, R13	2	5.1kΩ, 1/8W, 5% resistors
R14	1	56Ω, 1/8W, 5% resistor
R15, R16	2	22Ω, 1/8W, 5% resistors

DESIGNATION	QTY	DESCRIPTION
R25–R75, R78–R83, R86–R144	116	49.9Ω chip resistors
RN13, RN14	2	16 DIP, 47Ω resistors CTS, 761-3-R47 or equivalent
S0–S4, S10–S13	9	V3-outline SPDT switches
A/B SEL	1	V3-outline DPDT switch
U1	1	Dual op amp (8 DIP)
U2	1	Dual VHS comparator (20 PLCC)
U3	1	DUT (80 MQUAD)
U4–U7	4	Formed-lead, quint line receivers (24 QFP)
U8, U9	2	Formed-lead, hex 2:1 multiplexers plus D-FF (32 QFP)
U10	1	3-lead negative regulator (TO-220)
U11	1	Formed-lead, programmable delay line (24 QFP)
U12, U13	2	Formed-lead, 4-bit ripple counters (24 QFP)
U14	1	J-lead, quad 2:1 multiplexer (28 PLCC)
U15	1	Quad driver (24 DIP)
U16	1	Formed-lead, quad X-OR/NOR (24 QFP)
U18–U21	4	Hex D-F/Fs (24 DIP)
U22, U26	2	Quint X-ORs (24 DIP)
U24	1	275Msps video DAC (24 CERDIP)
N/A		BNC connector
N/A	12	Banana jacks (various colors)
N/A	13	Test points
N/A	10	Pin sockets
N/A	1	Heatsink

MAX1150/MAX1151 ADCs—Overview

The MAX1150 analog-to-digital converter (ADC) has a guaranteed 500Msps (min) sample rate, and the MAX1151 has a guaranteed 750Msps (min) sample rate. Only one -5.2V power supply is required. Two external references are applied across the 80Ω (typ) internal reference ladder.

The top reference is either 0V (typ), or connected to analog ground (AGND). The device's top force and sense pins (VRFT and VRST) are connected together internally. These voltage force and sense pins can be used to compensate for voltage drop.

The bottom reference is typically -2V. The device also has internally connected bottom force and sense pins (VRFB and VRSB). These can also be used to compensate for voltage drop.

All logic levels are compatible with both 10k ECL and 100k ECL. It is recommended that the clock input be driven differentially (CLK and NCLK) to improve noise immunity and reduce aperture jitter.

The digital outputs are split into two banks of 8-bit words and an overrange bit. The banks are alternately updated at one-half of the input clock rate. The differential data-ready signals for each bank are provided to accurately latch each data bank into the register. The output data is in gray-code format. Figure 2 is a timing diagram for the MAX1150/MAX1151, and shows the input-to-output relationship, clock-to-output delay, and output latency.

The full-scale analog input bandwidth is 500MHz (900MHz, for small-signal bandwidth), well above the converter's Nyquist frequency. Input capacitance is typically 15pF.

Power dissipation is specified at 6.25W (max) at Tj = +25°C. **Adequate air flow and a heatsink are required.** The data sheet provides the information necessary for heatsink selection, and indicates the required air-flow rates. Refer to the *Thermal Management* section of the MAX1150 or the MAX1151 data sheet.

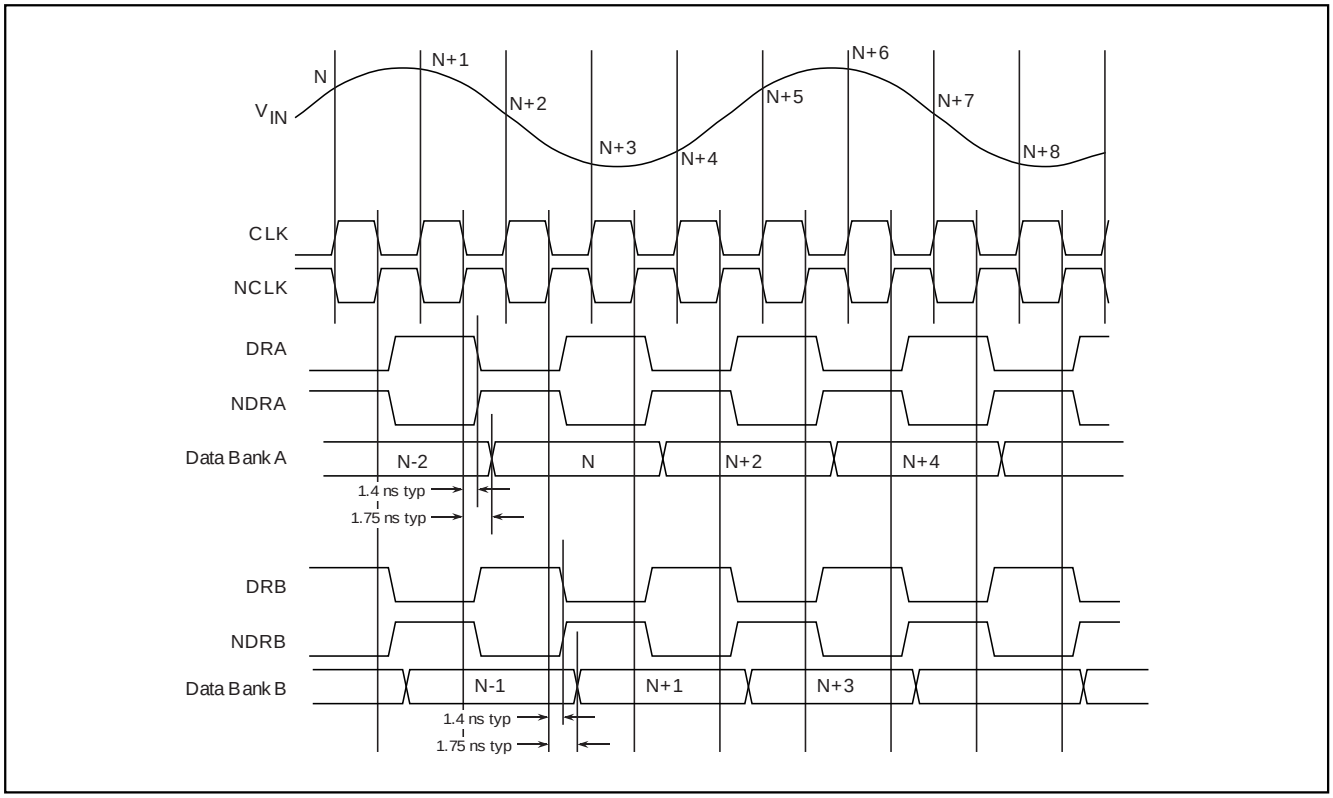


Figure 2. MAX1150/MAX1151 Timing Diagram

Detailed Description

Power Supplies and Grounding

Reference all interfacing circuits to the appropriate grounds to optimize performance and minimize ground loops. Reference the analog input, the clock input drivers, and the reference to AGND. Reference digital output loads, and all logic interfacing circuits to DGND. Figure 1 indicates where AGND and DGND are split. AGND and DGND are tied to each other through a ferrite bead as closely to the converter as possible.

The MAX1150/MAX1151 EV kit requires four power supplies (Table 1). An additional -1.0V supply provides offset to the analog input.

Table 2 shows the initial setup of the board jumpers and DIP switches.

Table 1. Power-Supply Requirements

SUPPLY	VOLTAGE RANGE (V)			TYPICAL CURRENT
	MIN	TYP	MAX	
+A5V	+4.80	+5.0	+5.2	10mA
-A5.2V	-4.95	-5.2	-5.45	1.5A
-D2V	-1.95	-2.0	-2.2	2.2A
-D4.5V	-4.20	-4.5	-4.8	2.1A

Table 2. Initial Setup

OPTION JUMPERS	STATUS	SWITCH	STATUS
J2	Short	A/B SEL	LO or HI
J3	Short	S0	HI
J4A	Short	S1	HI
J4B	Short	S2	LO
J5A	Open	S3	LO
J5B	Open	S4	LO
J6	Open	S10	HI
J7	Short	S11	X
J8	Open	S12	HI
—	—	S13	HI

X = Don't Care

Figure 3 is the recommended EV board power-supply hookup. It is recommended that all of the power supplies be turned on and off at the same time via a power strip.

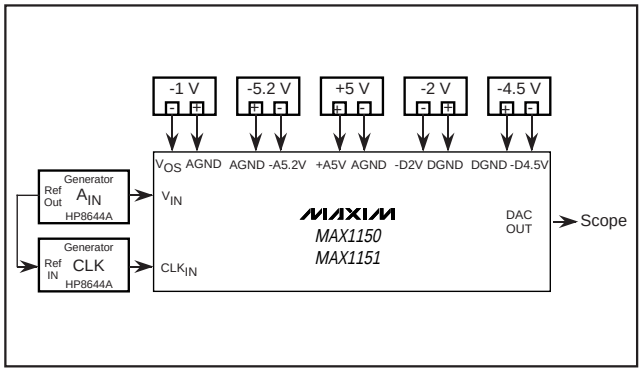


Figure 3. Power-Supply Configuration

Verifying Board Operation

The following procedure enables verification of correct board operation:

1) Connect power supplies and generators (leave off).
2) Set jumpers and DIP switches to the appropriate configurations (Table 2).
3) Turn on clock generator and set to 499.712MHz and 2Vp-p.
4) Turn on analog input generator and set to 3.965MHz and 2Vp-p.
5) Turn all power supplies on and observe the 61kHz sine wave at the scope (64 points/period).

Refer to the *Beat-Frequency Technique* section for more details.

Reference Circuit

D3, a 3.9V zener diode, is used to generate the base reference voltage (Figure 9a). Potentiometers R4 and R11 are used as an adjustable voltage divider to generate -2.0V at the REF test point. This voltage is then buffered with U1B and drives emitter follower Q1. The emitter follower is necessary to sink up to 33mA through the reference ladder (based on a 2V reference and a 60Ω minimum ladder resistance).

The top reference is connected to AGND if J2 is installed. The top reference can be driven externally through test point TF (with respect to AGND) and by removing jumper J2.

The MAX1150/MAX1151's reference-ladder middle tap is brought out to the VRM pin. The voltage at VRM must be centered between VRTF and VRBF. The U1A circuit provides the voltage to VRM. This circuit forces the midpoint of the ladder to the theoretical value (VRBF - VRTF) / 2.

A 10µF decoupling capacitor in parallel with 0.1µF and 100pF surface-mount capacitors is recommended to bypass all reference pins (VRTF, VRM, and VRBF).

Reference Calibration

The following is the reference calibration procedure:

1) Monitor the SB test point (referenced to AGND) with DVM, and adjust R4 for -2.000V ±5mV.
2) Measure VFT and VFB with respect to AGND, and record them for VRM calculation.
3) Monitor test point RM with DVM (referenced to AGND), and adjust R1 for (VFB - VFT) / 2.

Analog Input

The MAX1150/MAX1151 require an op amp with suitable drive, a bandwidth of at least 500MHz, and at least -50dB of distortion. With 15pF input capacitance, the required peak driving current is $2\pi fC$ = 23.6mA, for f = 250MHz (Figure 4a).

For AC input into the MAX1150/MAX1151 EV kit, connect the analog input into the VIN BNC. C20 is the AC input coupling capacitor. Applying -1.0V to the V_{OS} test point (referenced to AGND) offsets the input to meet the ADC's 0V to -2V input range.

If DC input is required, inject the analog input through test point VOS and place a ground capacitor on the VIN BNC. Figure 4b shows the DC-coupled input circuit with this configuration. Note that C20, R9, and R14 are socketed.

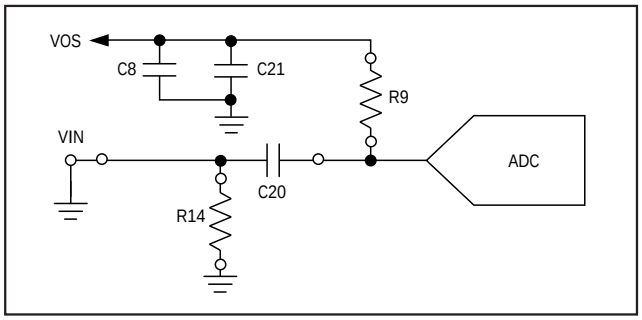


Figure 4a. AC Input Configuration

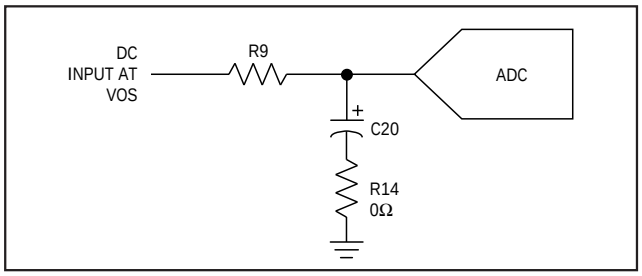


Figure 4b. DC-Coupled Input Configuration

Clock Circuit

The clock input driver uses comparator U2 to convert a sine-wave symmetrical around zero to a differential ECL output. U10 is a -2V regulator (from analog -5.2V), used only for U2 output load pull-down. Note that the clock circuits are biased from the analog supply. This is critical to maintaining optimum performance.

CLK and NCLK test points are provided on-board (Figure 9a). The layout of the test points provides a short ground path to the scope probe's ground.

The U2 input common-mode range is specified from -2.5V to +4V. Input offset for the grade B part is ±30mV (max). To minimize jitter and to keep the input clock duty cycle at 50%, the external clock input signal should be symmetric around 0V, with a ±1Vp-p (min) to ±2Vp-p amplitude.

MAX1150/MAX1151 Calibration Summary

1) Hook up power supplies as shown in Figure 3.
2) Refer to Table 2 for jumper/switch setup.
3) Switch on all power supplies.
4) Monitor -A2V test point with DVM, with respect to AGND.
5) Adjust R2 for -2.00V ±0.010V.
6) Monitor test point SB with DVM, with respect to AGND.
7) Adjust R4 for -2V ±0.004V.
8) Monitor test point RM with DVM, with respect to AGND.
9) Adjust R1 for (VFB - VFT) / 2 (note that the additional measurements of VFB and VFT are required.)

Digital Output Buffer and High-Speed Connector

The MAX1150/MAX1151 require a digital output buffer directly tied to the digital outputs. All digital outputs are pulled down to digital -2V (-D2V) through 49.9Ω resistors.

U4–U7 are CXB1103QYs, which are Sony SPECL Standard logic, quint line receivers with differential I/O in QFP packages. These, as well as all the digital logic on the board, require a power-supply voltage of -4.5V ±0.3V. The ADC's digital output buffer bank B (D0B–D8B, and DRB) is input into U4 and U5, and output buffer bank A (D0A–D8A, and DRA) is input into U6 and U7.

All the buffered outputs (from U4–U7) are brought out through connector P1. P1 is a 40-pin, very-high-speed, high-density, 50Ω controlled-impedance connector. Reflections at 1GHz are less than 5%, and crosstalk with 1ns rise time is less than 4%. Figure 5 shows the connector outline.

A 49.9Ω pulldown resistor to -2V is required for termination on each line at the receiving end.

The MAX1150/MAX1151 EV kit is shipped with a one-foot, high-speed cable with a high-speed connector for the user's receiving end. The update rate at DRA and DRB is CLKIN / 2.

The P1 output data format is gray code. A four-bit gray-code table is included in Table 3 for reference.

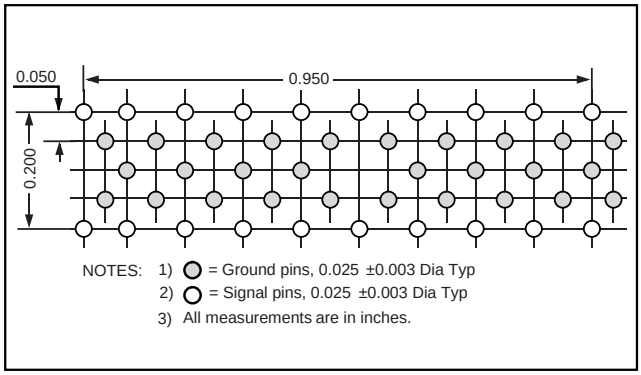


Figure 5. P1 Connector Outline

Table 3. Gray-to-Binary Conversion

DECIMAL	GRAY	BINARY
0	0000	0000
1	0001	0001
2	0011	0010
3	0010	0011
4	0110	0100
5	0111	0101
6	0101	0110
7	0100	0111
8	1100	1000
9	1101	1001
10	1111	1010
11	1110	1011
12	1010	1100
13	1011	1101
14	1001	1110
15	1000	1111

Decimation Circuit

Decimation enables the user to look at a periodically subsampled portion of the output through a divide-down scheme. Figures 9a, 9b, and 9c show the decimation-circuit schematic.

In this design, the decimation function is achieved in a two-stage process to minimize the impact of decimation-circuit jitter. The first stage of the two-stage design performs a small divide-down with very precise data-stream time slicing. Precise time slicing is important because jitter, rise times, and part-to-part variations are critical in this stage of the decimation circuit. The second stage performs the desired division with greatly reduced timing constraints. Figures 10 and 11 are detailed timing diagrams.

The first stage receives the data at speed and divides down the data stream by either ÷2 or ÷4. U8 and U9 (Sony CXB1144QY 2:1 muxes followed by D flip-flops) gate the data stream. Bank A or bank B is selected by the A/B SEL switch (low = bank A; high = bank B).

U12 and U13 (Sony CXB1116QY) are 4-bit ripple binary down counters set up as a cascade to decimate the data ready by 8/16/32/64 or the input clock by 16/32/64/128 (÷16 is not recommended). U11 (Sony CXB1139QY) is a programmable delay line, and is placed in front of this cascaded counter so that the rising edge of the clock for U8 and U9 may be adjusted to meet the required setup and hold times for U8 and U9 (t_S = 100ps min; t_H = 150ps min).

Setup and Hold-Time Adjustments

To set the proper setup and hold times for U8 and U9 (first decimation stage), use the following procedure:

1) With a high-bandwidth oscilloscope, monitor test point CL1A or CL1B, and either test point ND0A if A/B SEL = 0 or test point ND0B if A/B SEL = 1.
2) Adjust DIP switches S0–S4 to meet the required setup and hold times (t_S = 100ps min and t_H = 150ps min). Table 4 shows the typical propagation delays achieved out of U11 using S0–S4. Note that the decimal value of S0–S4 (N) must be from 1 to 23 for correct operation.

U14 (Synergy SY100E157) is a quad 2:1 multiplexer (mux) with separate select lines. U14A selects the data-ready source for the first stage of decimation (at U8 and U9). Switch S10 controls the selection of either ÷2 (S10 = 0) or ÷4 (S10 = 1).

Table 4. Delay-Line U11 Propagation Delays

DECIMAL VALUE (N)	S4	S3	S2	S1	S0	U11 TYPICAL PROPAGATION DELAY (ps)
0	0	0	0	0	0	Not valid
1	0	0	0	0	1	775
2	0	0	0	1	0	915
3	0	0	0	1	1	1015
4	0	0	1	0	0	1175
5	0	0	1	0	1	1305
6	0	0	1	1	0	1405
7	0	0	1	1	1	1595
8	0	1	0	0	0	1795
9	0	1	0	0	1	2010
10	0	1	0	1	0	2165
11	0	1	0	1	1	2385
12	0	1	1	0	0	2580
13	0	1	1	0	1	2800
14	0	1	1	1	0	2950
15	0	1	1	1	1	3165
16	1	0	0	0	0	3295
17	1	0	0	0	1	3510
18	1	0	0	1	0	3665
19	1	0	0	1	1	3880
20	1	0	1	0	0	4080
21	1	0	1	0	1	4295
22	1	0	1	1	0	4455
23	1	0	1	1	1	4650
≥24	Not valid					

The second stage of decimation occurs at U18 and U19 (Synergy SY100S351), which are hex D flip-flops. Their decimation clocks are selected by U14B-C (Table 6).

U15 (Synergy SY100S313) is set up as the clock distributor. Test points CL2A, CL2B, and DL1 are provided to verify correct setup and hold times for U18 and U19 (t_S = 500ps min and t_H = 550ps min). Clocks CL2A and CL2B have no phase adjustment because the speed and update rates are fairly slow at this stage of the circuit, and the design takes care of any timing issues.

Table 5. Logic Propagation Delay

LOGIC PROPAGATION DELAY (ps)			
PART	MIN	TYP	MAX
CXB1102Q; U16	380	520	670
CXB1103Q; U4–U7	310	410	520
CXB1116Q; U12, U13	—	—	—
OUT0	540	730	940
OUT1	680	910	1116
OUT2	830	1110	1410
OUT3	940	1260	1600
CXB1139Q; U11	775	—	4650
CXB1141Q; U8, U9	650	900	1170
100E157; U14	220	380	550
100S307; U22, U26	200	—	1100
100S313; U15	200	—	850
100S351; U18–U21	—	—	1400

Table 6. Decimation-Clock Selection (U14B-C)

S11	S12	S13	DECIMATION FACTOR (N) WITH RESPECT TO DATA-UPDATE RATE
0	X	0	16*
1	X	0	32
X	0	1	64
X	1	1	128

**Not recommended*
X = Don't Care

Gray-to-Binary Converter

Figures 9a, 9b, and 9c show the gray-to-binary converter (GBC) circuit schematic. U22 and U26 (Synergy SY100S307) are quint exclusive OR/NOR gates. They are set up as a gray-to-binary converter. The G0–G7 digital inputs are in gray code, and the B0–B7 digital outputs are in binary code.

There are seven logic-propagation delays between B7 and B0. The SY100S307 gate has a 1ns typical logic-propagation delay. Due to decimation, G0–G7 have a maximum update rate of 47MHz (T = 21ns), assuming f_{CLK} = 750MHz. Given the 21ns of valid input data at G0–G7 and the 7ns propagation delay through the GBC logic (the longest path), there will be 7ns out of 21ns of invalid data in the GBC circuit output.

Decimated Digital Output Data

The binary code is latched by U20 and U21 before being brought out to P3, which is a 37-pin D connector. (The latch circuit takes into account the invalid phase of the data output from the GBC described in the *Gray-to-Binary Converter* section.) The data lines at connector P3, including the decimating-clock output, are differential. Add a 47Ω or 49.9Ω resistor in series with each signal line to damp out the transients due to long cabling lengths. The differential clock to P3 (CCLK5 and CCLK6) phase can be inverted by selecting jumpers J5A and J5B, instead of J4A and J4B.

Decimated Reconstruction DAC

The decimated encode signal can be viewed through DAC OUT BNC. U24 (SPT HDAC10181 or SPT1019) is a 275Msps, 8-bit video DAC. It is set up for a fixed gain with an output range from 0mA to -9.5mA into a 51Ω load (R8 socket), or 0mV to -480mV. A larger output voltage range can be attained by replacing R8 with a larger value, as long as the output stays within the -1.2V output compliance voltage range.

Board Layout and Design Considerations

Both Microstrip and Strip Line PC board technologies have predictable characteristic impedances that can be controlled to within 5%. Figure 6 shows each technology's basic cross section. For G-10 dielectric material, the line's propagation delay is typically 148ps/in for Microstrip and 188ps/in for Strip Line. Propagation delay is independent of line width.

Due to the complexity of the MAX1150/MAX1151 EV kit design, both techniques were used to make routing easier. The line width is 10mil and has a 50Ω characteristic impedance. It is an eight-layer board stacked in the following manner:

Layer 1 = First controlled-impedance signal layer (Microstrip)

Layer 2 = Ground layer*

Layer 3 = Second controlled-impedance signal layer (Strip Line)

Layer 4 = Ground layer*

Layer 5 = Third controlled-impedance signal layer (Strip Line)

Layer 6 = Ground layer*

Layer 7 = Power layer—all supplies share this layer

Layer 8 = Fourth controlled-impedance signal layer (Microstrip)

**AGND and DGND share the same layer.*

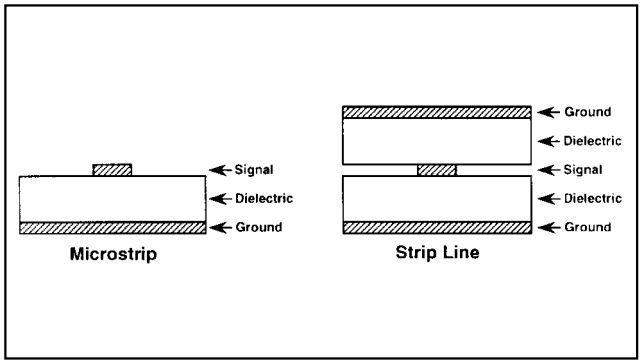


Figure 6. Cross Sections of Microstrip and Strip Line PCB Board Technologies

To minimize logic skew, the line lengths in each stage are closely matched to within 0.1", especially between the ADC output through the second decimation circuit (U18 and U19).

The following lists some of the key guidelines used in the design of the MAX1150/MAX1151 EV kit.

- Minimize the logic fan-out. Most of them have a fan-out of only one.
- If possible, avoid any through-hole vias between the sending and receiving ends of any high-speed lines. Avoid a logic pinout pattern that requires criss-crossing of high-speed lines.
- On all high-speed lines, the loading resistor should be as close to the receiving end as possible.
- All unterminated (open) lines must be less than one-fourth of the signal's rise time divided by the transmission-line propagation delay to assure minimal reflection:

  Open-line length (inches) < 1/4 x (t_{RISE} / t_{PD})

  where: t_{RISE} = rise time of the signal (ns)

  t_{PD} = 0.188ns/in (Strip Line characteristic)

  Table 7 shows typical rise times versus major high-speed logic families with a fan-out of one.
- Use a series damping resistor when an open line exceeds the 1/4 x (t_{RISE} / t_{PD}) maximum.
- Keep analog circuitry separate from digital circuitry, including isolation of grounds. AGND and DGND must be tied together through an inductor or ferrite bead as closely to the ADC as possible.
- Ensure adequate supply decoupling.
- Surface-mount resistors and capacitors work better for high-speed designs.

Table 7. Typical Rise Times vs. Major High-Speed Logic Families

	ECL 10k	ECL 10kH	SYNERGY 100E	SYNERGY 100S	SPECL SONY
t_{RISE} (ns)	2–3.5	1.1	0.3 – 0.4	0.7	0.3–0.4

Characterization

This section has recommendations for how best to characterize the MAX1150/MAX1151 using the MAX1150/MAX1151 EV kit.

Recommended Test Setup

Figure 7 is a simple block diagram of the recommended test setup.

Generator Selection

At higher analog input frequencies, selecting the signal sources becomes critical in order to minimize system-induced measurement error. Jitter and purity are two factors to consider in generator selection.

Generator Jitter Requirements

One of the key parameters in signal-source selection is phase jitter (aperture uncertainty). Jitter is caused by instability in the signal's time base. This appears as an erroneous voltage error at the sampled point. The source jitter must be kept below an allowable level so that accurate characterization of the conversion device can be conducted. The induced voltage error due to jitter is directly proportional to the analog input slew rate (Sr) at midscale. The highest slew rate is at midscale.

$Sr = \Delta V / \Delta t = 2\pi f$ (Slew rate for a sine wave)

$Tj = \Delta t = \Delta V / 2\pi f$ (Time jitter or aperture jitter)

For example, if a 2Vp-p analog input sine wave is used as the source, and if 0.2LSB of error caused by the signal source is acceptable, then the aperture jitter calculates as follows:

$Tj = \Delta V / 2\pi f$

allowable $\Delta V = (2 \times 0.2) / 256 = 1.563mV$

For f_{IN} = 250MHz, the allowable source jitter is Tj = 0.995ps

The Hewlett-Packard HP8644A frequency generator is specified to have 0.7ps RMS of phase jitter.

Source Purity

Another parameter that needs attention is the purity of the signal source used for the analog input. A suitable bandpass filter (BPF) might be needed between the signal source and the EV kit input (VIN).

Alternately, a notch filter can be inserted to suppress the harmonics close to the signal source. A simple notch filter can be constructed from a coaxial cable or twisted-wire stub cut to a quarter wavelength (Figure 8). The signal's speed depends on the conductor material used in the stub. Table 8 shows signal-propagation rates for several conductor types.

The wavelength $\lambda = v / f$, where f = frequency of interest. Use a network analyzer, or simply check the frequency of interest with an oscilloscope to cut the stub precisely to $\lambda/4$.

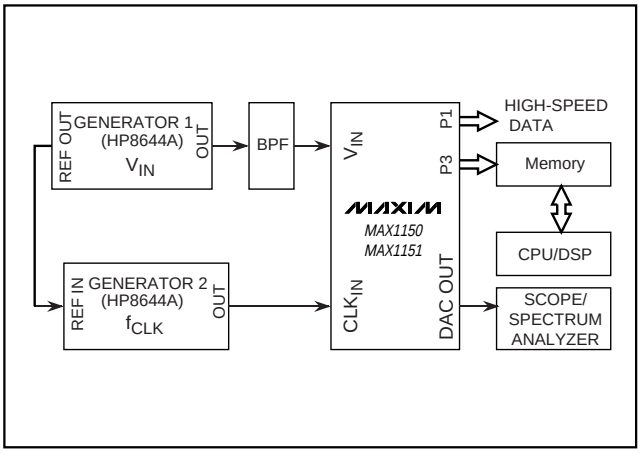


Figure 7. AC Test Setup Block Diagram

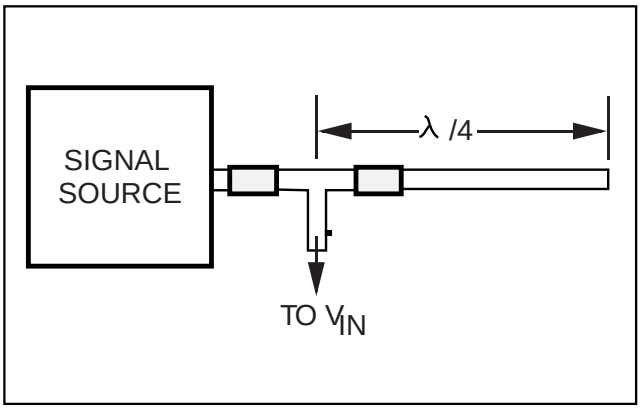


Figure 8. Stub Interconnection

Characterization at Speed

Connector P1 is provided to enable the user to extract data from the evaluation board (EV board) at full speed. P1 is a high-speed, high-density, 50Ω controlled-impedance connector. The digital output data, the overrange bit, and the data-ready signal for banks A and B are brought out through this port. Refer to the *Digital Output Buffer and High-Speed Connector* section for more details.

Characterization Using Decimated Data Output

The MAX1151 is sampled at 750Msps with an output data rate of half the clock rate (375MHz). Given this very high data rate, there is no simple tool to analyze the data without tedious development of a breadboard involving demultiplexers, high-speed memory fan-out, etc.

The MAX1150/MAX1151 EV kit provides the user with decimated data output (by factors of 32/64/128 with respect to the input clock) at the P3 connector and the DAC output.

Method 1: Characterization Through DAC OUT

With the setup in Table 9, the DAC output signal is a sine wave at f_B and consists of 4096 points/period ($1/f_B$). The DAC reconstruction signal ensures proper EV board setup, and can be used directly for characterization. The device's performance can be viewed from the DAC OUT signal with a spectrum analyzer.

The analog input offset and gain can be adjusted by monitoring DAC OUT with an oscilloscope.

The DAC OUT signal can be used to adjust the delay of the clock to the first-stage decimation, to meet setup and hold times. Refer to the *Decimation Circuit* section and adjust the clock delay through S0–S4 until no glitches or spikes appear in the DAC OUT signal.

Method 2: Noise Characterization Through DAC OUT

This noise is inherent in the ADC as DC noise or a noise floor. It could be identified simply by entering a DC input and measuring the number of code counts. The simplest and most accurate way to measure this noise is to input a slow ramp and measure the code-transition noise, through DAC OUT. The ramp input's slope suggests at least 10 capture data per LSB, or slope ≤ (LSB x f_C) / 10.

With certain types of ADCs, this transition-code noise changes with the input frequency. The beat-frequency technique offers a tool for characterizing code-transition noise at higher input frequencies. Table 9 is the setup for S = 4096 points per beat period. The code-transition noise could be viewed through DAC OUT with a scope by reducing S to a much smaller number of points per period (for example, from 32 to 64).

Method 3: Characterization Through Connector P3

From Table 9, 4096 points FFT can be performed from the data output at P3 (37-pin D-shell connector). Refer to Figure 9c for the pin assignment. Note that the reconstruction DAC OUT signal should be used before an FFT is taken to verify proper EV board setup (decimation setup and delay switches) and analog input signal (offset and gain).

Beat-Frequency Technique

The beat-frequency technique is highly recommended when characterizing the MAX1150/MAX1151 using the decimated data output from connector P3 or DAC output BNC. Three parameters must be properly selected for the beat-frequency technique to work:

f_S = Sampling frequency or CLK IN

f_{IN} = Analog input frequency

N = 32/64/128, decimation factor (Table 6)

The input frequency is calculated as follows:

$$f_{IN} = nf_C \pm f_B$$

where: $f_C = f_S/N$ Capture frequency (Decimated frequency at P3)

n = integer

$f_B = f_C / S$ Beat frequency

S = number of sample points

Example:

Capturing a 4096-point FFT at connector P3 with the following constraints is desired:

f_S = 750MHz

f_{IN} = 50MHz and 100MHz

Maximum update rate of the memory = 20MHz

Solution:

a. For N = 64

$$f_C = f_S / N = \frac{750 \times 10^6}{64} = 11.71875MHz < 20MHz$$

b. The beat frequency:
$f_B = f_C / 4096 = 2861.022949Hz$

c. Round off f_B to eliminate round-off errors:
$f_B = 2860$
Then work backward:
$f_C = f_B \times 4096 = 11.71456MHz$
$f_S = f_C \times 64 = 749.73184MHz$

d. For n = 4, $f_{IN} = 4 \times f_C + f_B = 46.861101MHz$
For n = 9, $f_{IN} = 9 \times f_C - f_B = 105.4339MHz$

e. Conclusions:
$f_S = 749.73184MHz$
$f_{IN} = 46.861101MHz$
and = 105.4339MHz
N = 64

For convenience, Table 9 shows example setup parameters for 4096 point beat-frequency tests.

Table 8. Signal-Propagation Rates by Conductor Type

CONDUCTOR	SPEED (V)
Any conductor in air	30cm/ns
Microstrip line (epoxy)	15cm/ns
Coaxial cable (Teflon)	20cm/ns

Table 9. 4096 Point Beat-Frequency Test Setup

f_S (MHz)	f_{IN} (MHz)	N (DECIMATION)	f_C (MHz)	f_B (Hz)	n
499.908608	46.868339	64	7.811072	1907	6
499.908608	101.542029	64	7.811072	1907	13
499.908608	148.412274	64	7.811072	1907	19
499.908608	203.085965	64	7.811072	1907	29
499.908608	249.956211	64	7.811072	1907	32
750.256128	52.750953	128	5.861376	1431	9
750.256128	99.644823	128	5.861376	1431	17
750.256128	152.394345	128	5.861376	1431	26
750.256128	199.288215	128	5.861376	1431	34
750.256128	252.037737	128	5.861376	1431	43
999.817216	46.868339	128	7.811072	1907	6
999.817216	101.542029	128	7.811072	1907	13
999.817216	148.412274	128	7.811072	1907	19
999.817216	203.085965	128	7.811072	1907	29
999.817216	249.956211	128	7.811072	1907	32

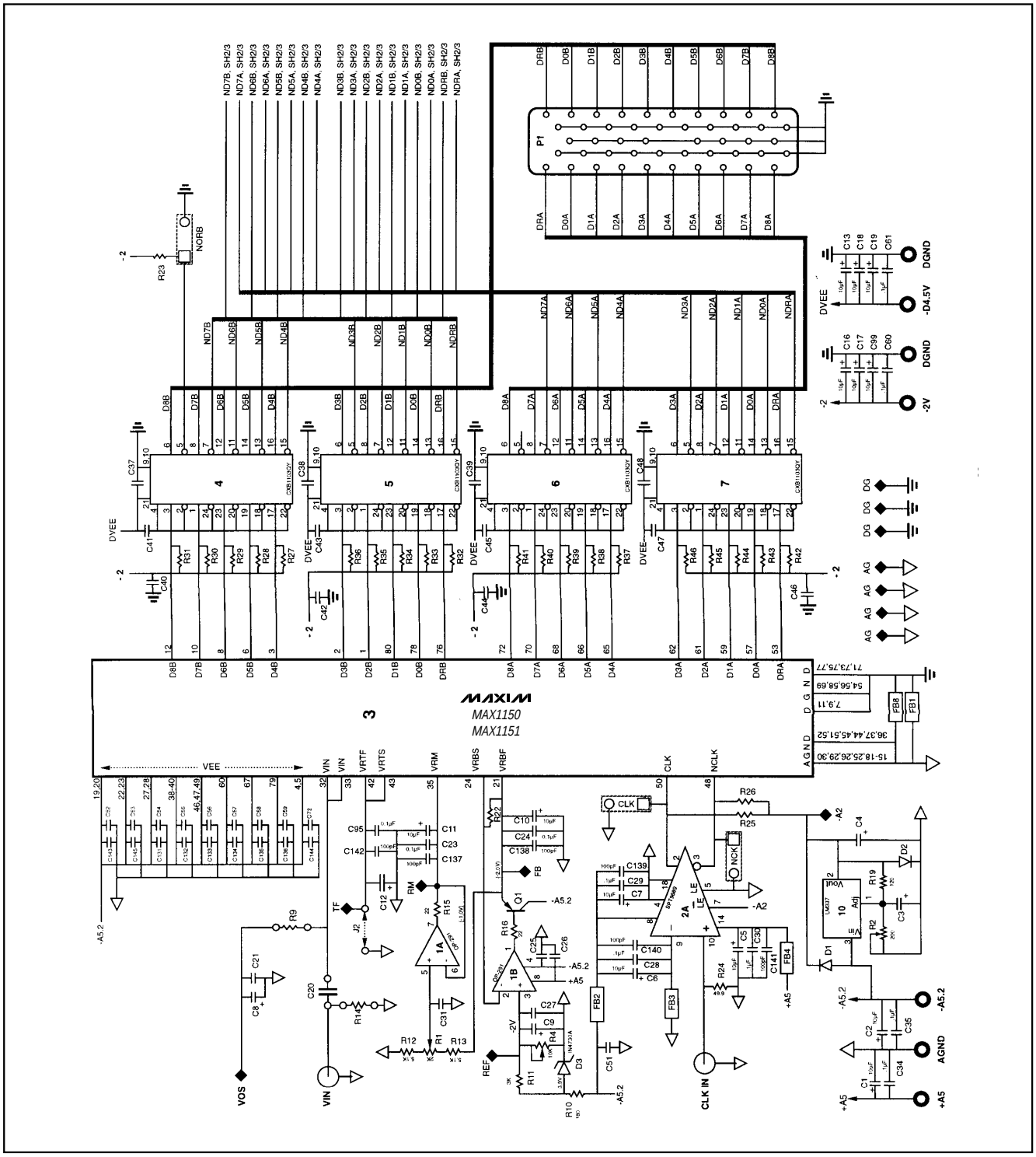


Figure 9a. MAX1150/MAX1151 EV Kit Schematic

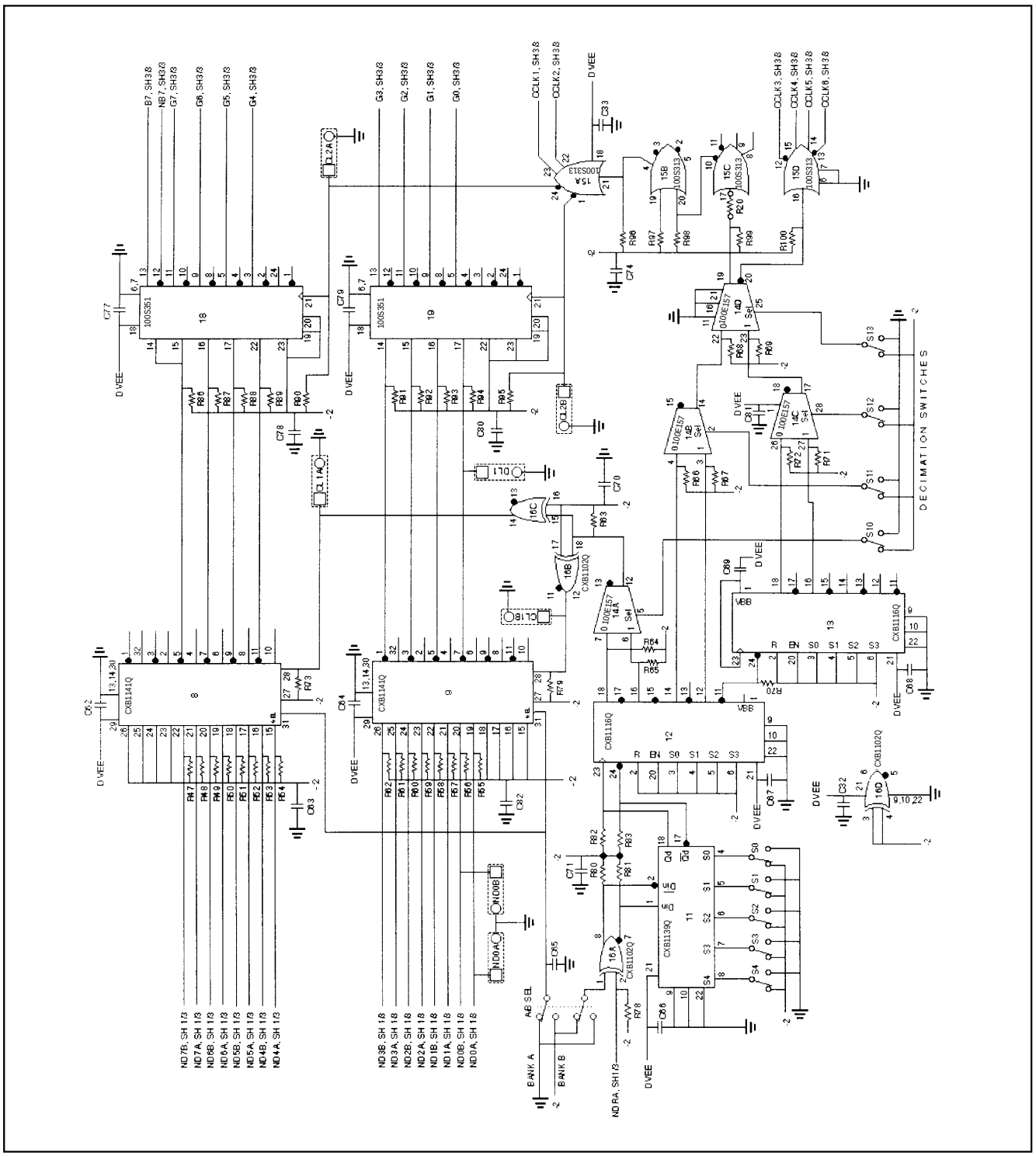


Figure 9b. MAX1150/MAX1151 EV Kit Schematic (continued)

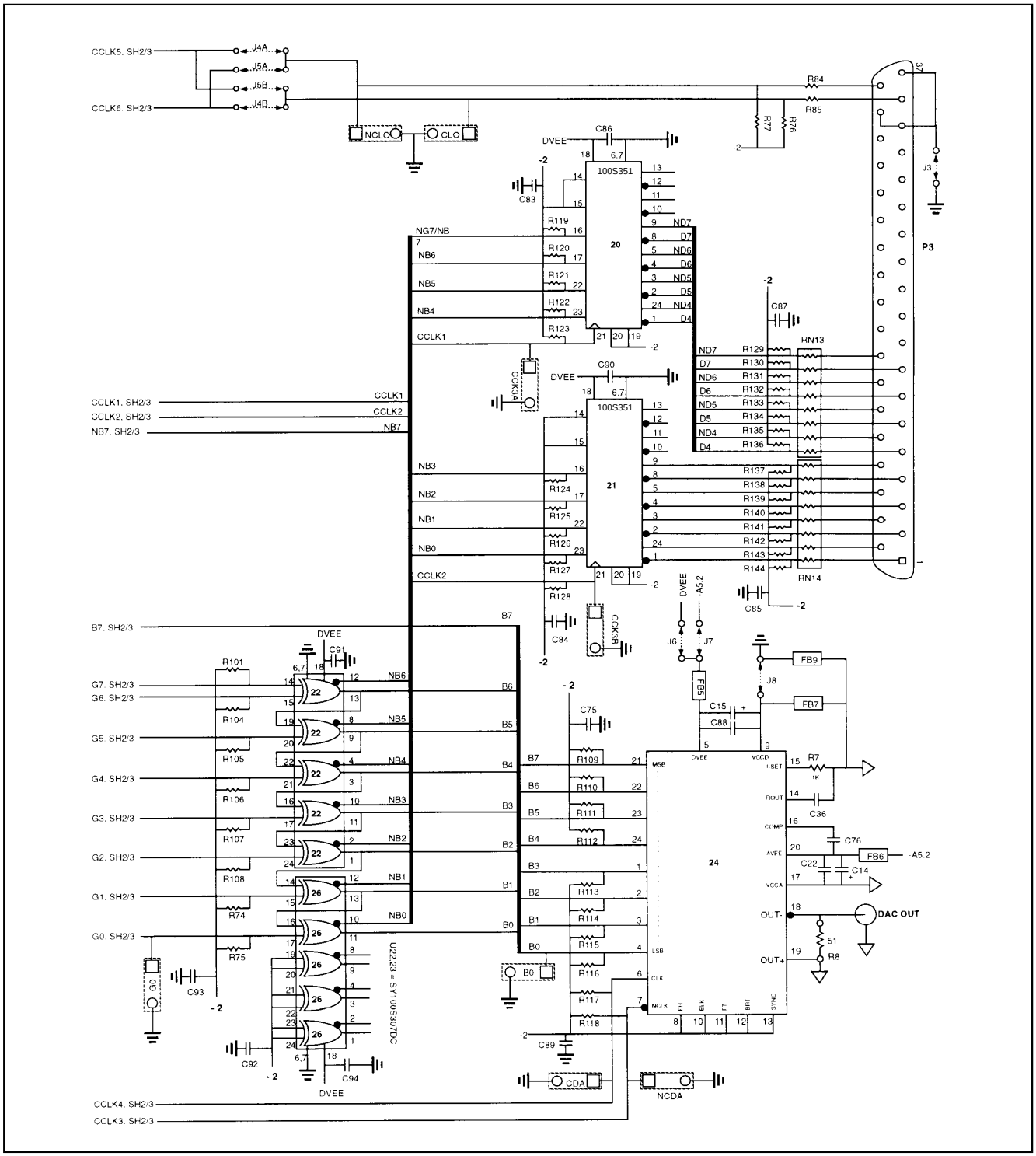


Figure 9c. MAX1150/MAX1151 EV Kit Schematic (continued)

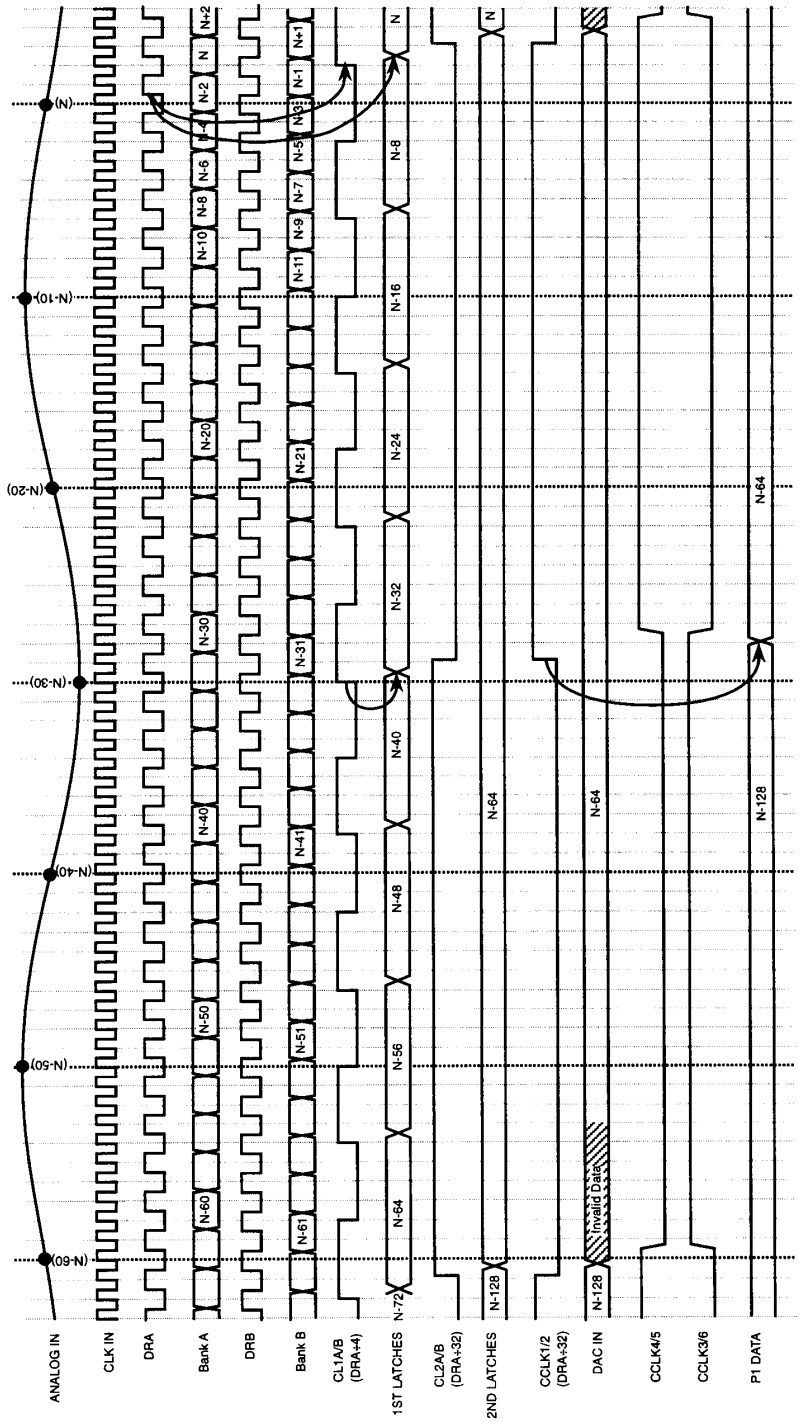
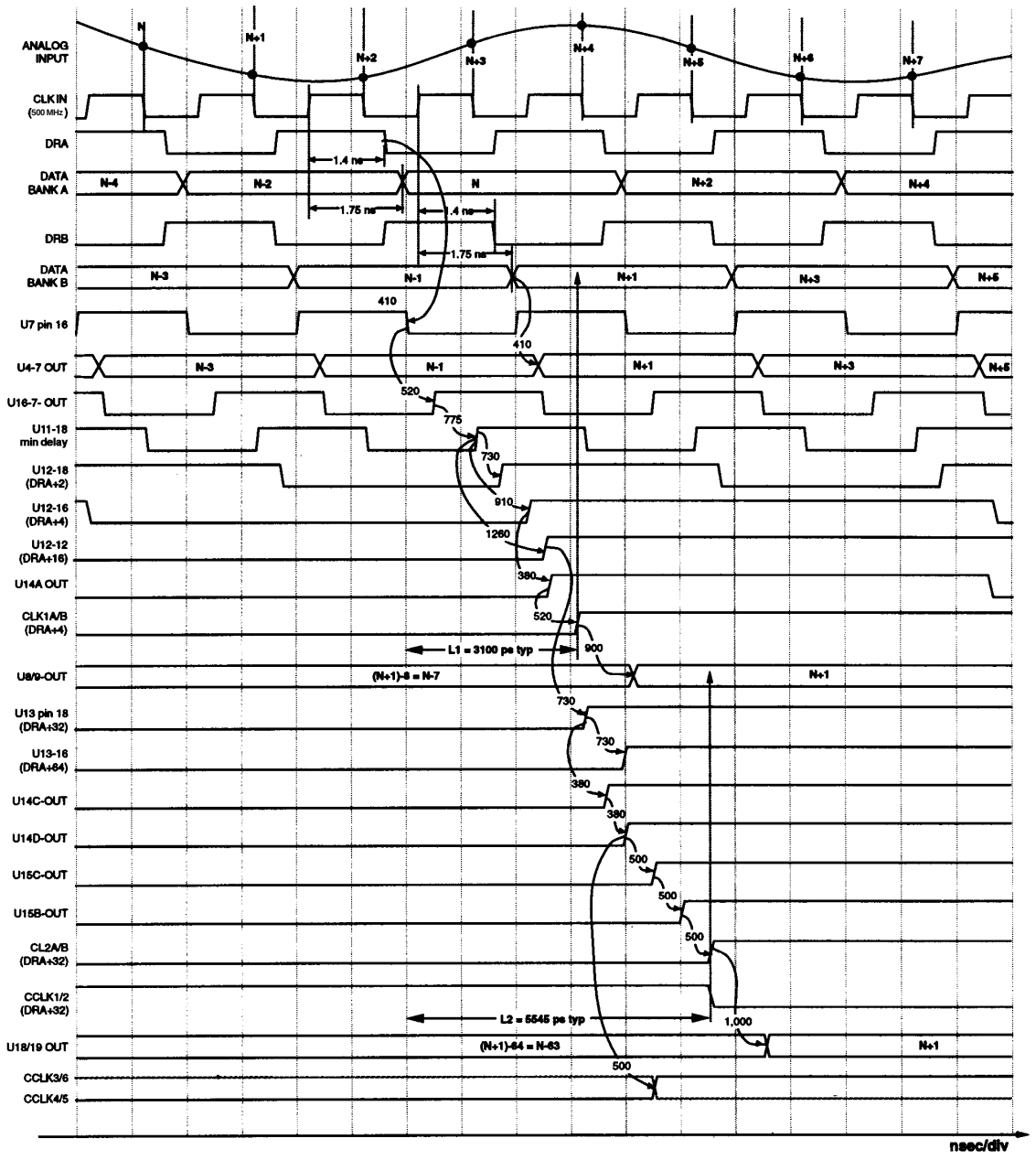


Figure 10. MAX1150/MAX1151 EV Kit Timing Diagram



Notes: 1. A/B Sel switch = 1 for Bank B selection (Figure 9a).
2. S10 switch = 1 for a divided-by-4 latch (from the data-ready signal) on the first decimation stage.
3. S12 = 0; S13 = 1 (S11 = don't care) for a divided-by-32 latch (from the data-ready signal) on the second decimation stage.
4. Unless otherwise specified, all units are in picoseconds.
5. All logic-propagation delays are typical.
6. L1 timing (CLK1A/B) could be adjusted by programming U11 delay through S0–S4 switches (Table 4).

Figure 11. MAX1150/MAX1151 EV Kit Timing Diagram

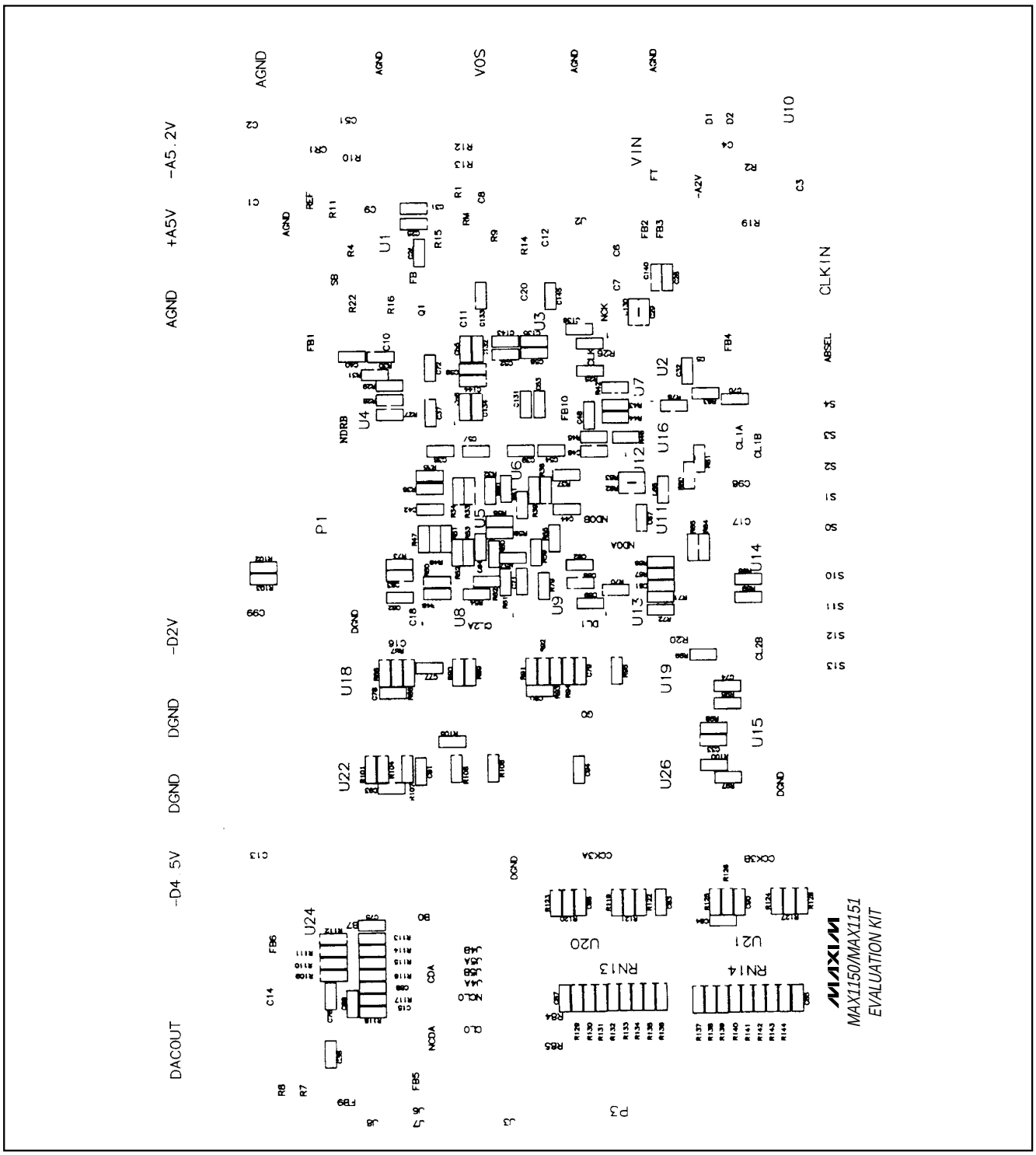


Figure 12. MAX1150/MAX1151 EV Kit Component Placement Guide—Component Side

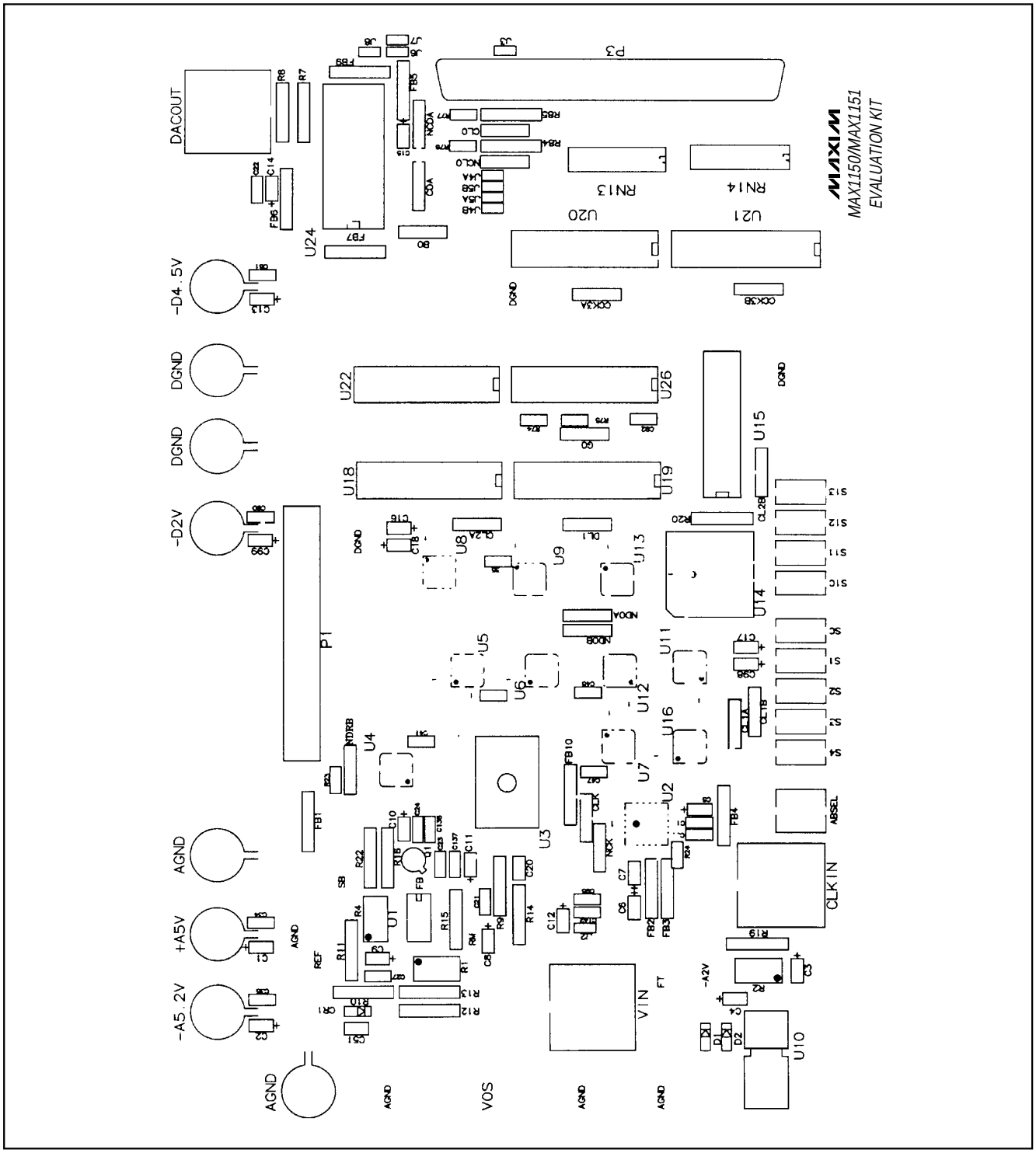


Figure 13. MAX1150/MAX1151 EV Kit Component Placement Guide—Solder Side

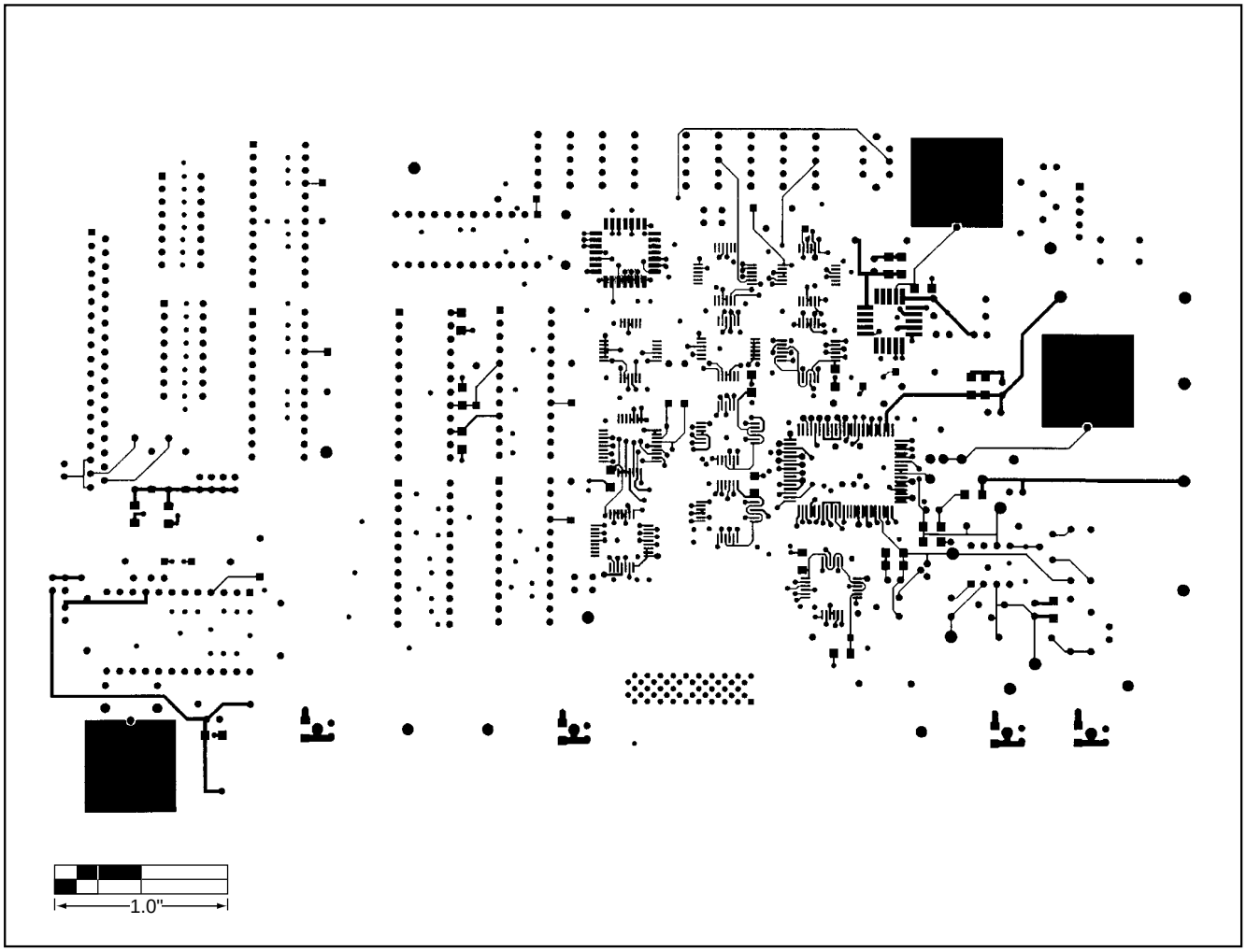


Figure 14. MAX1150/MAX1151 EV Kit PC Board Layout—Component Side (signal 1, layer 1)

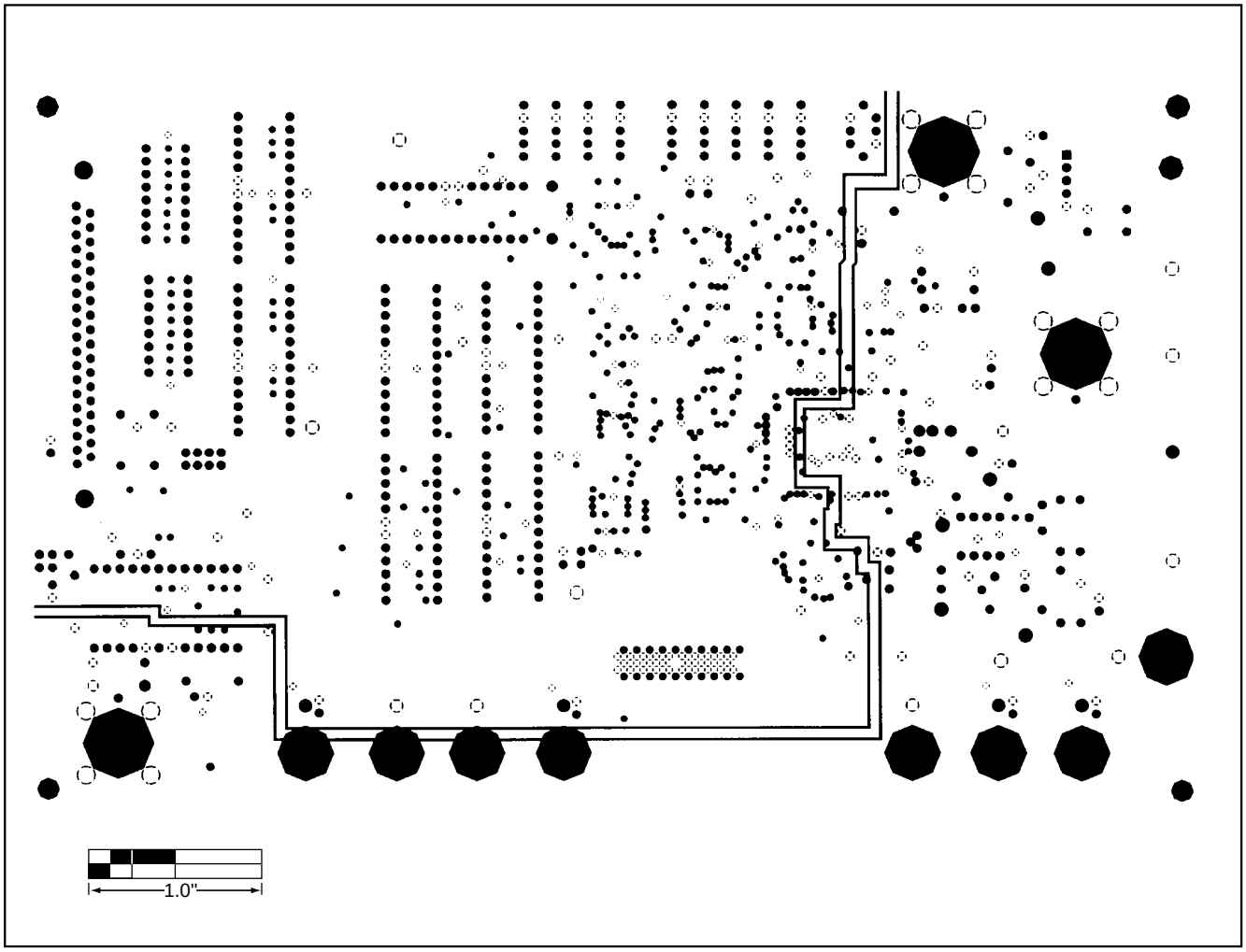


Figure 15. MAX1150/MAX1151 EV Kit PC Board Layout—Ground Plane (layers 2, 4, and 6)

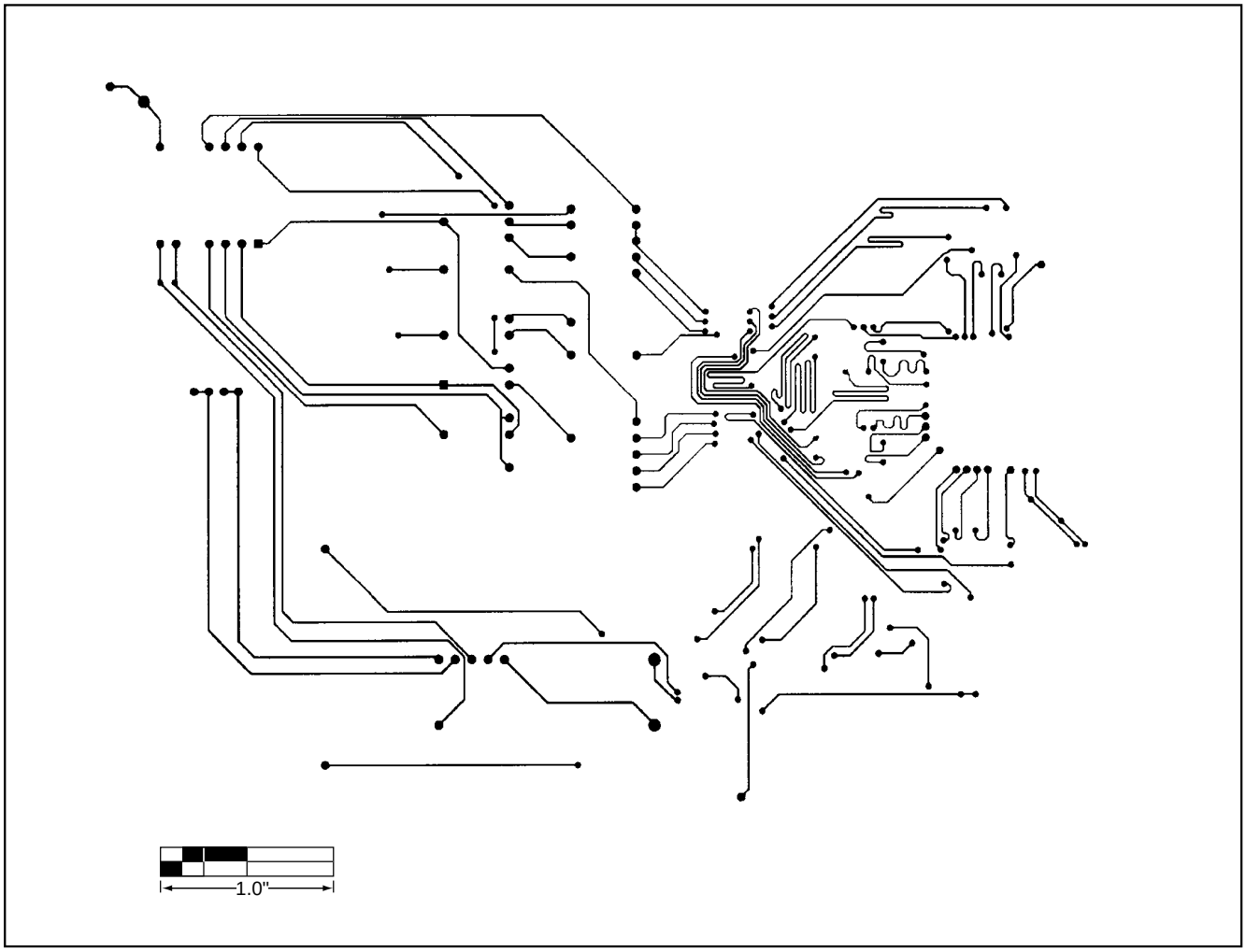


Figure 16. MAX1150/MAX1151 EV Kit PC Board Layout (signal 2, layer 3)

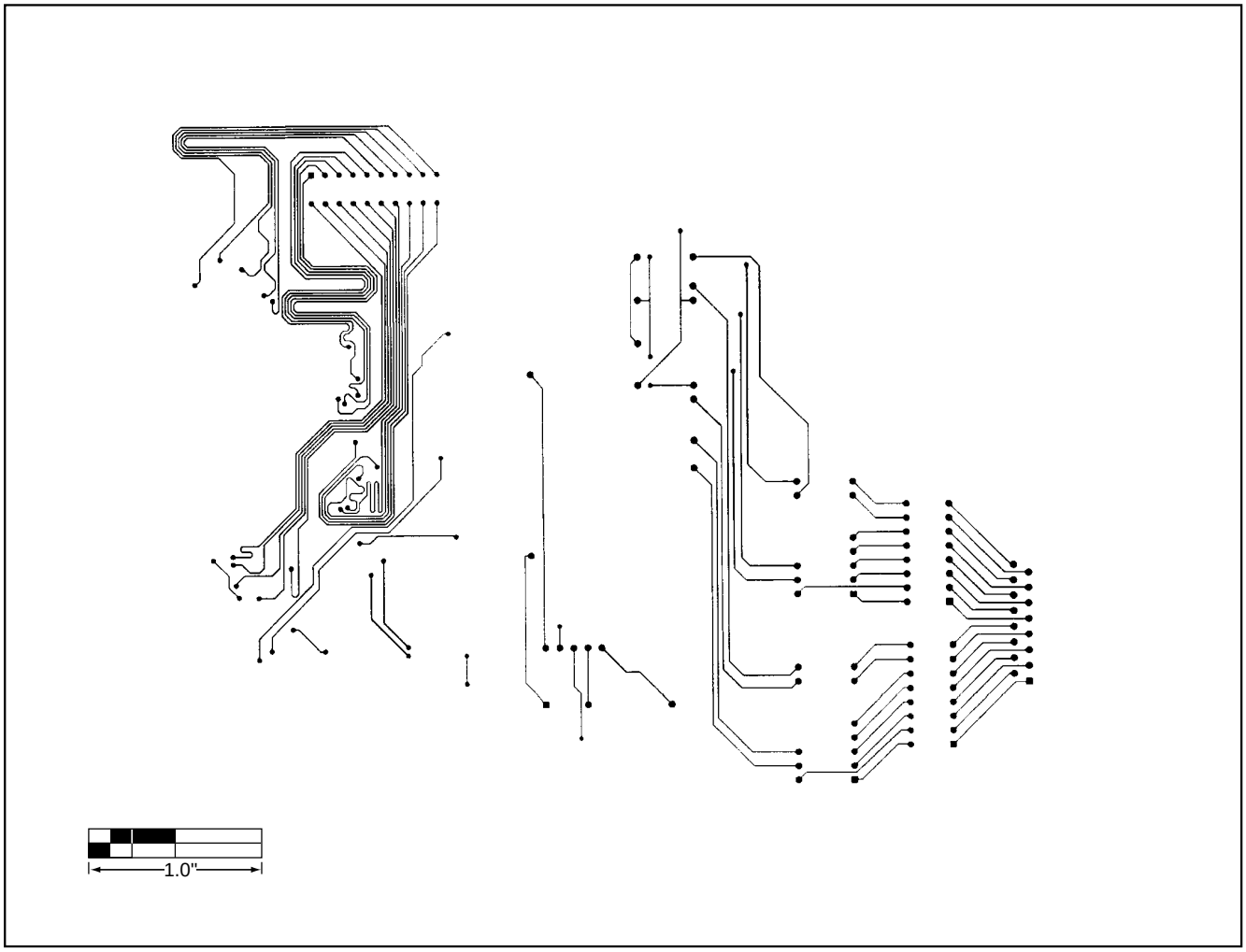


Figure 17. MAX1150/MAX1151 EV Kit PC Board Layout (signal 3, layer 5)

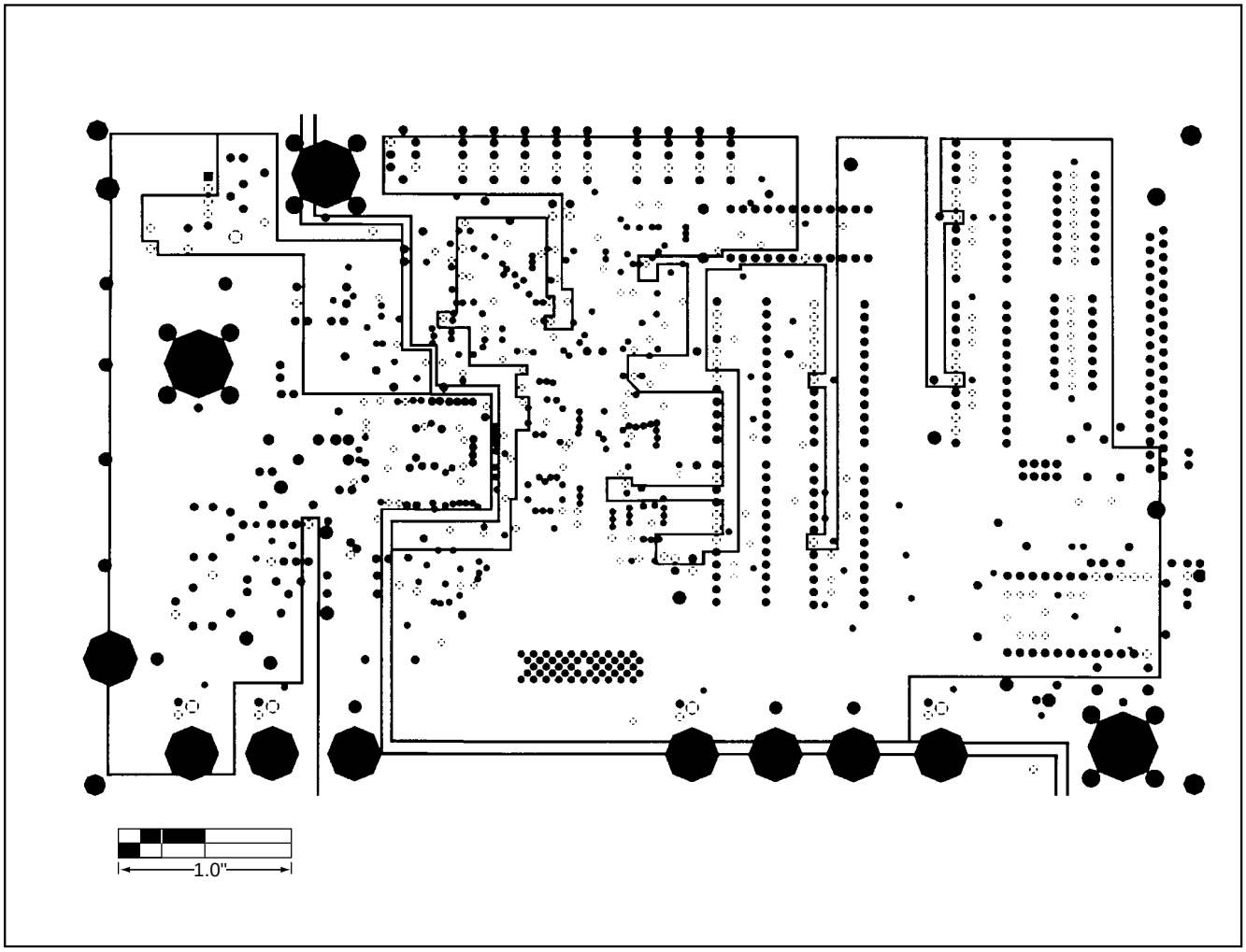


Figure 18. MAX1150/MAX1151 EV Kit PC Board Layout—Power Plane (layer 7)

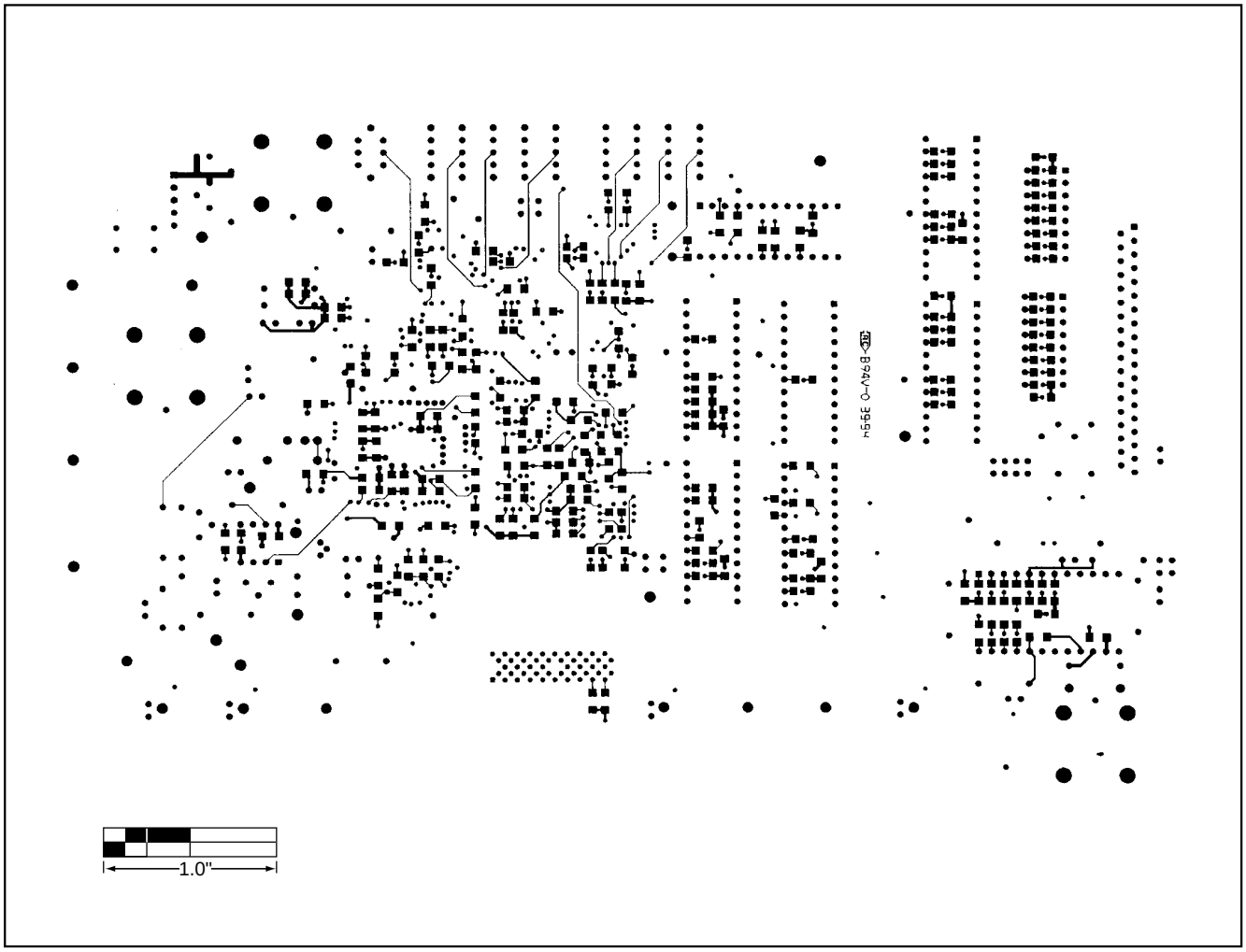


Figure 19. MAX1150/MAX1151 EV Kit PC Board Layout—Solder Side (signal 4, layer 8)