19-1152; Rev 0; 10/96

MAX1114/MAX1125 Evaluation Kit

Evaluates: MAX1114/MAX1125

General Description

The MAX1114/MAX1125 Evaluation Kit (EV kit) is a tool for the evaluation and characterization of the MAX1114 (150MHz) or MAX1125 (300MHz) analog-to-digital converters (ADCs).

The evaluation board's dimensions are 7.562" x 8.125". It consists of several electrical sections, each of which is explained in the *Detailed Description:*

- Power connections
- Reference circuit
- Analog input circuit
- MAX1114/MAX1125 ADC
- Clock driver/divider circuit
- Digital output latches

Features

- **150MHz/300MHz Conversion Rate**
- **On-Board Reference Circuit**
- **AC-Coupled Input**
- **Clock-Input/Divider Circuit**
- **On-Board Reconstruction DAC**

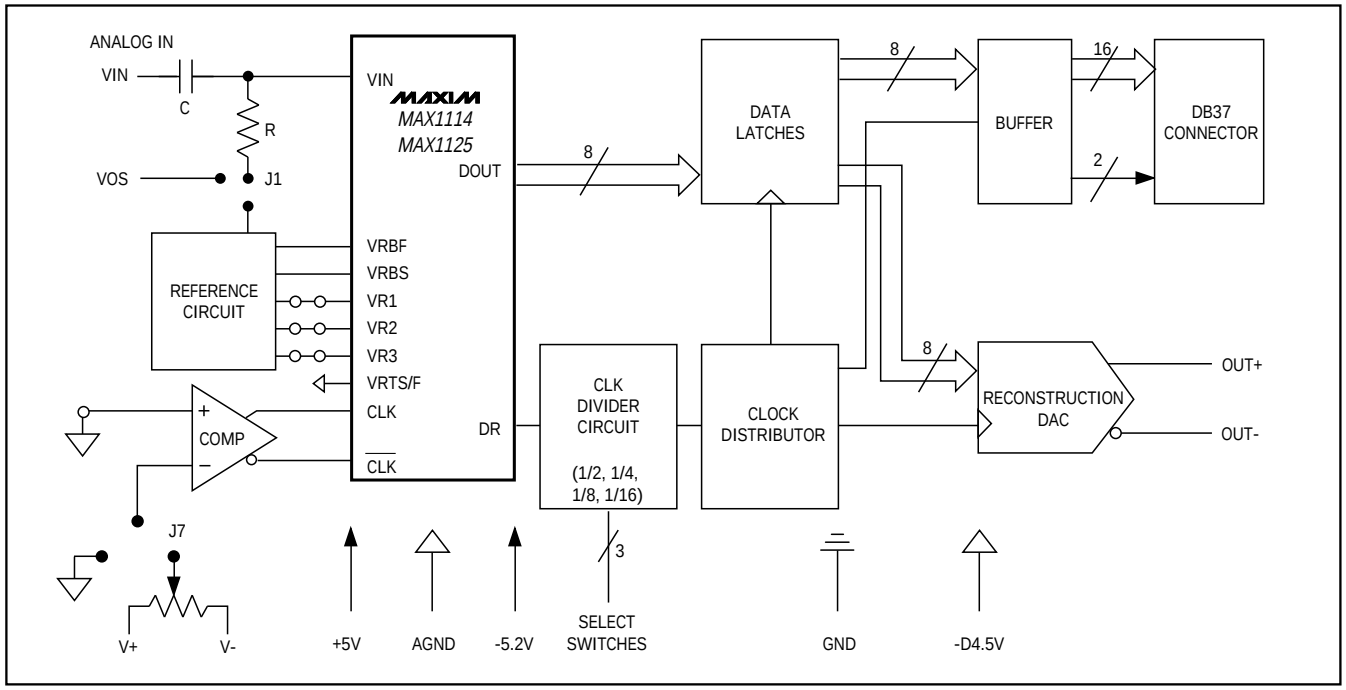
Ordering Information

PART	TEMP. RANGE	BOARD TYPE
MAX1114 EVKIT	0°C to +70°C	PGA (with MAX1114)
MAX1125 EVKIT	0°C to +70°C	PGA (with MAX1125)

Applications

Digital Oscilloscopes
Transient Capture
Radar, EW, ECM
Direct RF Down-Conversion
Medical Electronics

Block Diagram



Component List

DESIGNATION	QTY	DESCRIPTION
C1, C2, C3	3	10µF, 25V, 20% tantalum capacitors
C4–C22, C100, C101	21	4.7µF, 16V, 20% tantalum capacitors
C28	1	0.01µF ceramic capacitors
C29, C30–C51, C53–59, C61, C63–C72, C87, C88, C89, C903, C904	46	0.1µF ceramic capacitors
C80–C86, C800, C801	9	100pF ceramic capacitors
D1	1	3.9V zener diode 1N5228
D2–D5	4	Diodes 1N4001
FB1–FB9	9	Ferrite beads
P1	1	DB37 connector
Q1, Q2	2	Transistors 2N2907
R1, R3, R4	3	51Ω, 1/8W, 5%, carbon-film resistors
R2	1	22Ω, 1/8W, 5%, carbon-film resistor
R5–R9	5	200Ω potentiometers
R10–R13	4	1kΩ potentiometers
R14, R15	2	120Ω chip resistors
R16, R17, R18	3	2kΩ chip resistors
R19–R24	6	1kΩ chip resistors
R25–R29	5	22Ω chip resistors
R30	1	200Ω chip resistor
R31	1	5.1kΩ chip resistor
R32	1	390Ω chip resistor
R38–R46, R48–R62, R65–R73	33	49.9Ω chip resistors
RN1, RN2	2	16 DIP, 47Ω resistor networks
RN3–RN7	5	6 SIP, 51Ω resistor networks
RN8	1	8 SIP, 51Ω resistor network
RN9	1	10 SIP, 51Ω resistor network
SW1, SW2, SW3	3	Single-pole, double-throw switches
U1	1	DUT, MAX1114 or MAX1125 46L PGA
U2	1	Op amp
U3	1	Op amp (quad)
U4	1	Comparator
U5, U13	2	Regulators
U6, U7	2	Hex flip-flops
U8	1	Counter
U9	1	Multiplexer
U10	1	Digital-to-analog converter
U11, U12, U13, U14	4	XOR Gates
N/A	5	Banana jacks
N/A	4	BNC connectors
N/A	8	Pin sockets
N/A	4	Spacers
N/A	13	Test points

Detailed Description

Analog Inputs

The analog signal is input via the V_{IN} BNC connector. It is AC coupled and level shifted by a -1V offset. The AC coupling is provided by C28 (0.01µF) in parallel with C29 (0.1µF). The AC-coupled signal is level shifted though the 49.9Ω resistor R2 (Figure 6).

The -1V offset voltage can be internally supplied by putting a jumper at J1, or it can be externally supplied through test point V_{OS} by leaving jumper J1 open.

The on-board offset is generated by D1, which is a 3.9V zener diode. R11 is a voltage-divider adjustment potentiometer that feeds the adjusted -1V reference into buffer U2 and drives the Q1 emitter follower to provide the final offset voltage.

Note that the MAX1114/MAX1125 EV board provides no voltage input protection for the analog input. Take care to ensure that the input voltage does not exceed the device's absolute maximum input rating, which is from (V_{EE} - 0.7V) to (GND + 0.7V).

Reference Circuits

The reference ladder top input pins, VRTF (force) and VRTS (sense), should be 0.0V. VRTF and VRTS are tied directly to ground through jumpers J5 and J6, respectively. To drive these pins with active force and sense, build this circuitry in the prototype area provided on the board. With J5 and J6 removed, inject the force and sense directly into test points VRTF and VRTS. See the MAX1114 or MAX1125 data sheet for the recommended force and sense circuit.

Table 1. Ladder Adjust Points

TEST POINT	ADJUST	SET POINT ±5mV
VRBF	R10	-2.0V
VR1	R7	-1.5V
VR2	R8	-1.0V
VR3	R9	-0.5V

Table 2. Power-Supply Requirements

POWER SUPPLY	MIN	TYP	MAX	TYP CURRENT REQUIREMENT
-5.2V Analog	-5.1	-5.2	-5.3	500mA
+5.0V Analog	+4.9	+5.0	+5.1	20mA
-4.5V Digital	-5.1	-5.2	-5.3	1A

The same diode described above, D1 (3.9V zener diode), is used in conjunction with voltage divider R10 (1kΩ potentiometer) to generate the on-board reference for the bottom of the reference ladder. R10 adjusts the reference level, and the voltage is buffered through U3A and fed into the bottom of the ladder force and sense through the Q2 emitter follower. R31 (5.1kΩ) closes the loop to prevent U3A's output from going to the rail when the analog-to-digital converter (ADC) is removed.

Driving Additional Ladder Taps

The MAX1114/MAX1125 CERQUAD package version provides additional pins for driving the 1/4-, 1/2-, and 3/4-scale ladder taps. Only a 1/2-scale ladder-tap pin is provided for the MAX1114/MAX1125 ceramic SB package version. The reference ladder taps can be used to improve the linearity of the converter and tracking over temperature.

The MAX1114/MAX1125 EV kit uses a PGA version of the part that provides all three taps. The voltage reference source for all three taps is derived from a voltage divider connected between VRBF and VRTF with four resistors: R20, R21, R22, and R23; and three potentiometers: R7, R8, and R9. Avoid using potentiometers in an actual application design, because they have a very poor temperature coefficient (TC). The resistors used in a design should be ratio matched to 0.1% or better (i.e., 1/4LSB), and track each other over temperature.

R7 is the adjustment potentiometer for the 3/4-scale tap (typically -1.5V); R8 is for the 1/2-scale tap (typically -1.0V); and R9 is for the 1/4-scale tap (typically -0.5V). These voltages are buffered through U3B, U3C, and U3D, respectively. Jumpers J2, J3, and J4 are the jumper options for VR1, VR2, and VR3, respectively. The jumpers should be configured according to the desired setup.

It is critical that the reference voltage not exceed the absolute maximum rating. U3 is a rail-to-rail op amp, and is supplied from ground to -5.2V. It is very important that this op amp's output not go above 0.0V. Reference circuit U3A is self-protected to prevent going above ground or below $-V_{EE}$.

It is highly recommended that each reference pin be decoupled with three capacitors in parallel. A 100pF chip capacitor should be closest to the converter, followed by a 0.01µF chip capacitor, and then a 2µF to 10µF tantalum capacitor.

Converter Power Supply

The MAX1114/MAX1125 require a single -5.2V (V_{EE}) power supply, which is supplied through a total of six pins in the PGA package. Due to the distribution of supply pins on the PGA package, the supply decoupling on the MAX1114/MAX1125 EV kit board is divided into four pin groups (Figure 6). The four groups comprise a single H1 pin, a single G8 pin, pins C1 and E2, and pins C9 and E9.

Each group is decoupled with three capacitors in parallel. A 100pF chip capacitor should be closest to the converter, followed by a 0.01µF chip capacitor, and then a 2µF to 10µF tantalum capacitor.

Board Layout

The MAX1114/MAX1125 EV kit is built on a six-layer PC board with 10mil signal lines. These lines are 50Ω controlled impedance. Layer assignments are as follows:

Layer 1: Signal lines (controlled impedance)
Layer 2: Ground layer
Layer 3: Ground layer
Layer 4: Power layer
Layer 5: Ground layer
Layer 6: Signal lines (controlled impedance)

Analog and digital ground share the same ground layer. All supplies share the same power layer.

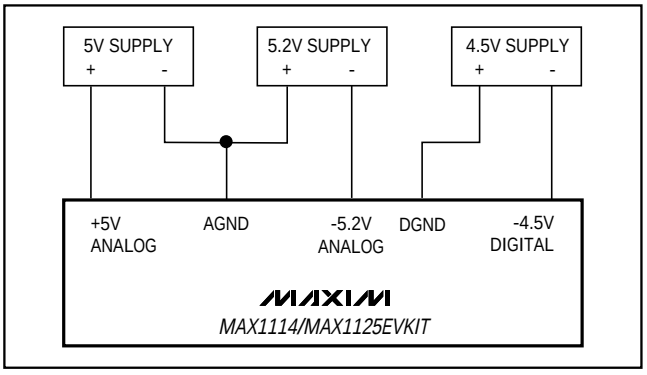


Figure 1. Power-Supply Hookup

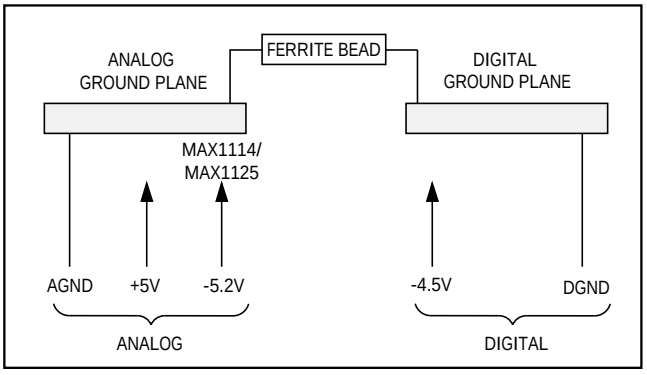


Figure 2. Power and Ground Distribution

Table 3. Data Ready Output Decimation Table

S2	S1	S0	DECIMATED OUTPUT
0	0	0	÷1
0	0	1	÷2
0	1	0	÷4
0	1	1	÷8
1	0	0	÷16
1	0	1	Logic Zero or No Clock
1	1	0	
1	1	1	

Clock-Driver Circuit

The MAX1114/MAX1125 EV kit uses a high-speed voltage comparator (U4A) in the clock-driver circuit, allowing the user to drive the evaluation board directly from a symmetrical sinewave input signal (U4B is not used).

Comparator U4A converts the signal into a differential ECL output signal compatible with the MAX1114/MAX1125. Driving the MAX1114/MAX1125 with a differential clock is highly recommended because it minimizes aperture jitter in the converter.

Note that the circuit associated with U4A is supplied from all analog supplies: -5.2V (analog), +5.0V (analog), and -2V pull-down voltage (analog). U4 must be supplied from analog supplies to eliminate the possibility of ground loops that may degrade the performance of the converter. The -2V (-A2) pull-down voltage is generated from an adjustable voltage regulator (U5).

In normal operation, jumper J7A must be installed and J7B must be open. This achieves a 50% duty cycle for the clock input into the converter, assuming the input clock signal (CLK IN) is a sinewave symmetrical about 0.0V. The clock input should not exceed ±2V. (Input compliance for U4 is ±2.5V.)

In some applications, there may be a need for a clock duty cycle other than 50%. To test the converter performance under these conditions, open jumper J7A and short J7B. Adjust potentiometer R12 for the desired duty cycle. A clock-monitoring test point is provided. The test point looks similar to the way it is pictured in the schematic. (It provides a short ground-path connection.)

Maxim recommends using a Motorola Eclipse Lite MC10EL16 driver in designing your clock-driver circuit. Figure 3 shows the MC10EL16 in a differential ECL input clock-driver configuration, and Figure 4 shows how it is used when driving from a single-ended ECL clock source.

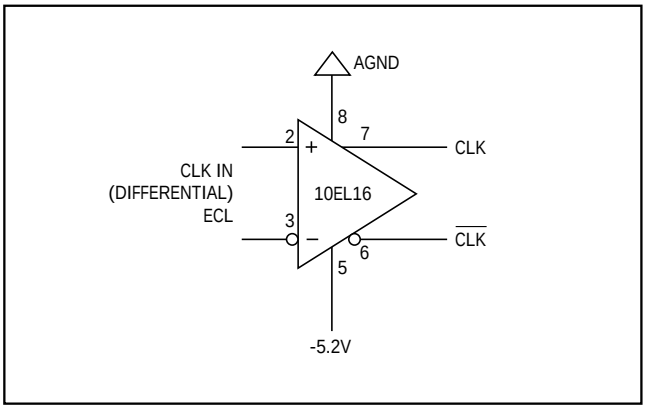


Figure 3. Differential Input Clock

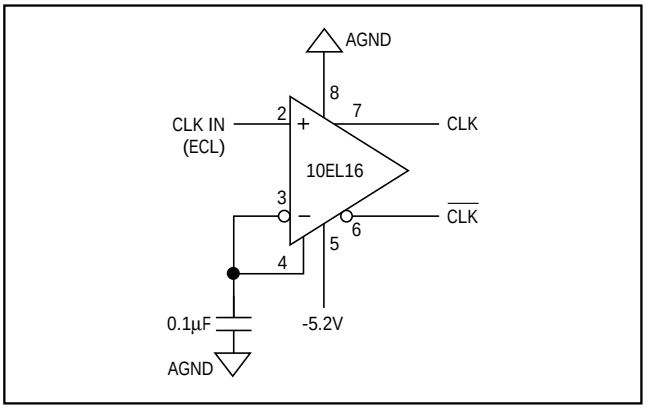


Figure 4. Single Input Clock

Digital Outputs

The MAX1114/MAX1125's digital outputs are immediately followed by U6 and U7 latched hex D flip-flop registers. U14C and U14D are used as gated buffers to latch the registers using the decimated Data Ready signal generated from U8 and U9 (Table 3.) Each of the differential outputs of U6 and U7 is split into two digital output paths.

The first path goes to buffers U11 and U12 to provide a differential output of the data through the P1 connector (D shell). The second path feeds U10, a reconstruction digital-to-analog converter (DAC). Both paths also carry the decimated Data Ready signal generated from U8 and U9 (Table 3).

Data Ready Signal

The MAX1114/MAX1125's Data Ready signal is fed into a four-state counter/shift register (U8). U8 divides down (decimates) the Data Ready by 2, 4, 8, and 16. Connecting jumper J12 to ground inverts the Data Ready before input into the counter.

The desired decimated Data Ready signal is selected by switches S0–S2 (Table 3). These switches select the output from U9 (dual 8-input multiplexer) and feed it to the two output paths described above (i.e., P1 or the reconstruction DAC).

Data Output Logic Control

The MAX1114/MAX1125 EV kit provides options for inverting the MSB, LSB, and Data Ready outputs via output control pins MINV, LINV, and DRINV, respectively. These pins are internally tied low inside the MAX1114/MAX1125. They may be tied high using jumpers J8 (for DRINV), J9L (for LINV), and J9M (for MINV). The MAX1114 or MAX1125 data sheet shows the output coding table as a function of these output control pins.

NOTE: The reconstruction DAC (U10) requires a straight binary digital input format.

Board Power Supplies and Grounding

The MAX1114/MAX1125 EV kit requires three externally supplied power supplies: +5V analog, -5.2V analog, and -4.5V digital.

In addition, a -2V pull-down supply is generated from digital -4.5V using an adjustable voltage regulator (U13). The analog and digital ground planes are kept separate and are tied together through a ferrite bead as close to the ADC as possible (Figure 2).

Reconstruction DAC

U10 is an 8-bit, high-performance reconstruction DAC. U10 is set for a fixed gain when jumper J16 is installed, or can be adjusted by removing J16 and using potentiometer R13.

Both OUT+ and OUT- are current-sinking outputs, and are loaded with 50Ω termination resistors R3 and R4. These termination resistors are socketed and can be removed. The load can be changed as long as the output remains within the -1.2V to +1.5V output compliance voltage range. The digital input format is straight binary.

Jumper Options

Table 4 shows the MAX1114/MAX1125 EV kit jumper defaults.

Table 4. Jumper Defaults*

JUMPER	STATUS	CONFIGURATION
J1	Short	Internal -1V analog input level shift
J2	Open	VR1 reference ladder tap open
J3	Short	Force middle reference ladder tap VR2
J4	Open	VR3 reference ladder tap open
J5	Short	Connect VTRF to AGND
J6	Short	Connect VRTS to AGND
J7A	Short	Set clock reference voltage to AGND
J7B	Open	(J7B must be open when J7A is shorted)
J8	Open	DRINV to logic low
J9L	Open	LINV to logic low
J9M	Open	MINV to logic low
J10	Open	No inversion for U14C and U14D
J11	Open	No inversion for U14E
J12	Open	No inversion for DREAD
J13	Open	No inversion of clock signal to P1
J14	Short	P1, pins 33, 34, 37 to DGND
J16	Short	U10 (DAC) set for a fixed gain
J17A	Open	Required jumper configuration for U10
J17B	Short	Required jumper configuration for U10
J18A	Open	Required jumper configuration for U10
J18B	Short	Required jumper configuration for U10

**An additional 10 jumpers are shipped with the board.*

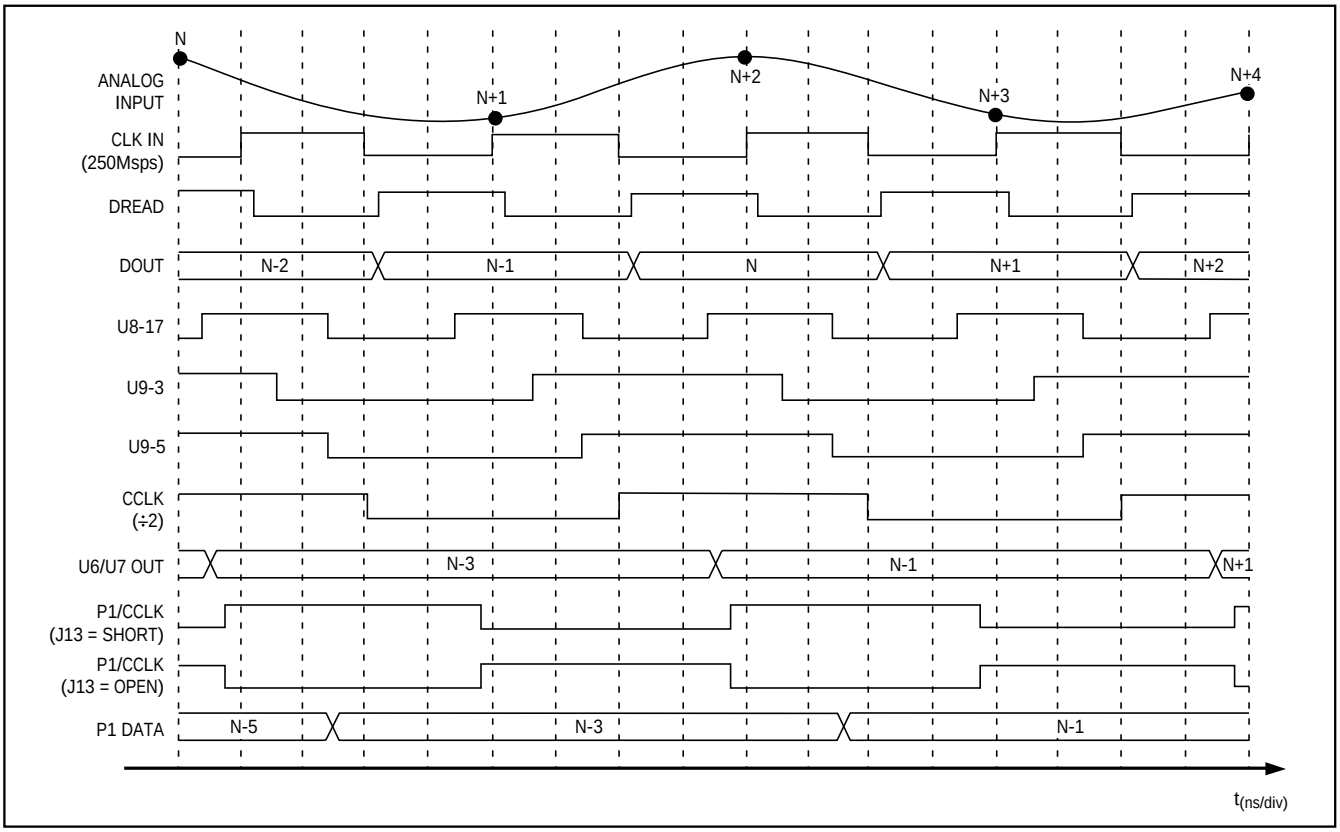


Figure 5. Timing Diagram

Notes:

1) Logic-Critical Timing Parameters:

DEVICE	tpd (ns)			SETUP/HOLD TIME	
	Min	Typ	Max	ts (min)	th (min)
100S307	200	700	1100	—	—
100S336	440	900	1300	—	—
100S363	300	600	900	—	—
100S351	—	1000	1400	500	550

2) All timing parameters shown above are based on actual values, including logic-propagation delays and line-propagation delays.

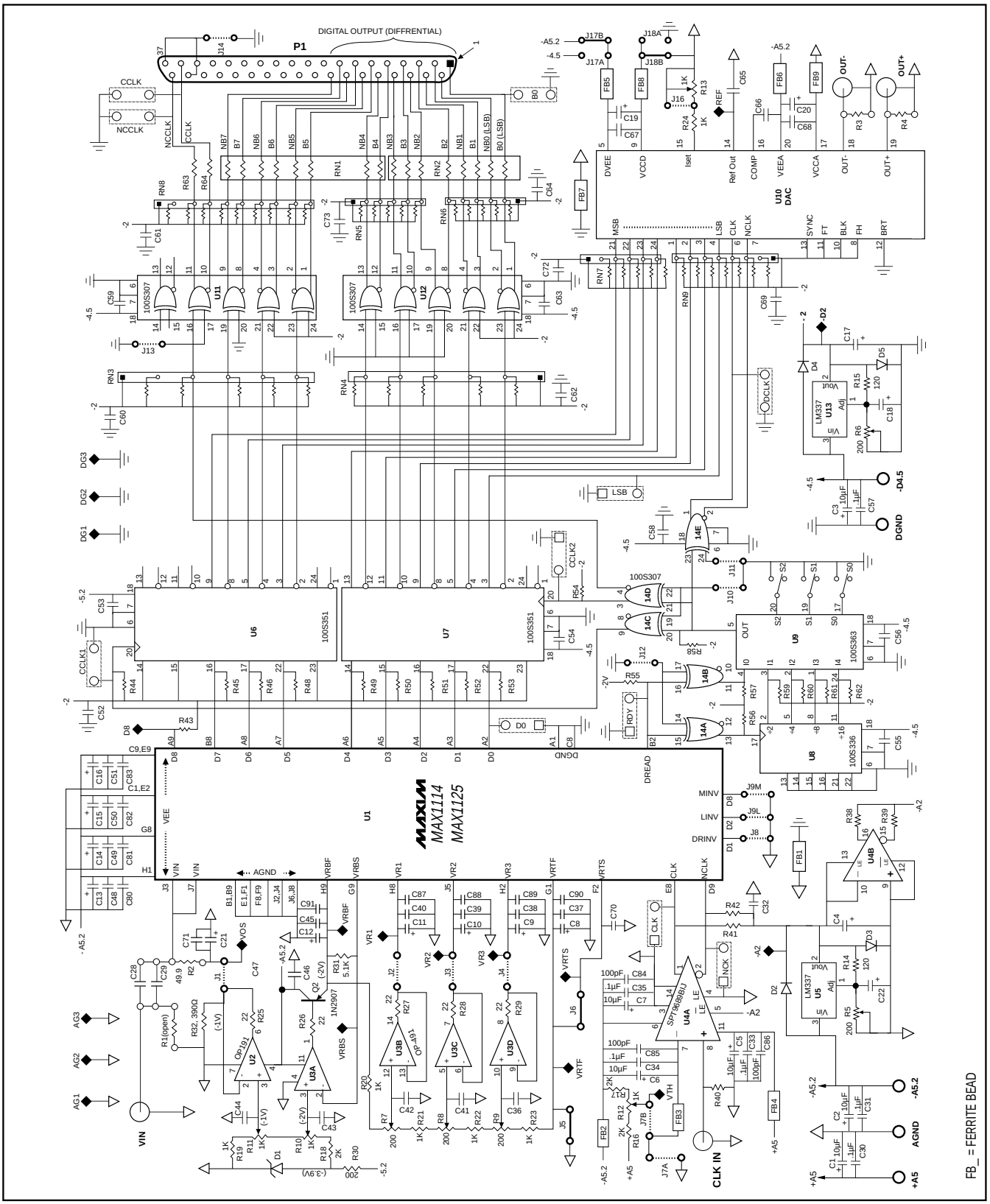


Figure 6. MAX1114/MAX1125 EV Kit Schematic

Start-Up and Calibration Procedures

Verify that jumpers are set as outlined in Table 4. Connect power supplies as recommended in Table 2 and Figure 2. Turn on all power supplies simultaneously.

Unless otherwise specified, all measurements are with respect to AGND.

1.0 References calibration

1.1 Verify that jumper J1 is installed. Monitor the VOS test point with a DVM and adjust potentiometer R11 for -1.000V ± 0.003V.

1.2 Monitor the VRBS test point with a DVM and adjust potentiometer R10 for -2.000V ± 0.005V.

1.3 Measure and record VRBF.

1.4 Verify that jumpers J5 and J6 are installed.

1.5 Install J2. Monitor the VR1 test point with a DVM and adjust potentiometer R7 for VR1 = 3/4 VRBF.

1.6 Verify that jumper J3 is installed. Monitor VR2 with a DVM and adjust potentiometer R8 for VR2 = 1/2VRBF.

1.7 Install jumper J4. Monitor VR3 with a DVM and adjust potentiometer R9 for VR3 = 1/4VRBF.

Note: Procedures 1.5 and 1.7 are performed only if the additional reference ladder taps (VR1 and VR3) are to be used.

2.0 Clock-driver calibration. No calibration is necessary for the clock-input driver. For the recommended 50% duty cycle, verify that J7A is installed instead of J7B.

2.1 Monitor the -A2 test point with DVM and adjust potentiometer R5 for -2.00V ± 0.01V.

3.0 -2V digital output pulldown calibration

3.1 Monitor -D2 with a DVM with respect to DGND, and adjust potentiometer R6 for -2.00V ± 0.01V.

4.0 Reconstruction DAC

4.1 Verify that the jumper J16 is installed. No adjustment is necessary for U10.

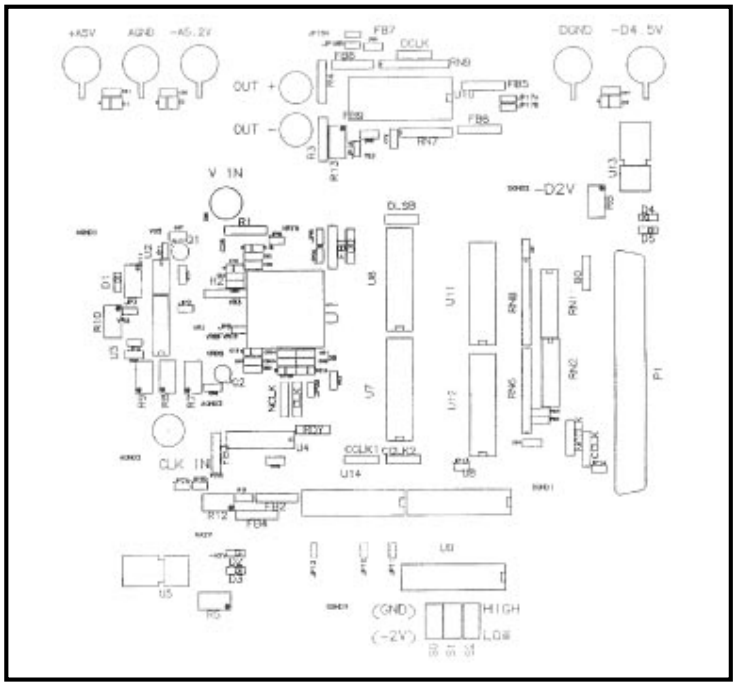


*Figure 7. MAX114/MAX1125 EV Kit Component Placement Guide—Component-Side Silk Screen**

**Not to scale*

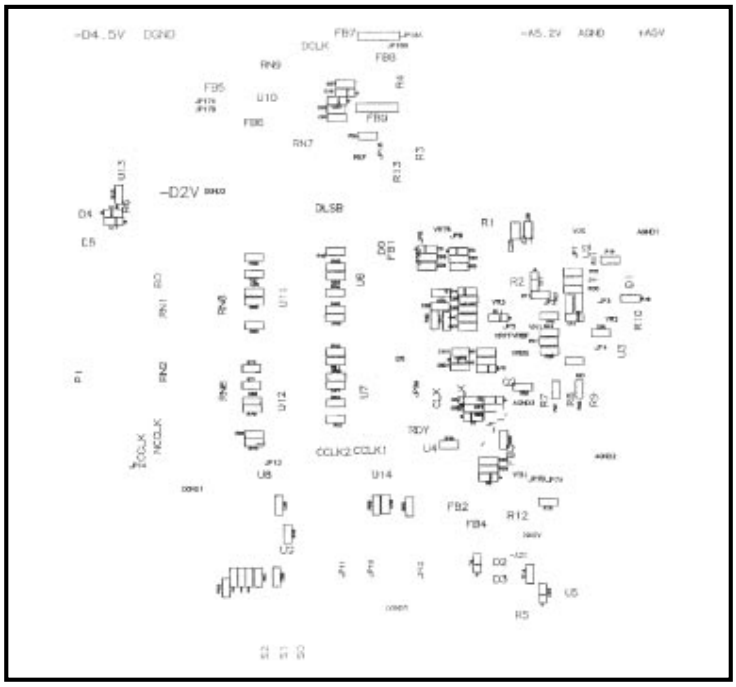


*Figure 8. MAX1114/MAX1125 EV Kit Component Placement Guide—Solder-Side Silk Screen**

**Not to scale*

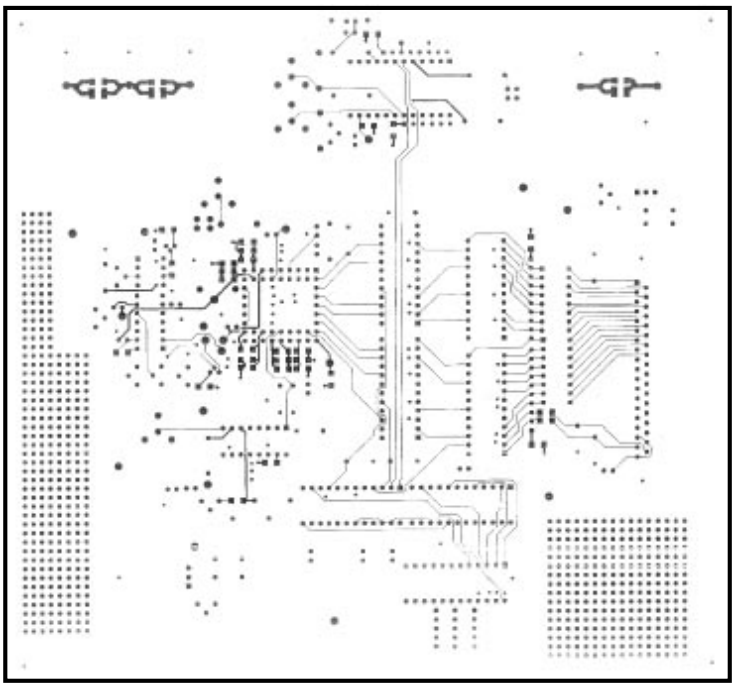


*Figure 9. MAX1114/MAX1125 EV Kit Component Placement Guide—Component-Side Layout**

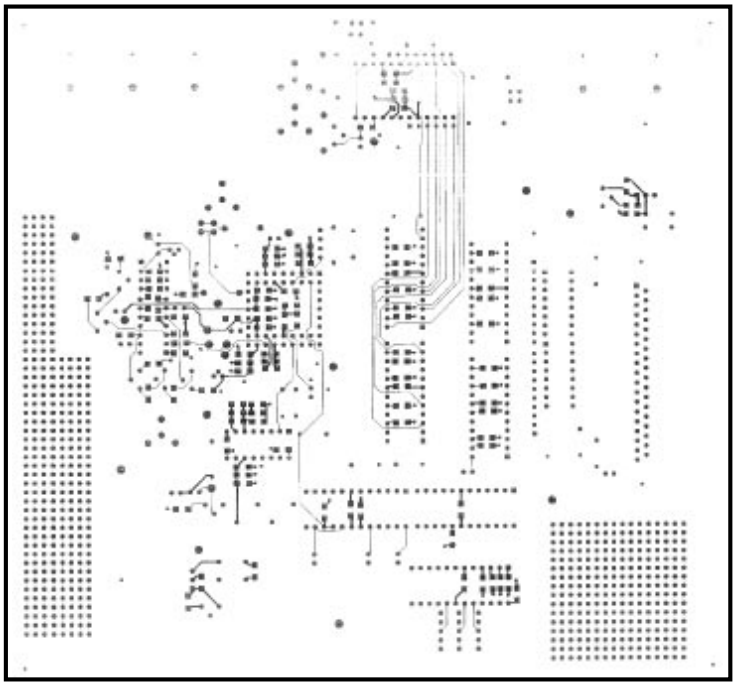


*Figure 10. MAX1114/MAX1125 EV Kit Component Placement Guide—Solder-Side Layout**

**Not to scale*

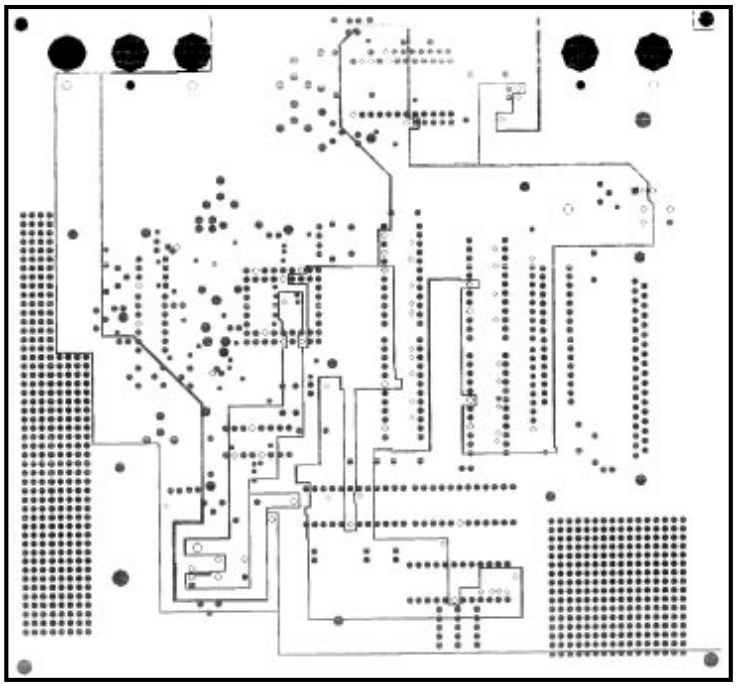


*Figure 11. MAX1114/MAX1125 EV Kit PC Board Layout—Power Plane**

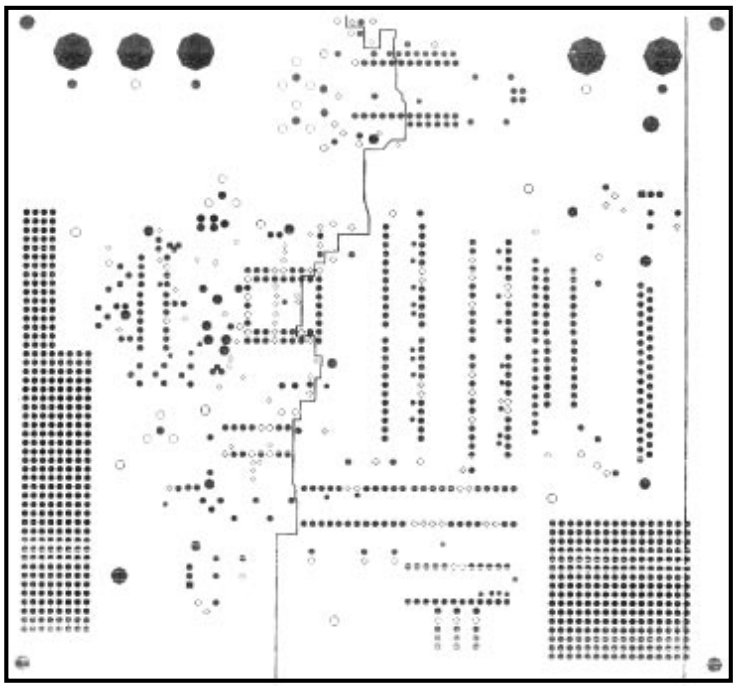


*Figure 12. MAX1114/MAX1125 EV Kit PC Board Layout—Ground Plane**

**Not to scale*