19-1129; Rev 2; 7/97

MAXIM

Ultra-High-Speed, +3V/+5V, Rail-to-Rail, Single-Supply Comparators

General Description

The MAX961–MAX964 are ultra-high-speed, single/dual/quad comparators with internal hysteresis. These devices are optimized for single +3V or +5V operation. The input common-mode range extends 100mV beyond both supply rails, and the outputs can sink or source 4mA to within 0.52V of GND and V_{CC}. Propagation delay is under 7ns (5mV overdrive), while supply current is 5.5mA per comparator.

The MAX961/MAX963 feature complementary outputs, a low-power shutdown mode, and a latch-enable function. The latch function enables the user to hold a valid comparator output. In shutdown mode, the MAX961/MAX963/MAX964 consume only 270µA supply current per comparator. The single MAX961 and dual MAX962 are available in space-saving 8-pin µMAX packages.

Features

- ♦ **Ultra-Fast, 4.5ns Propagation Delay**
- ♦ **Ideal for +3V and +5V Single-Supply Applications**
- ♦ **Rail-to-Rail® Input Voltage Range**
- ♦ **3.5mV Internal Hysteresis for Clean Switching**
- ♦ **Output Latch (MAX961/MAX963)**
- ♦ **TTL/CMOS-Compatible Complementary Outputs (MAX961/MAX963)**
- ♦ **270µA Shutdown Current per Comparator (MAX961/MAX963/MAX964)**
- ♦ **Available in Space-Saving Packages:**
  8-Pin µMAX (MAX961/MAX962)
  16-Pin QSOP (MAX964)

Applications

3V/5V Systems

Battery-Powered Systems

Threshold Detectors/Discriminators

Line Receivers

Zero-Crossing Detectors

High-Speed Sampling Circuits

Ordering Information

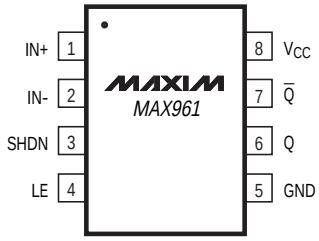
PART	TEMP. RANGE	PIN-PACKAGE
MAX961ESA	-40°C to +85°C	8 SO
MAX961EUA	-40°C to +85°C	8 µMAX
MAX962ESA	-40°C to +85°C	8 SO
MAX962EUA	-40°C to +85°C	8 µMAX
MAX963ESD	-40°C to +85°C	14 SO
MAX964ESE	-40°C to +85°C	16 Narrow SO
MAX964EEE	-40°C to +85°C	16 QSOP

Selector Guide

PART	NO. OF COMPARATORS	COMPLEMENTARY OUTPUT	SHUTDOWN	LATCH ENABLE	PACKAGE
MAX961	1	Yes	Yes	Yes	8 SO/µMAX
MAX962	2	No	No	No	8 SO/µMAX
MAX963	2	Yes	Yes	Yes	14 SO
MAX964	4	No	Yes	No	16 SO/QSOP

Pin Configurations

TOP VIEW



SO/µMAX

Pin Configurations continued at end of data sheet.

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Ultra-High-Speed, +3V/+5V, Rail-to-Rail, Single-Supply Comparators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} to GND.....+6V to -0.3V
All Other Pins.....-0.3V to (V_{CC} + 0.3V)
Duration of Output Short Circuit to GND or V_{CC} .....Continuous
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 5.88mW/°C above +70°C).....471mW/°C
8-Pin µMAX (derate 4.10mW/°C above +70°C).....330mW/°C
14-Pin SO (derate 8.33mW/°C above +70°C).....667mW/°C
16-Pin SO (derate 8.70mW/°C above +70°C).....696mW/°C
16-Pin QSOP (derate 8.33mW/°C above +70°C)....667mW/°C
Operating Temperature Range
MAX96_E .....-40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, V_{CM} = 0V, C_{OUT} = 5pF, V_{SHDN} = 0V, V_{LE} = 0V, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		T_A = +25°C			T_{MIN} to T_{MAX}		UNITS
				MIN	TYP	MAX	MIN	MAX	
Supply Voltage	V_{CC}	Inferred by PSRR		2.7		5.5	2.7	5.5	V
Input Common-Mode Voltage Range	V_{CMR}	(Note 2)		-0.1		V_{CC} + 0.1	-0.1	V_{CC} + 0.1	V
Input-Referred Trip Points	V_{TRIP}	V_{CM} = - 0.1V or 5.1V, V_{CC} = 5V (Note 3)	MAX96_UA		±2.0	±3.5		±5.2	mV
			All other packages		±2.0	±3.5		±4.0	
Input-Referred Hysteresis					3.5				mV
Input Offset Voltage	V_{OS}	V_{CM} = - 0.1V or 5.1V, V_{CC} = 5V (Note 4)	MAX96_UA		±0.5	±1.5		±3.5	mV
			All other packages		±0.5	±1.5		±2.0	
Input Bias Current	I_B	V_{IN+} = V_{IN-} = 0V or V_{CC}, V_{CC} = 5V	MAX96_UA			±15		±30	µA
			All other packages			±15		±15	
Differential Input Clamp Voltage		V_{CC} = 5.5V, V_{IN-} = 0V, I_{IN+} = 100µA			2.1				V
Input Capacitance					3				pF
Differential Input Impedance	R_{IND}	V_{CC} = 5V			8				kΩ
Common-Mode Input Impedance	R_{INCM}	V_{CC} = 5V			130				kΩ
Common-Mode Rejection Ratio	CMRR	V_{CC} = 5V, V_{CM} = -0.1V to 5.1V (Note 5)			0.1	0.3		0.5	mV/V
Power-Supply Rejection Ratio	PSRR	V_{CM} = 0V (Note 6)			0.05	0.3		0.3	mV/V
Output High Voltage	V_{OH}	I_{SOURCE} = 4mA		V_{CC} - 0.52			V_{CC} - 0.52		V
Output Low Voltage	V_{OL}	I_{SINK} = 4mA				0.52		0.52	V
Capacitive Slew Current		V_{OUT} = 1.4V, V_{CC} = 2.7V		30	60				mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, V_{CM} = 0V, C_{OUT} = 5pF, V_{SHDN} = 0V, V_{LE} = 0V, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_{MIN} to T_{MAX}		UNITS
			MIN	TYP	MAX	MIN	MAX	
Output Capacitance				4				pF
Supply Current per Comparator	I_{CC}	MAX961/MAX963, V_{CC} = 5V		8.5	11		11	mA
		MAX962/MAX964, V_{CC} = 5V		5.5	8		9	
Shutdown Supply Current per Comparator	I_{SHDN}	MAX961/MAX963/MAX964, V_{CC} = 5V		0.27	0.5		0.5	mA
Shutdown Output Leakage Current		MAX961/MAX963/MAX964, V_{OUT} = 0.5V and V_{CC} - 0.5V			1		20	µA
Rise/Fall Time	t_R, t_F	V_{CC} = 5V		2.3				ns
Logic Input High	V_{IH}		(V_{CC} / 2) + 0.4			(V_{CC} / 2) + 0.4		V
Logic Input Low	V_{IL}				(V_{CC} / 2) - 0.4		(V_{CC} / 2) - 0.4	V
Logic Input Current	I_{IL}, I_{IH}	V_{LOGIC} = 0V or V_{CC}			±15		±30	µA
Propagation Delay	t_{PD}	5mV overdrive (Note 7)		4.5	7		8.5	ns
Differential Propagation Delay	t_{PD}	Between any two channels or outputs (Q/$\overline{Q}$)		0.3				ns
Propagation-Delay Skew	t_{SKEW}	Between t_{PD-} and t_{PD+}		0.3				ns
Data-to-Latch Setup Time	t_{SU}	(Note 8)			5		5	ns
Latch-to-Data Hold Time	t_H	(Note 8)			5		5	ns
Latch Pulse Width	t_{LPW}	(Note 8)			5		5	ns
Latch Propagation Delay	t_{LPD}	(Note 8)			10		10	ns
Shutdown Time	t_{OFF}	Delay until output is high-Z (>10kΩ)		150				ns
Shutdown Disable Time	t_{ON}	Delay until output is valid		250				ns

Note 1: The MAX961EUA/MAX962EUA are 100% production tested at T_A = +25°C; all temperature specifications are guaranteed by design.

Note 2: Inferred by CMRR. Either input can be driven to the absolute maximum limit without false output inversion, provided that the other input is within the input voltage range.

Note 3: The input-referred trip points are the extremities of the differential input voltage required to make the comparator output change state. The difference between the upper and lower trip points is equal to the width of the input-referred hysteresis zone. (See Figure 1.)

Note 4: Input offset voltage is defined as the mean of the trip points.

Note 5: CMRR = (V_{OSL} - V_{OSH}) / 5.2V, where V_{OSL} is the offset at V_{CM} = -0.1V and V_{OSH} is the offset at V_{CM} = 5.1V.

Note 6: PSRR = (V_{OS}2.7 - V_{OS}5.5) / 2.8V, where V_{OS}2.7 is the offset voltage at V_{CC} = 2.7V, and V_{OS}5.5 is the offset voltage at V_{CC} = 5.5V.

Note 7: Propagation delay cannot be measured in automatic test equipment with low input overdrive values. The MAX96_ES_ devices are sample tested to 0.1% AQL, with a 200mV step and 100mV overdrive at T_A = +25°C. Correlation tests show that t_{PD} can be guaranteed with this test, since additional DC tests are performed that guarantee that all internal bias conditions are correct. Propagation delay on the µMAX and QSOP packages is guaranteed by design. For low-overdrive conditions, V_{OS} is added to the overdrive.

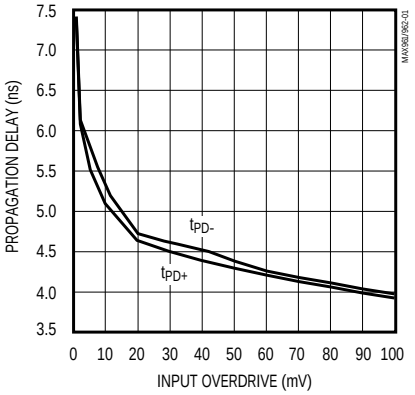
Note 8: Guaranteed by design.

Ultra-High-Speed, +3V/+5V, Rail-to-Rail, Single-Supply Comparators

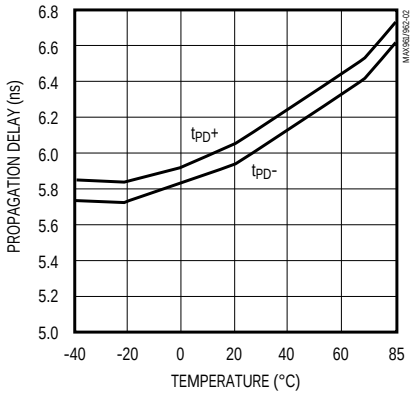
Typical Operating Characteristics

(V_{CC} = +3.0V, 5mV of overdrive, T_A = +25°C, unless otherwise noted.)

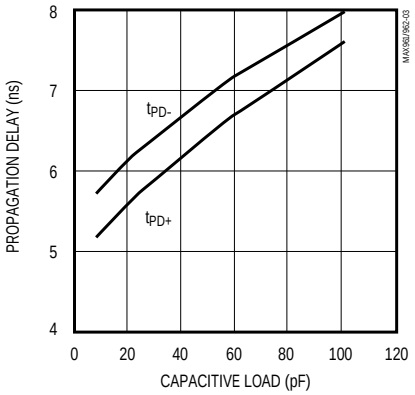
PROPAGATION DELAY vs. INPUT OVERDRIVE



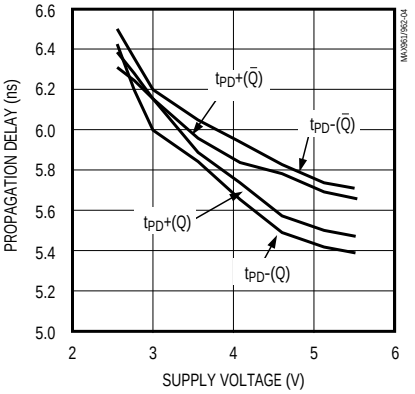
PROPAGATION DELAY vs. TEMPERATURE



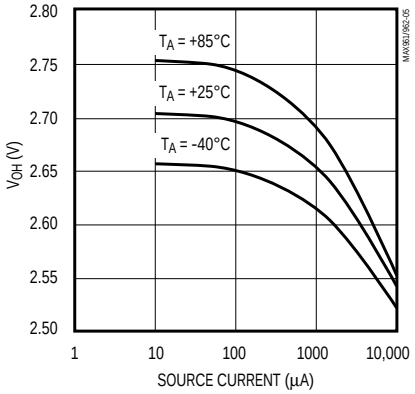
PROPAGATION DELAY vs. CAPACITIVE LOAD



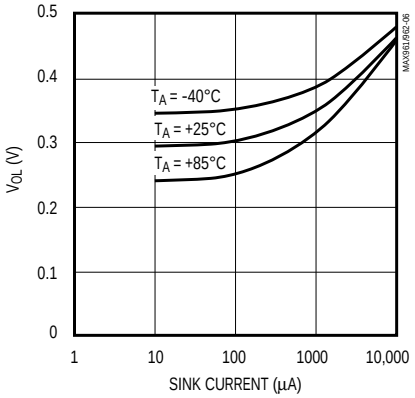
PROPAGATION DELAY vs. SUPPLY VOLTAGE



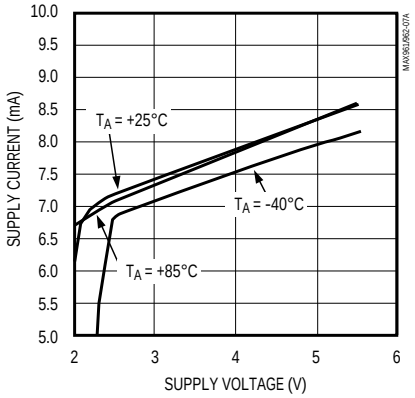
OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



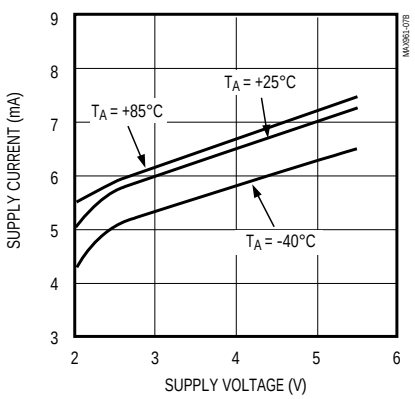
OUTPUT LOW VOLTAGE vs. SINK CURRENT



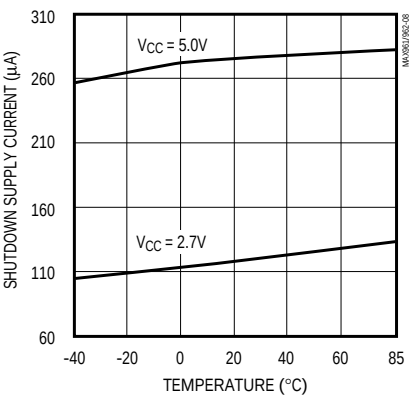
MAX961/MAX963 SUPPLY CURRENT PER COMPARATOR vs. SUPPLY VOLTAGE



MAX962/MAX964 SUPPLY CURRENT PER COMPARATOR vs. SUPPLY VOLTAGE



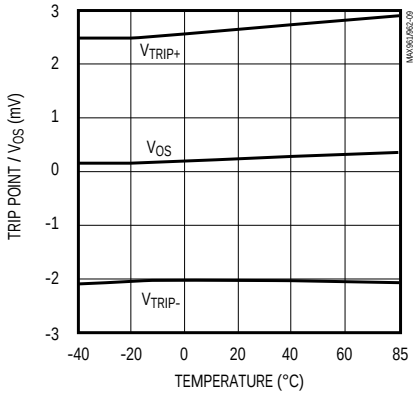
MAX961/MAX963/MAX964 SHUTDOWN SUPPLY CURRENT PER COMPARATOR vs. TEMPERATURE



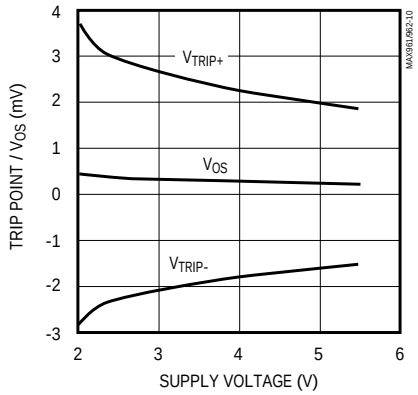
Typical Operating Characteristics (continued)

(V_{CC} = +3.0V, 5mV of overdrive, T_A = +25°C, unless otherwise noted.)

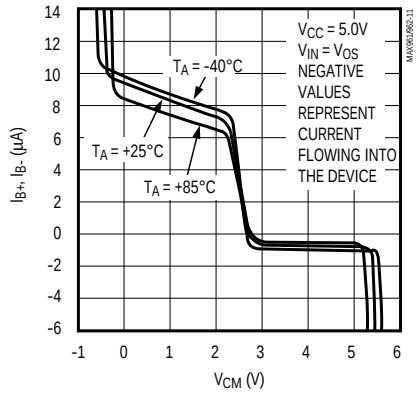
VOLTAGE TRIP POINT/INPUT OFFSET VOLTAGE vs. TEMPERATURE



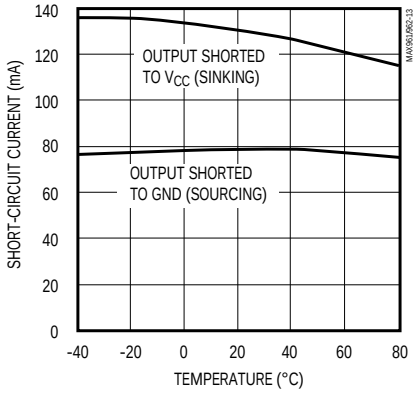
VOLTAGE TRIP POINT/INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE



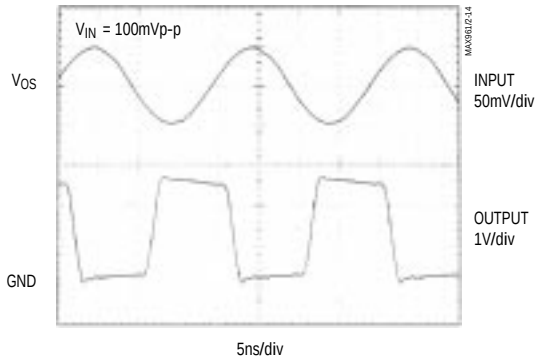
INPUT BIAS CURRENT (I_{B+}, I_{B-}) vs. COMMON-MODE VOLTAGE



SHORT-CIRCUIT OUTPUT CURRENT vs. TEMPERATURE



50MHz RESPONSE

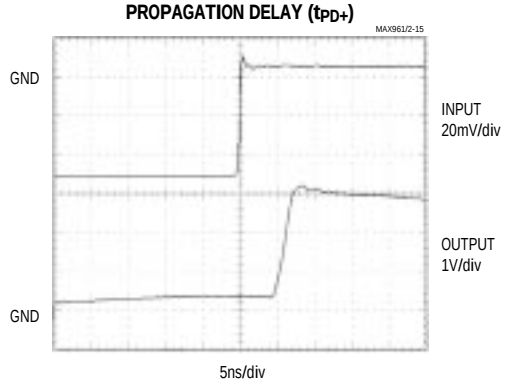


Ultra-High-Speed, +3V/+5V, Rail-to-Rail, Single-Supply Comparators

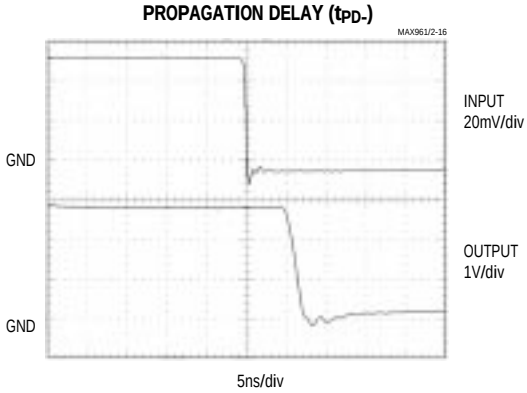
Typical Operating Characteristics (continued)

(V_{CC} = +3.0V, 5mV of overdrive, T_A = +25°C, unless otherwise noted.)

PROPAGATION DELAY (t_{PD+})



PROPAGATION DELAY (t_{PD-})



Pin Description

PIN				NAME	FUNCTION
MAX961	MAX962	MAX963	MAX964		
2	2	1	1	INA-	Comparator A Inverting Input
1	1	2	2	INA+	Comparator A Noninverting Input
4	—	3, 5	—	LE, LEA, LEB	Latch-Enable Input. The output latches when LE_ is high. The latch is transparent when LE_ is low.
5	5	4, 11	12	GND	Ground
—	—	—	16	N.C.	No Connect. Connect to GND to prevent parasitic feedback.
—	4	6	3	INB-	Comparator B Inverting Input
—	3	7	4	INB+	Comparator B Noninverting Input
—	—	—	5	INC-	Comparator C Inverting Input
—	—	—	6	INC+	Comparator C Noninverting Input
—	—	—	7	IND-	Comparator D Inverting Input
—	—	—	8	IND+	Comparator D Noninverting Input
3	—	8	9	SHDN	Shutdown Input. The device shuts down when SHDN is high.
—	6	9	14	QB	Comparator B Output
—	—	—	11	QC	Comparator C Output
—	—	—	10	QD	Comparator D Output
—	—	10	—	$\overline{QB}$	Comparator B Complementary Output
8	8	12	13	V_{CC}	Positive Supply Input (V_{CC} to GND must be ≤5.5V)
6	7	13	15	QA	Comparator A TTL Output
7	—	14	—	$\overline{QA}$	Comparator A Complementary Output

Detailed Description

The MAX961–MAX964 single-supply comparators feature internal hysteresis, ultra-high-speed operation, and low power consumption. Their outputs are guaranteed to pull within 0.52V of either rail without external pull-up or pull-down circuitry. Rail-to-Rail input voltage range and low-voltage, single-supply operation make these devices ideal for portable equipment. The MAX961–MAX964 all interface directly to CMOS logic.

Timing

Most high-speed comparators oscillate in the linear region because of noise or undesirable parasitic feedback. This can occur when the voltage on one input is close to or equal to the voltage on the other input. These devices have a small amount of internal hysteresis to counter parasitic effects and noise.

The added hysteresis of the MAX961–MAX964 creates two trip points: one for the rising input voltage and one for the falling input voltage (Figure 1). The difference between the trip points is the hysteresis. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. The MAX961–MAX964's fixed internal hysteresis eliminates these resistors.

Figure 1 illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except for an inverted output.

The MAX961/MAX963 include internal latches that allow storage of comparison results. LE has a high input impedance. If LE is low, the latch is transparent (i.e., the comparator operates as though the latch is not present). The comparator's output state is stored when LE is pulled high. All timing constraints must be met when using the latch function (Figure 2).

Input Stage Circuitry

The MAX961–MAX964 include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages. This protection circuitry consists of two groups of three front-to-back diodes between IN+ and IN-, as well as two 200Ω resistors (Figure 3). The diodes limit the differential voltage applied to the comparator's internal circuitry to no more than $3V_F$, where V_F is the diode's forward-voltage drop (about 0.7V at +25°C).

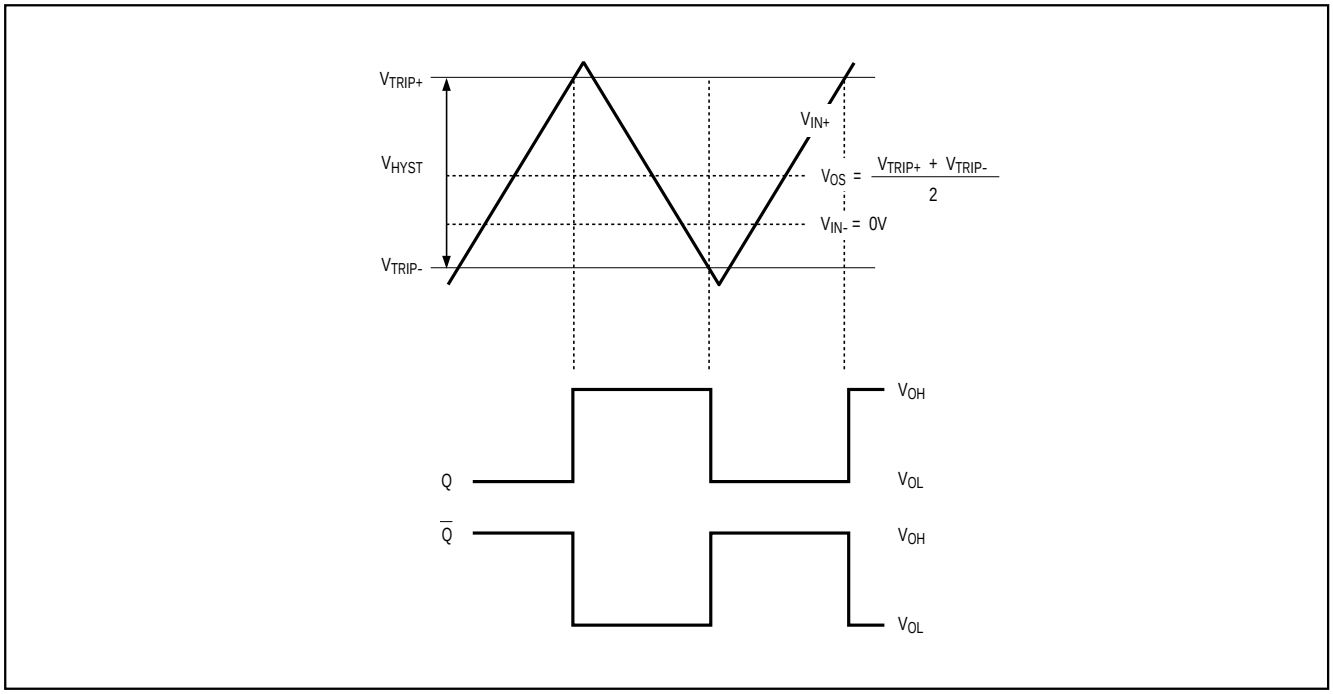


Figure 1. Input and Output Waveforms, Noninverting Input Varied

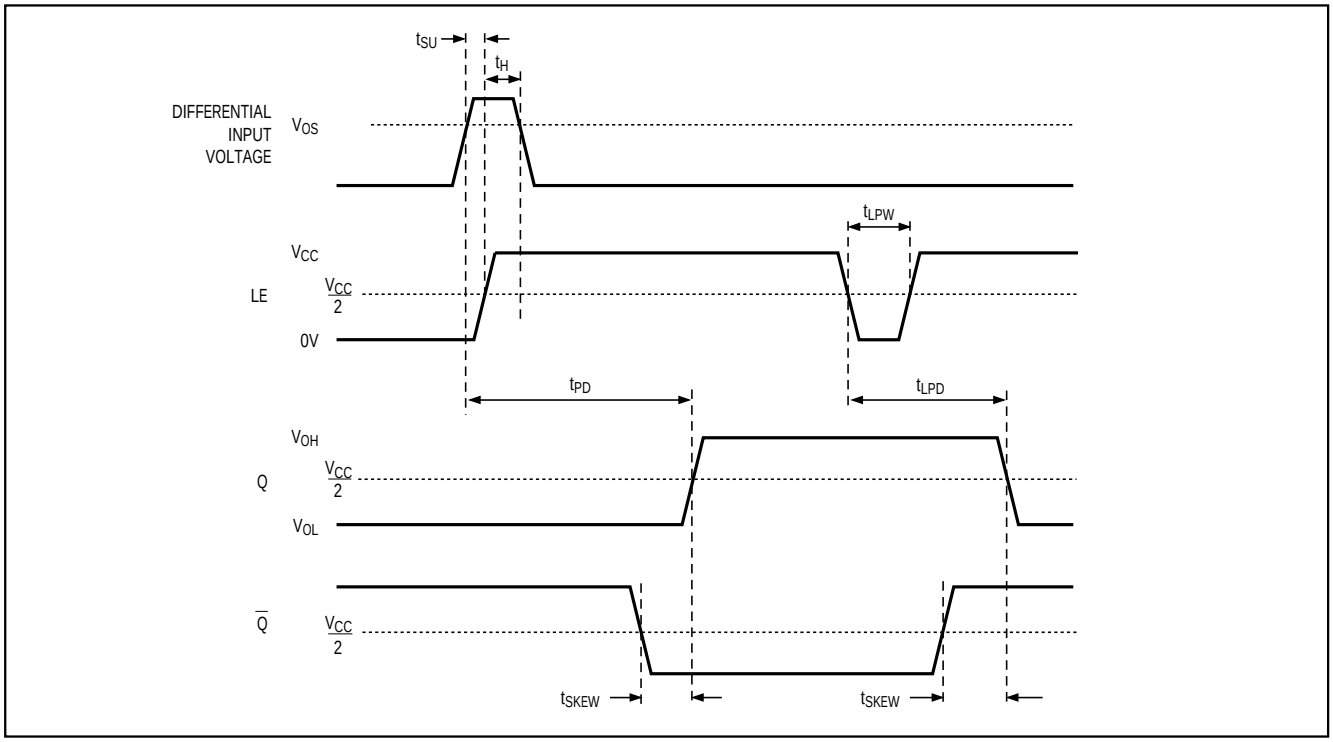


Figure 2. MAX961/MAX963 Timing Diagram

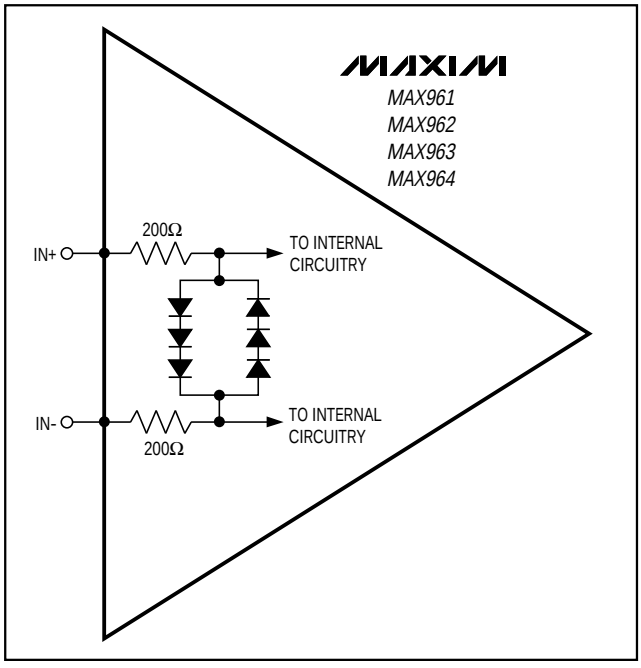


Figure 3. Input Stage Circuitry

For a large differential input voltage (exceeding $3V_F$), this protection circuitry increases the input bias current at IN+ (source) and IN- (sink).

$$\text{Input current} = \frac{(IN+ - IN-) - 3V_F}{2 \times 200}$$

Input currents with large differential input voltages should not be confused with input bias currents (I_B). As long as the differential input voltage is less than $3V_F$, this input current is less than $2I_B$. The protection circuitry also allows for the MAX961–MAX964's input common-mode range to extend beyond both power-supply rails. The output remains in the correct logic state if one or both inputs are within the common-mode range. Taking either input outside the common-mode range causes the input to saturate and the propagation delay to increase.

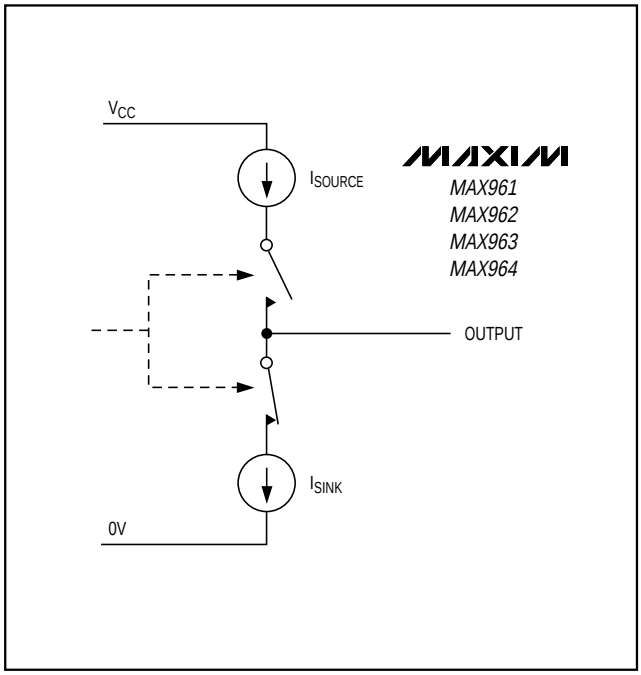


Figure 4. Output Stage Circuitry

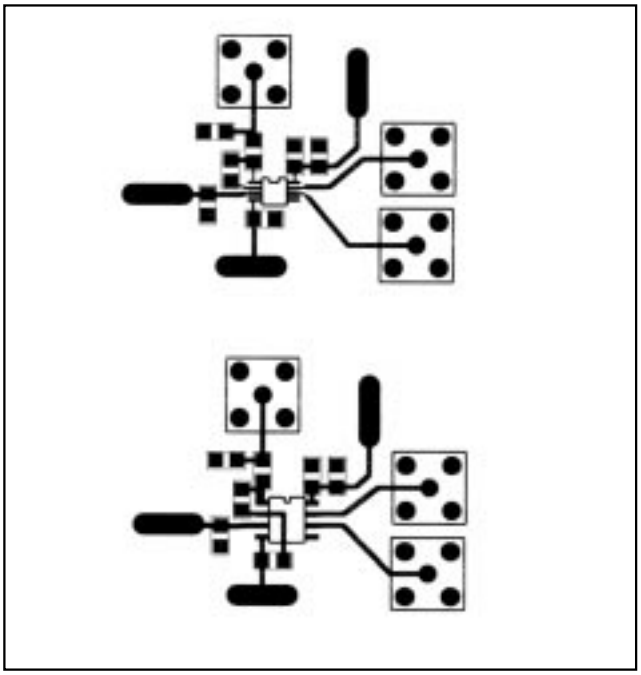


Figure 5. MAX961 PC Board Layout

Output Stage Circuitry

The MAX961–MAX964 contain a current-driven output stage, as shown in Figure 4. During an output transition, I_{SOURCE} or I_{SINK} is pushed or pulled to the output pin. The output source or sink current is high during the transition, creating a rapid slew rate. Once the output voltage reaches V_{OH} or V_{OL}, the source or sink current decreases to a small value, capable of maintaining the V_{OH} or V_{OL} in static condition. This decrease in current conserves power after an output transition has occurred.

One consequence of a current-driven output stage is a linear dependence between the slew rate and the load capacitance. A heavy capacitive load slows down the voltage output transition. This is useful in noise-sensitive applications, where fast edges may cause interference.

Shutdown Mode

When SHDN is high, the MAX961/MAX963/MAX964 shut down. When shut down, the supply current drops to 270µA per comparator, and the outputs become high impedance. SHDN has a high input impedance. Connect SHDN to GND for normal operation. Exit shutdown with LE low; otherwise, the output is indeterminate.

Applications Information

Circuit Layout and Bypassing

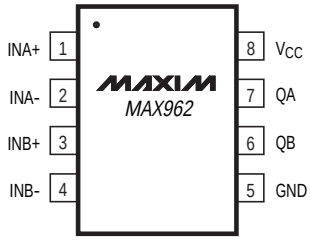
The MAX961–MAX964's high bandwidth requires a high-speed layout:

1) Use a printed circuit board with a good, unbroken, low-inductance ground plane.
2) Place a decoupling capacitor (a 0.1µF ceramic surface-mount capacitor is a good choice) as close to V_{CC} as possible.
3) On the inputs and outputs, keep lead lengths short to avoid unwanted parasitic feedback around the comparators. Keep inputs away from outputs. Keep impedance between the inputs low.
4) Solder the device directly to the printed circuit board rather than using a socket.
5) Figure 5 depicts the recommended circuit layout.
6) For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes negligible degradation to t_{PD} when the source impedance is low.

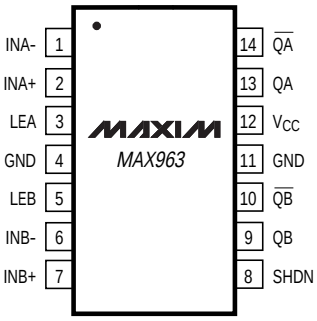
Ultra-High-Speed, +3V/+5V, Rail-to-Rail, Single-Supply Comparators

Pin Configurations

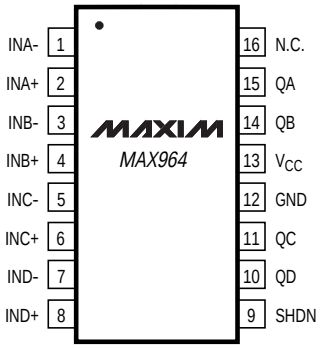
TOP VIEW



SO/µMAX



SO



SO/QSOP

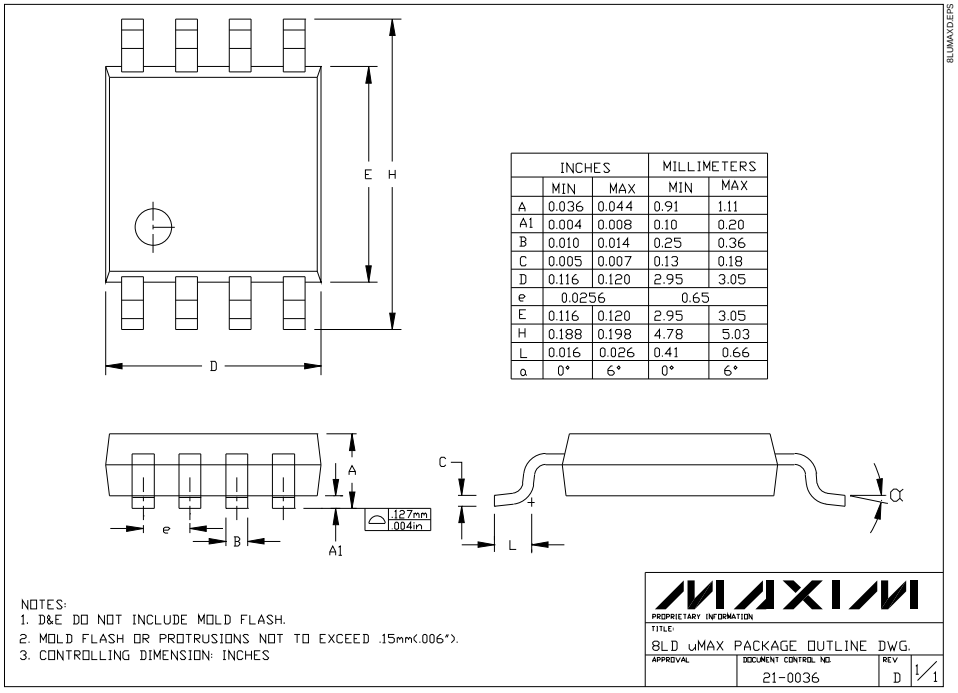
Chip Information

TRANSISTOR COUNT:

MAX961/MAX962: 286

MAX963/MAX964: 607

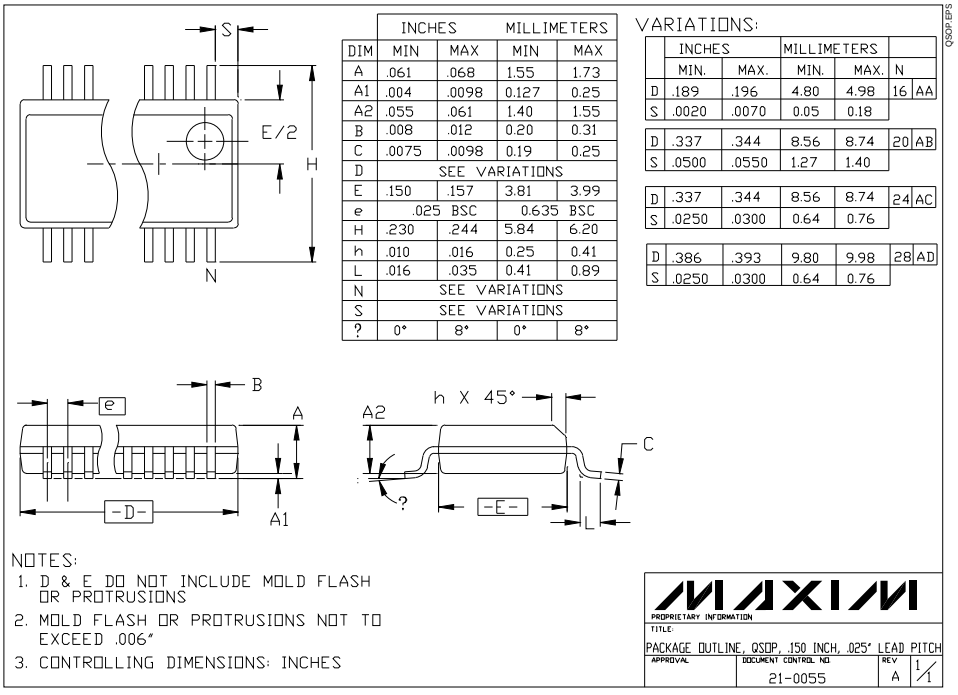
Package Information



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256		0.65	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm(.006").
3. CONTROLLING DIMENSION: INCHES

MAXIM
PROPRIETARY INFORMATION
TITLE:
8LD uMAX PACKAGE OUTLINE DWG.
APPROVAL | DOCUMENT CONTROL NO. 21-0036 | REV D | 1/1



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.127	0.25
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.19	0.25
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
S	SEE VARIATIONS			
?	0°	8°	0°	8°

VARIATIONS:

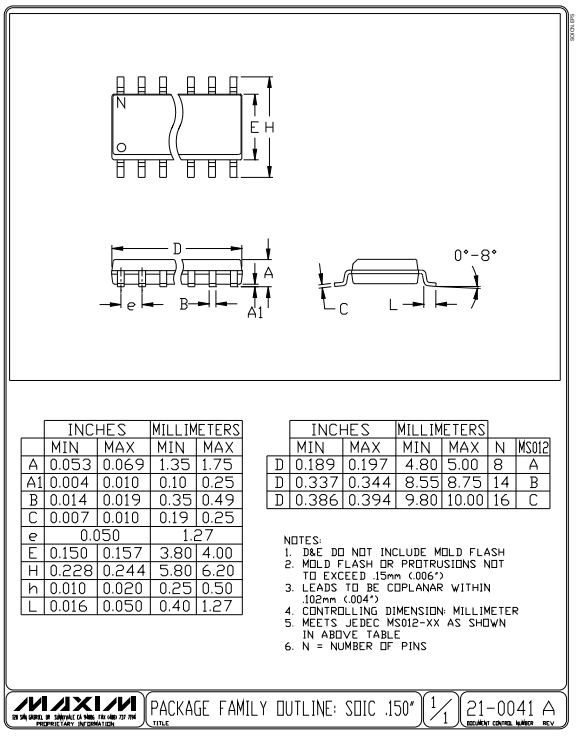
	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.27	1.40		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.64	0.76		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.64	0.76		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006"
3. CONTROLLING DIMENSIONS: INCHES

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP, .150 INCH, .025" LEAD PITCH
APPROVAL | DOCUMENT CONTROL NO. 21-0055 | REV A | 1/1

Ultra-High-Speed, +3V/+5V, Rail-to-Rail, Single-Supply Comparators

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SOIC .150" | 1/1 | 21-0041 A