19-1099; Rev 1; 9/96

MAXIM

Low-Power, +2.5V to +5.5V, Dual 8-Bit Voltage-Output DAC in µMAX

General Description

The MAX549 dual, serial 8-bit, voltage-output, digital-to-analog converter (DAC) operates on a single +2.5V to +5.5V supply. Its ±1LSB TUE specification is guaranteed over temperature. Operating current (supply current plus reference current) is typically 150µA with V_{DD} = 2.5V and less than 1µA in shutdown mode.

The interface operates at clock rates up to 10MHz and is compatible with 3-wire SPI™, QSPI™, and Microwire™ interface standards. The serial input shift register is 16 bits: 8 bits for DAC selection and shutdown control, and 8 bits of DAC input data.

The MAX549's ultra-low power consumption and small µMAX package make it ideal for portable and battery-powered applications.

Applications

VCXO Control

Comparator Level Settings

GaAs Amp Bias Control

Digital Gain and Offset Control

Features

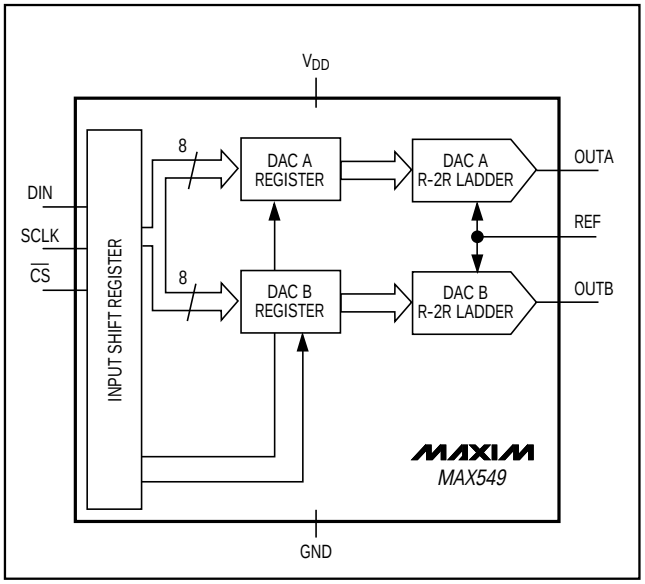
- **+2.5V to +5.5V Single-Supply Operation**
- **±1LSB (max) TUE**
- **Low 150µA Operating Current (V_{DD} = +2.5V)**
- **1µA Shutdown Mode**
- **µMAX Package—50% Smaller than 8-Pin SO**
- **10MHz, 3-Wire Serial Interface**
- **Internal Power-On Reset Clears All Registers to Zero**

Ordering Information

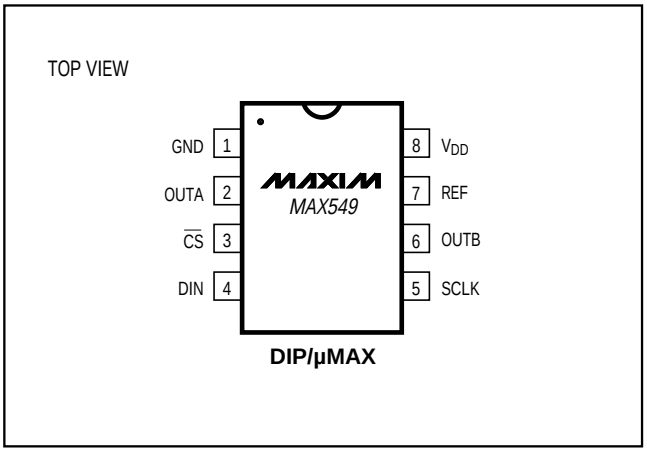
PART	TEMP. RANGE	PIN-PACKAGE
MAX549BCPA	0°C to +70°C	8 Plastic DIP
MAX549BCUA	0°C to +70°C	8 µMAX
MAX549BC/D	0°C to +70°C	Dice*
MAX549BEPA	-40°C to +85°C	8 Plastic DIP
MAX549BEUA	-40°C to +85°C	8 µMAX

**Dice are specified at T_A = +25°C, DC parameters only.*

Functional Diagram



Pin Configuration



DIP/µMAX

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ABSOLUTE MAXIMUM RATINGS

V_{DD}, SCLK, D_{IN}, $\overline{CS}$, OUTA, OUTB to GND .....-0.3V to +6V
REF .....-0.3V to (V_{DD} + 0.3V)
Maximum Current (any pin) 50mA
Continuous Power Dissipation
Plastic DIP (derate 9.1mW/°C above +70°C) 727mW
µMAX (derate 4.1mW/°C above +70°C) 330mW
Operating Temperature Ranges
MAX549BC_A .....0°C to +70°C
MAX549BE_A .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			8			Bits
Differential Nonlinearity	DNL	Guaranteed monotonic	MAX549BC_A/MAX549BEPA			±0.9	LSB
			MAX549BEUA (Note 1)			±0.9	
Total Unadjusted Error	TUE		MAX549BC_A/MAX549BEPA			±1	LSB
			MAX549BEUA (Note 1)			±1	
Zero-Code Error	ZCE	T_A = +25°C				±1	LSB
Full-Scale Error	FSE					±1	LSB
REFERENCE INPUT							
Reference Input Voltage	V_{REF}	For specified performance		2.5		V_{DD}	V
Reference Input Resistance (Note 2)	R_{REF}	DAC code = 55 hex			16		kΩ
Reference Input Current (Note 3)	I_{REF}	DAC code = 55 hex	V_{DD} = V_{REF} = 5.5V		325	550	µA
			V_{DD} = V_{REF} = 2.5V		150	250	
DAC OUTPUTS (OUTA, OUTB)							
DAC Output Voltage Swing				0		REF	V
DAC Output Resistance	R_{OUT}				32		kΩ
DAC Output Resistance Match	$\Delta(R_{OUTA} - R_{OUTB})$				±0.2		%
DIGITAL INPUTS ($\overline{CS}$, SCLK, DIN)							
Input High Voltage	V_{IH}			0.7V_{DD}			V
Input Low Voltage	V_{IL}					0.3V_{DD}	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}				±1	µA
Input Capacitance (Note 4)	C_{IN}					10	pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE							
Digital Feedthrough and Crosstalk		$\overline{CS}$ = high, all digital inputs from 0V to V_{DD}			50		nV-sec
Voltage-Output Settling Time		To ±1/2LSB, C_L = 20pF			4		µs
Voltage-Output Slew Rate	SR	C_L = 20pF	V_{DD} = +2.5V		1.4		V/µs
			V_{DD} = +5.5V		3.1		
Wake-Up Time		C_{LOAD} = 20pF			4		µs
POWER SUPPLIES							
Supply Voltage Range	V_{DD}	Outputs unloaded, all inputs = GND or V_{DD}		2.5		5.5	V
Supply Current	I_{DD}	V_{DD} = +5.5V, outputs unloaded, all inputs = GND or V_{DD}			0.3	10	µA
Shutdown Current		Shutdown mode			0.3		µA

Note 1: 0°C to -40°C testing guaranteed by design using six sigma design limits.
Note 2: Worst-case input resistance at REF occurs at DAC code 55 hex.
Note 3: Worst-case reference input current occurs at DAC code 55 hex.
Note 4: Guaranteed by design. Not production tested.

TIMING CHARACTERISTICS (Note 5)

(V_{DD} = +2.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Digital inputs switching from 0V to V_{DD}.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
DIN to SCLK High Setup	t_{DS}		30			ns
DIN to SCLK High Hold	t_{DH}	V_{DD} = +2.5V	0			ns
		V_{DD} = +5.5V	10			
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		30			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		30			ns
SCLK High to $\overline{CS}$ Low Hold	t_{CSH0}	V_{DD} = 2.5V	10			ns
		V_{DD} = 5.5V	20			
Delay, SCLK High to $\overline{CS}$ High	t_{CSH1}		10			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		40			ns
SCLK Period	t_{CP}		80			ns
V_{DD} High to $\overline{CS}$ Low		Power-on reset delay			5	µs

Note 5: Guaranteed by design. Not production tested.

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Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2	OUTA	DAC A Output Voltage
3	$\overline{CS}$	Chip-Select Input. A logic low on $\overline{CS}$ enables serial data to be clocked into the input shift register. Programming commands are executed at $\overline{CS}$'s rising edge.
4	DIN	Serial Data Input. Data is clocked into the 16-bit input shift register on SCLK's rising edge.
5	SCLK	Serial Clock Input. Data is clocked in on SCLK's rising edge.
6	OUTB	DAC B Output Voltage
7	REF	External Reference Voltage Input for DAC A and DAC B (2.5V to V_{DD})
8	V_{DD}	Positive Power Supply (+2.5V to +5.5V)

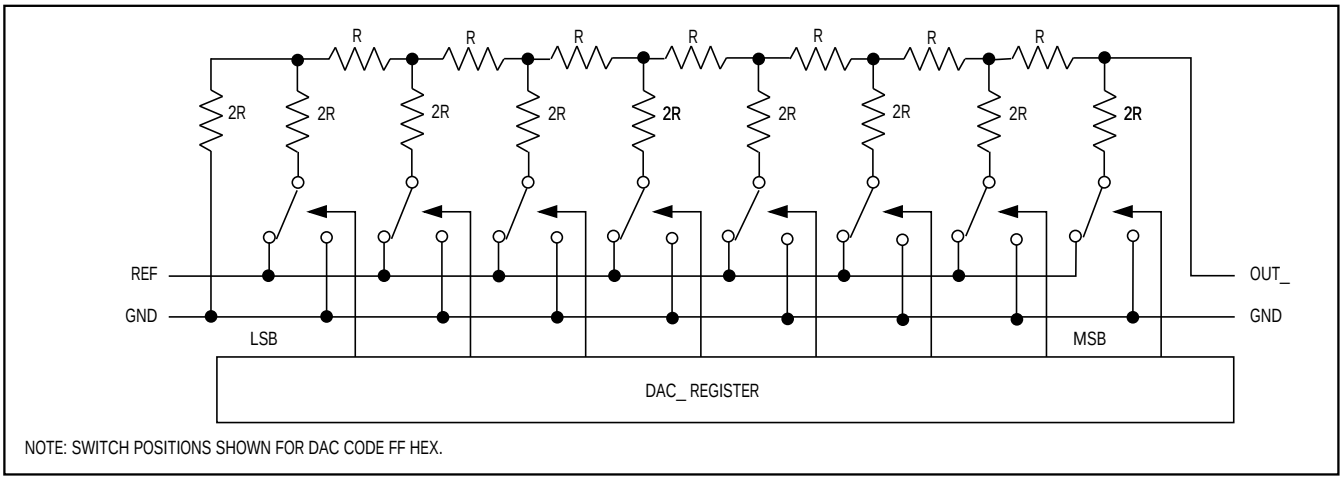

Figure 1. DAC Simplified Circuit Diagram

Detailed Description

Analog Section

The MAX549 is a dual, 8-bit, voltage-output digital-to-analog converter (DAC). Each DAC consists of an R-2R ladder network that converts 8-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltage (Figure 1). The MAX549's outputs are unbuffered and have a typical output resistance of 32kΩ. The external reference is used by both DACs. The power-supply range is from +2.5V to +5.5V.

Reference Input

The voltage applied at REF sets the full-scale output for both DACs and may range from 2.5V to V_{DD}. The REF input resistance is code dependent, with the lowest value (typically 16kΩ) occurring when both DAC registers are loaded with a code of 01010101 (55 hex). To minimize INL errors, the reference voltage source should have less than 3Ω output impedance.

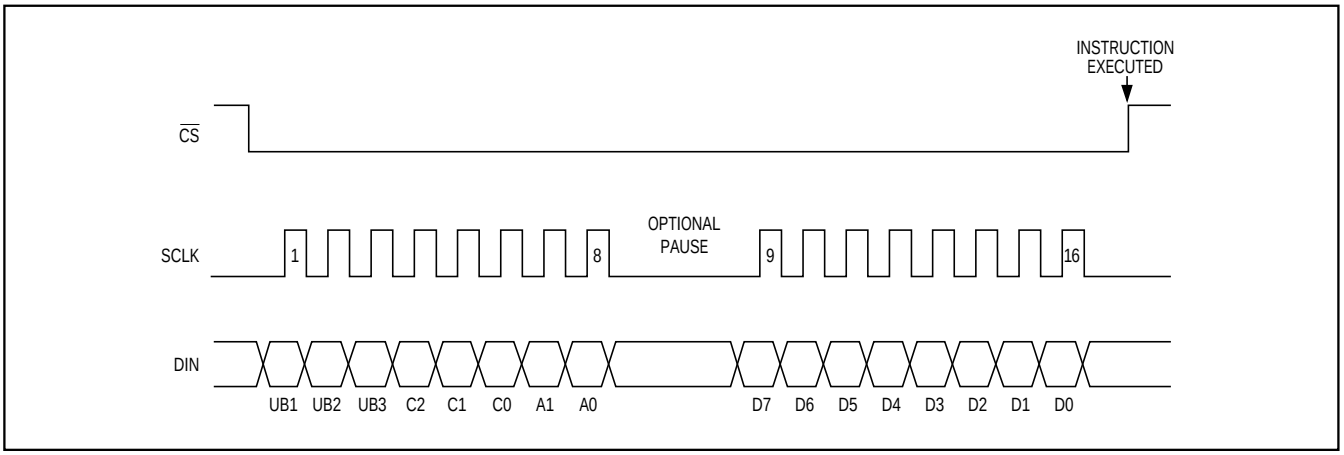

Figure 2. MAX549 Serial-Interface Timing Diagram

DAC Outputs

The MAX549's outputs are unbuffered; each output connects directly to an R-2R ladder. This configuration minimizes power consumption and reduces offset errors. For highest accuracy, apply high resistive loads (1MΩ and up). Lower resistive loads can be driven, but output loading increases full-scale error. The magnitude of the expected error is the ratio of the DAC output resistance to the DC load resistance at the output.

Typically, an energy pulse is coupled into the DAC output on the rising edge of $\overline{CS}$. Since the MAX549's outputs are unbuffered (connected directly to the R-2R ladder), connecting a small capacitor (200pF to 1000pF) from the output to ground creates a lowpass filter that effectively suppresses the pulse for sensitive applications.

Shutdown Mode

When the MAX549 is in shutdown mode, REF becomes high-impedance. The supply current is unchanged, but REF input current decreases to less than 1µA. This allows the system reference to remain active with minimal power consumption.

When exiting shutdown mode, recovery time is equivalent to the DAC settling time.

Serial Interface

The MAX549 interface is compatible with 3-wire SPI™, QSPI™, and Microwire™ microprocessor (µP) interface standards. An active-low chip select ($\overline{CS}$) enables the input shift register to receive data from the serial input (DIN). Data is clocked into the input shift register on rising edges of the serial clock signal (SCLK). The clock frequency can be as high as 10MHz.

Transmit data MSB first in one 16-bit word or two 8-bit bytes. The write cycle can be segmented when $\overline{CS}$ is kept active (low) to allow two 8-bit-wide transfers. After clocking all 16 bits into the input shift register, a rising edge on $\overline{CS}$ programs the DAC. The DAC outputs can be changed independently or simultaneously. The DAC outputs reflect the data stored in the DAC registers.

Initialization

The MAX549 has an internal power-on reset. At power-up, all internal registers are reset to zero; therefore, an initialization write is not necessary.

Serial Input Data Format and Control Codes

The control byte determines which DAC register is updated (Table 1). Table 2 lists the MAX549's serial-input command format. The 16-bit input word consists of an 8-bit control byte and an 8-bit data byte. The 8-bit control byte is not decoded internally; every control bit performs one function. Data is clocked in starting with uncommitted bit 1 (UB1), followed by the remaining control bits and the DAC data byte. The LSB (D0) of the data byte is the last bit clocked into the input shift register (Figure 2).

Table 3 is an example of a 16-bit word. It performs the following functions:

1) Load 80 hex (128 decimal) into both DAC registers
2) Update both DAC outputs on $\overline{CS}$'s rising edge

Table 4 shows how to calculate the output voltage based on the input code. Figure 3 gives detailed timing information.

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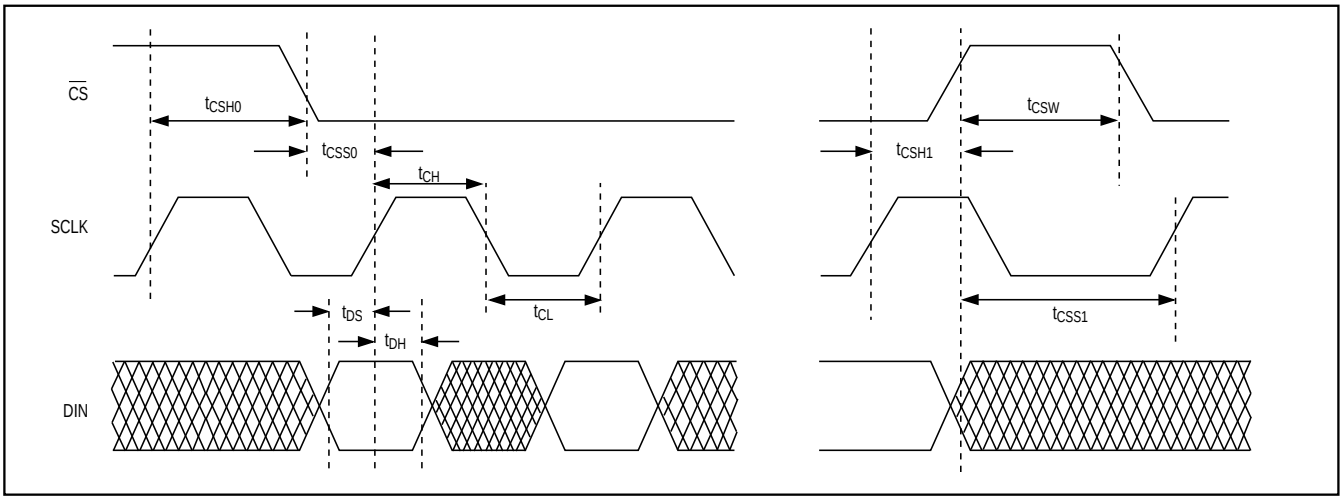

Figure 3. Detailed Serial-Interface Timing Diagram

Table 1. Control Byte/Input Word Bit Definitions

Control Byte	UB1*	X	Unassigned Bit 1
	UB2	X	Unassigned Bit 2
	UB3	X	Unassigned Bit 3
	C2	0	Power-Up Mode
	C2	1	Power-Down Mode
	C1	0	DAC Register Load Operation Disabled
	C1	1	DAC Register Load Operation Enabled
	C0	0	DAC Output Updated on Rising Edge of $\overline{CS}$
	C0	1	Unassigned Operation
	A1	0	Do Not Address DAC B
	A1	1	Address DAC B
	A0	0	Do Not Address DAC A
	A0	1	Address DAC A
Data Byte	D7	X	DAC Data Bit 7 (MSB)
	D6	X	DAC Data Bit 6
	D5	X	DAC Data Bit 5
	D4	X	DAC Data Bit 4
	D3	X	DAC Data Bit 3
	D2	X	DAC Data Bit 2
	D1	X	DAC Data Bit 1
	D0**	X	DAC Data Bit 0 (LSB)

**Clocked in first*
***Clocked in last*

Microprocessor Interfacing

The MAX549 serial interface is compatible with Microwire, SPI, and QSPI interface standards. For SPI, clear the CPOL and CPHA bits (CPOL = 0 and CPHA = 0). CPOL = 0 sets the idle clock state to zero and CPHA = 0 changes data at SCLK's falling edge. This setting allows SPI to run at full clock speeds (1.5MHz). If a serial port is not available on your µP, three bits of a parallel port can be used to emulate a serial port by bit manipulation. Minimize digital feedthrough at the DAC outputs by operating the serial clock only when necessary.

Applications Information

Power-Supply and Ground Considerations

Connect GND to the highest-quality ground available. Bypass V_{DD} with a 0.1µF to 0.22µF capacitor to GND. The reference input can be used without bypassing. However, for optimum line/load-transient response and noise performance, bypass the reference input with 0.1µF to 4.7µF to GND.

Careful PC board layout minimizes crosstalk among the DAC outputs, the reference, and the digital inputs. Separate analog traces by running ground traces between them. Make sure high-frequency digital lines are not routed parallel to analog lines.

Table 2. Serial Interface Programming Commands

CONTROL BYTE								DATA BYTE								COMMAND
Loaded First															Loaded Last	
UB1	UB2	UB3	C2	C1	C0	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Initial condition of all registers after power-up.
X	X	X	0	0	0	X	X	X	X	X	X	X	X	X	X	On $\overline{CS}$'s rising edge, wake up both DACs. DAC registers unchanged.
X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	Unassigned command
X	X	X	0	1	0	0	1	8-bit DAC data								On $\overline{CS}$'s rising edge, load DAC A register. DAC B register unchanged.
X	X	X	0	1	0	1	0	8-bit DAC data								On $\overline{CS}$'s rising edge, load DAC B register. DAC A register unchanged.
X	X	X	0	1	0	1	1	8-bit DAC data								On $\overline{CS}$'s rising edge, load and update both DAC registers.
X	X	X	1	0	0	1	1	X	X	X	X	X	X	X	X	On $\overline{CS}$'s rising edge, power down both DACs. Both DAC outputs go to zero. DAC registers unchanged.
X	X	X	1	1	0	1	1	8-bit DAC data								On $\overline{CS}$'s rising edge, power down both DACs and update both DAC registers. Both DAC outputs go to zero.

X = Don't Care

Table 3. Example Input Word

Loaded First															Loaded Last
UB1	UB2	UB3	C2	C1	C0	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	0	1	0	1	1	1	0	0	0	0	0	0	0

X = Don't Care

Table 4. Analog Output vs. Code

DAC CONTENTS								ANALOG OUTPUT (V)
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	1	1	$+V_{REF}$ x (255/256)
1	0	0	0	0	0	0	1	$+V_{REF}$ x (129/256)
1	0	0	0	0	0	0	0	$+V_{REF}$ x (128/256) = $+V_{REF}/2$
0	1	1	1	1	1	1	1	$+V_{REF}$ x (127/256)
0	0	0	0	0	0	0	1	$+V_{REF}$ x (1/256)
0	0	0	0	0	0	0	0	0

Note: 1LSB = $V_{REF} \times 2^{-8} = V_{REF}(1/256)$
ANALOG OUTPUT = $+V_{REF}(I/256)$, where I = Integer Value of Digital Input

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AC Considerations

Digital Feedthrough

High-speed data at any of the digital input pins may couple through the DAC's internal stray package capacitance and cause noise (digital feedthrough) at the DAC's output, even though $\overline{CS}$ is held high. This digital feedthrough is tested by holding $\overline{CS}$ high and toggling the digital inputs from all 1s to all 0s.

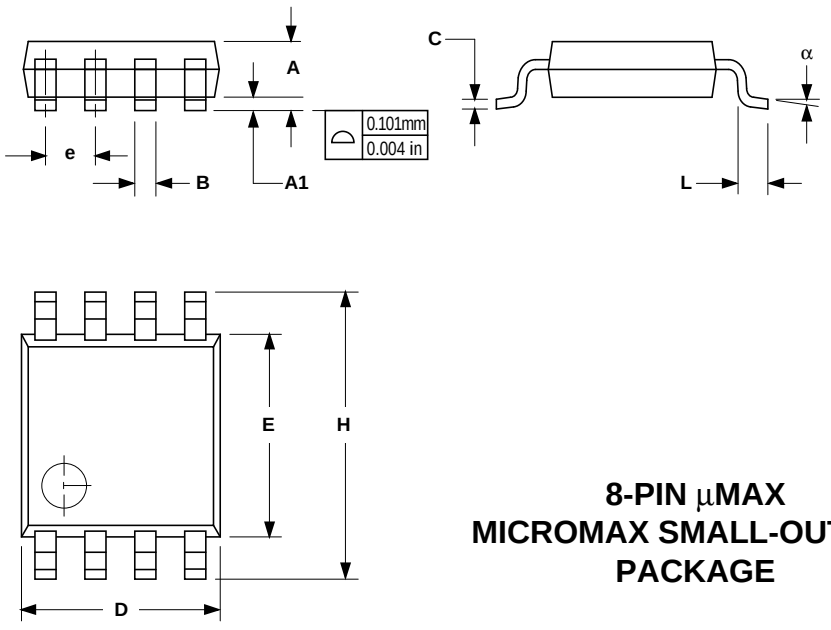
Analog Feedthrough

Due to internal stray capacitance, higher-frequency analog input signals at REF may couple to the output, even when the input digital code is all 0s. Test analog feedthrough by setting all DAC outputs to 0V and sweeping REF.

Chip Information

TRANSISTOR COUNT: 1562

Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
E	0.116	0.120	2.95	3.05
e	0.0256		0.65	
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°

21-0036D

8-PIN µMAX
MICROMAX SMALL-OUTLINE
PACKAGE