SRM2264LCT10/12

CMOS 64K-BIT STATIC RAM

- **Industrial Temperature Range**
- **Low Supply Current**
- **Access Time 100ns/120ns**
- **8,192 Words × 8 Bits, Asynchronous**

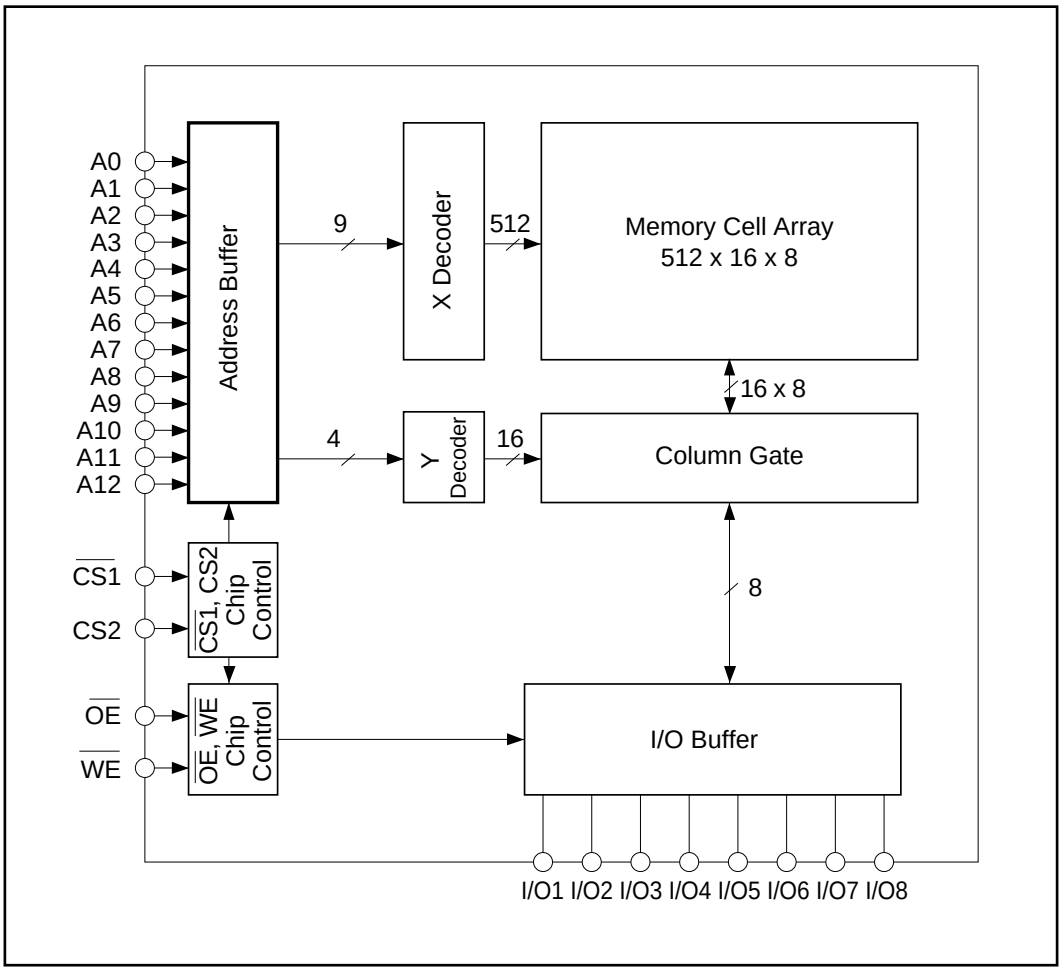
■ DESCRIPTION

The SRM2264LCT10/12 is an 8,192-word × 8-bit asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The –40 to 85°C operating temperature range is good for industrial use. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible, and the three-state output allows easy expansion of memory capacity.

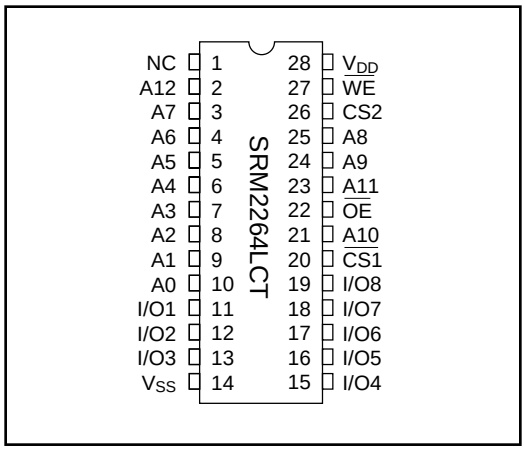
■ FEATURES

- Industrial temperature range . . . . . –40 to 85°C
- Fast access time . . . . . SRM2264LCT10 . . . . . .100ns (Max)
  SRM2264LCT12 . . . . . .120ns (Max)
- Low supply current. . . . . Standby : 0.5µA (Typ)
  Operation : 47mA (Typ) 100ns
  45mA (Typ) 120ns
- Completely static . . . . . No clock required
- Single power supply. . . . . 5V ± 10%
- TTL compatible inputs and outputs
- Three-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package. . . . . SRM2264LCT10/12 . . . . . 28-pin DIP (plastic)
  SRM2264LMT10/12 . . . . . 28-pin SOP (plastic)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

A0 to A12	Address Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS1}$, CS2	Chip Select
I/O1 to 8	Data Input/Output
V_{DD}	Power Supply (+5V)
V_{SS}	Logic Power Supply (0V)
NC	No Connection

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to 7.0	V
Input voltage*	V_I	–0.5 to 7.0	V
Input/output voltage*	$V_{I/O}$	–0.5 to V_{DD} + 0.3	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{OPR}	–40 to 85	°C
Storage temperature	T_{STG}	–65 to 150	°C
Soldering temperature and time	T_{SOL}	260°C, 10s (at lead)	—

*V_I, $V_{I/O}$ (Min) = –3.0V (Pulse width is 50ns)

■ RECOMMENDED DC OPERATING CONDITIONS

(V_{SS} = 0V, T_a = –40 to 85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	3.5	V_{DD} + 0.3	V
	V_{IL}	–0.3*	0	0.8	V

* If pulse width is less than 50ns, it is –1.0V

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, T_a = –40 to 85°C)

Parameter	Symbol	Conditions	SRM2264LCT10			SRM2264LCT12			Unit
			Min	Typ*	Max	Min	Typ*	Max	
Input leakage current	I_{LI}	V_I = 0 to V_{DD}	–1	—	1	–1	—	1	µA
Standby supply current	I_{DDS}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}	—	0.5	1.0	—	0.5	1.0	mA
	I_{DDS1}	$\overline{CS1}$ = CS2 ≥ V_{DD} – 0.2V or CS2 ≤ 0.2V	—	0.5	30	—	0.5	30	µA
Average operating current	I_{DDA}	V_I = V_{IL}, V_{IH} $I_{I/O}$ = 0mA, t_{CYC} = Min	—	47	82	—	45	80	mA
Operating supply current	I_{DDO}	V_I = V_{IL}, V_{IH} $I_{I/O}$ = 0mA	—	35	60	—	35	60	mA
Output leakage	I_{LO}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{DD}	–1	—	1	–1	—	1	µA
High level output voltage	V_{OH}	I_{OH} = –1.0mA	2.4	V_{DD} – 0.1	—	2.4	V_{DD} – 0.1	—	V
Low level output voltage	V_{OL}	I_{OL} = 4.0mA	—	0.2	0.4	—	0.2	0.4	V

* Typical values are measured at T_a = 25°C and V_{DD} = 5.0V

● Terminal Capacitance

(f = 1MHz, T_a = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address capacitance	C_{ADD}	V_{ADD} = 0V	—	3	5	pF
Input capacitance	C_I	V_I = 0V	—	5	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	6	7	pF

● AC Electrical Characteristics

○ Read Cycle

(V_{DD} = 5V ± 10%, V_{SS} = 0V, T_a = –40 to 85°C)

Parameter	Symbol	Conditions	SRM2264LCT10		SRM2264LCT12		Unit
			Min	Max	Min	Max	
Read cycle time	t_{RC}	*1	100	—	120	—	ns
Address access time	t_{ACC}		—	100	—	120	ns
$\overline{CS1}$ access time	t_{ACS1}		—	100	—	120	ns
CS2 access time	t_{ACS2}		—	100	—	120	ns
$\overline{OE}$ access time	t_{OE}		—	50	—	60	ns
$\overline{CS1}$ output set time	t_{CLZ1}	*2	10	—	10	—	ns
$\overline{CS1}$ output floating time	t_{CLZ1}		—	35	—	40	ns
CS2 output set time	t_{CLZ2}		10	—	10	—	ns
CS2 output floating time	t_{CLZ2}		—	35	—	40	ns
$\overline{OE}$ output set time	t_{OLZ}		5	—	5	—	ns
$\overline{OE}$ output floating time	t_{OLZ}		—	35	—	40	ns
Output hold time	t_{OH}	*1	10	—	10	—	ns

○ Write Cycle

(V_{DD} = 5V ± 10%, V_{SS} = 0V, T_a = –40 to 85°C)

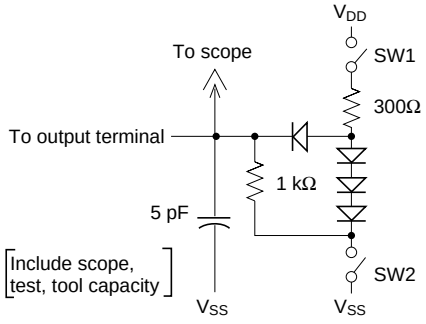
Parameter	Symbol	Conditions	SRM2264LCT10		SRM2264LCT12		Unit
			Min	Max	Min	Max	
Write cycle time	t_{WC}	*1	100	—	120	—	ns
Chip select time 1	t_{CW1}		80	—	85	—	ns
Chip select time 2	t_{CW2}		80	—	85	—	ns
Address enable time	t_{AW}		80	—	85	—	ns
Address setup time	t_{AS}		0	—	0	—	ns
Write pulse width	t_{WP}		60	—	70	—	ns
Address hold time	t_{WR}		0	—	0	—	ns
Input data setup time	t_{DW}		50	—	50	—	ns
Input data hold time	t_{DH}		0	—	0	—	ns
$\overline{WE}$ output floating	t_{WHZ}	*3	—	35	—	40	ns
$\overline{WE}$ output setup time	t_{OW}		5	—	5	—	ns

***1 Read/Write Cycle Test Conditions**

1. Input pulse level: 0.8V to 2.4V
2. $t_r = t_f = 10ns$
3. Input and output timing reference levels: 1.5V
4. Output load $I_{TTL} + C_L = 100pF$

***2 Read Cycle Test Conditions**

1. Input pulse level: 0.8V to 2.4V
2. $t_r = t_f = 10ns$
3. Test Circuit

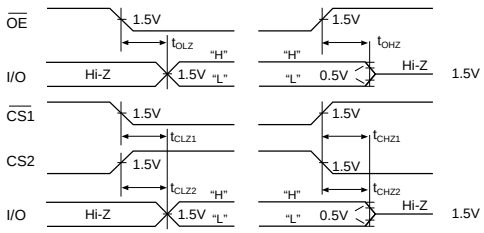


Test: t_{CHZ1}, t_{CHZ2}, t_{OHZ}
Both SW1 and SW2 are closed.

Test: t_{CLZ1}, t_{CLZ2}, t_{OLZ} Hi-Z→"H"
SW1 is open, SW2 is closed.

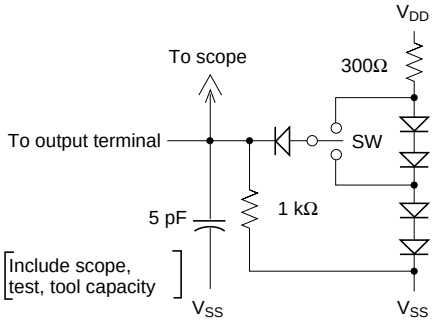
Test: t_{CLZ1}, t_{CLZ2}, t_{OLZ} Hi-Z→"L"
SW1 is closed, SW2 is open.

Output turn-on turn-off times



***3 Write Cycle Test Conditions**

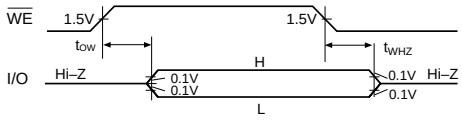
1. Input pulse level: 0.8V to 2.2V
2. $t_r = t_f = 10ns$
3. Test Circuit



Test: t_{OW}, t_{WHZ} Hi-Z→"H" and "H"→Hi-Z
SW is V_{DD} side

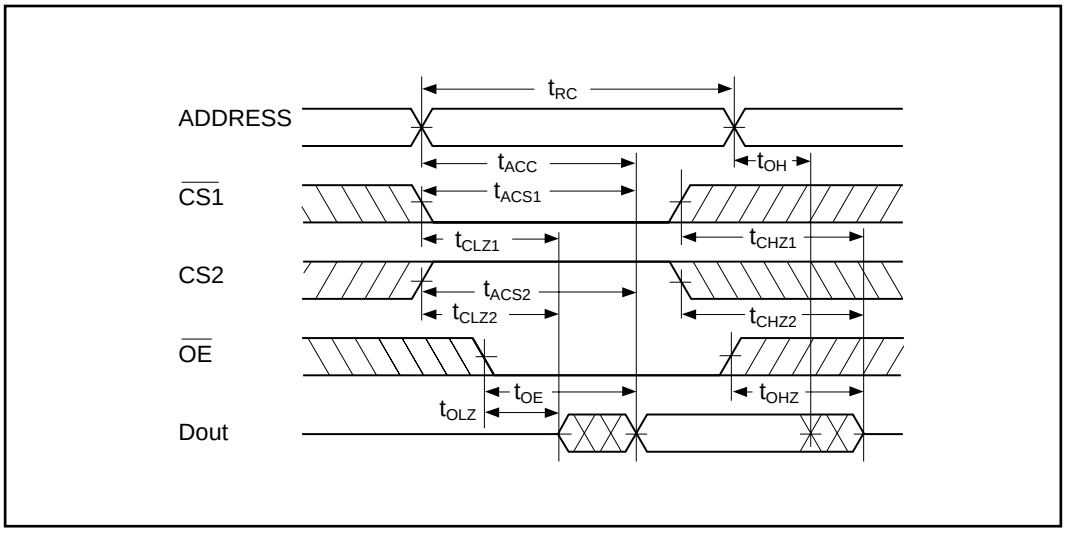
Test: t_{OW}, t_{WHZ} Hi-Z→"L" and "L"→Hi-Z
SW is V_{SS} side

Output turn-on turn-off times



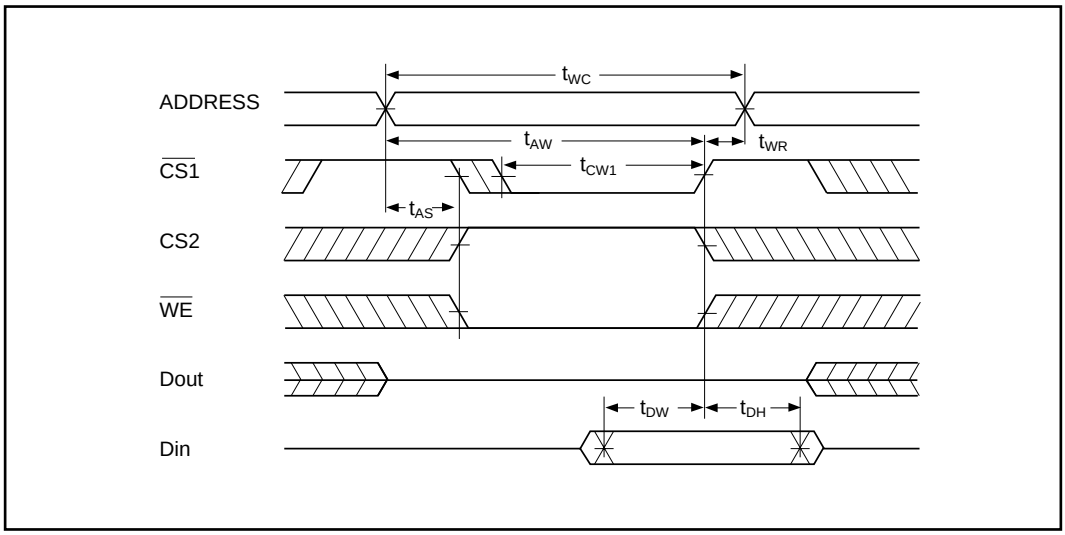
● **Timing Charts**

○ **Read Cycle*1**



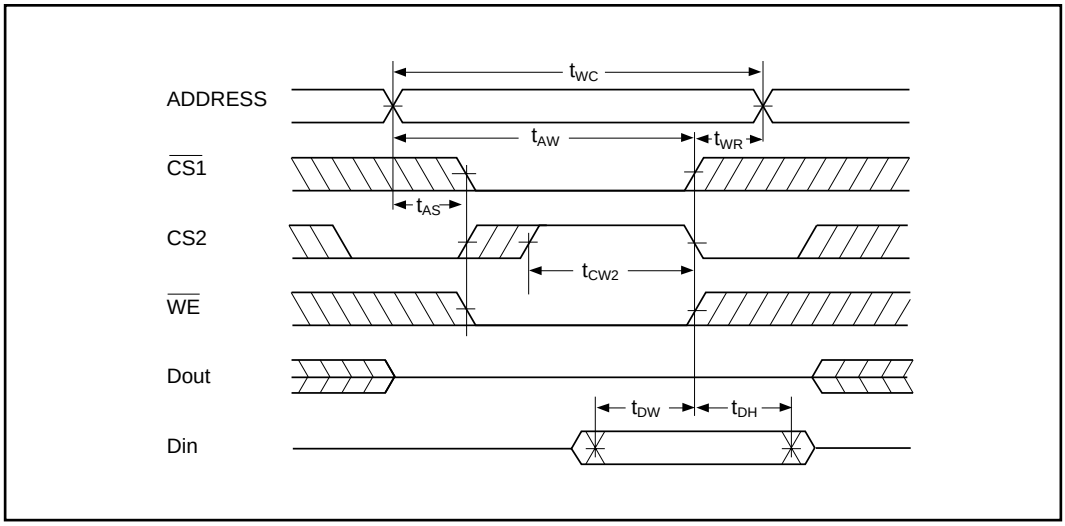
Note: *1. During the read cycle, $\overline{WE}$ must be “H”.

○ **Write Cycle (1) ($\overline{CS1}$ Control)*2**



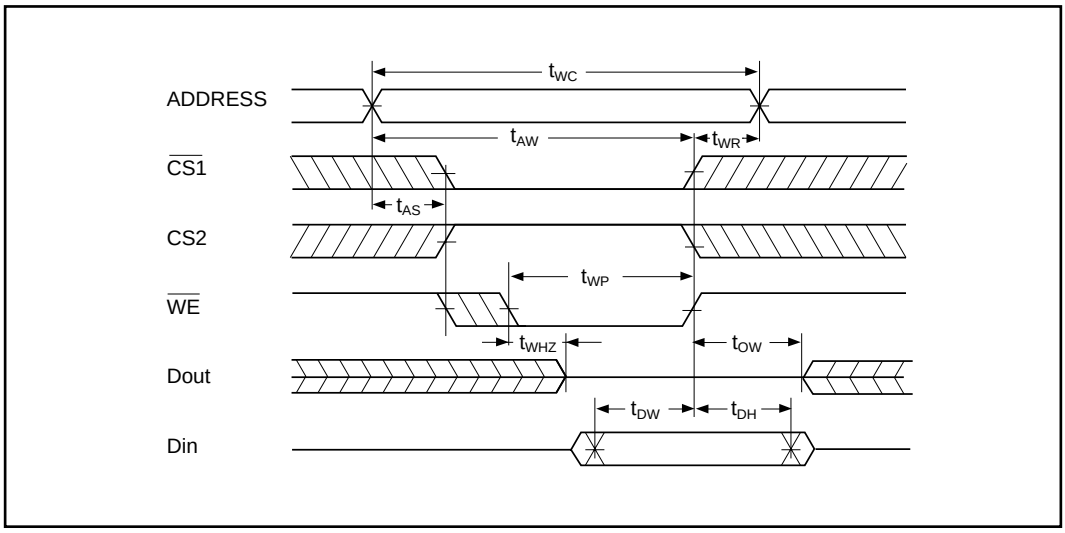
Note: *2. During write cycle (1) and (2), the Output Buffer is in high impedance regardless of the $\overline{OE}$ level.

- **Write Cycle (2) (CS2 Control)*2**



Note: *2. During write cycle (1) and (2), the output buffer is in high impedance regardless of the $\overline{OE}$ level.

- **Write Cycle (3) ($\overline{WE}$ Control)*3**



Note: *3. During write cycle (3), the output buffer is in high impedance if the $\overline{OE}$ level is “H”.

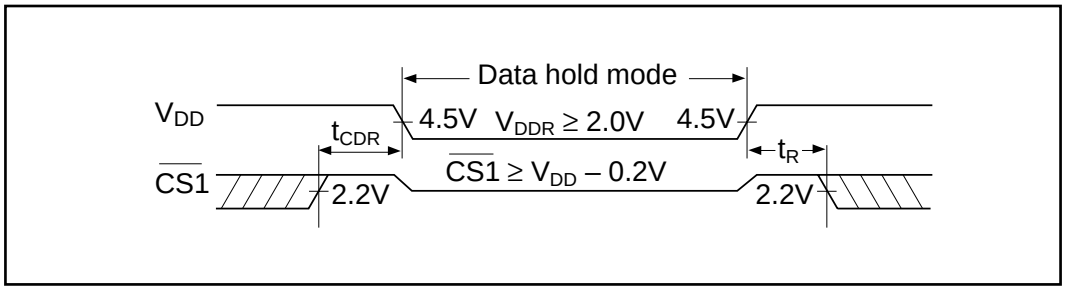
■ DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

(T_a = 0 to 70°C)

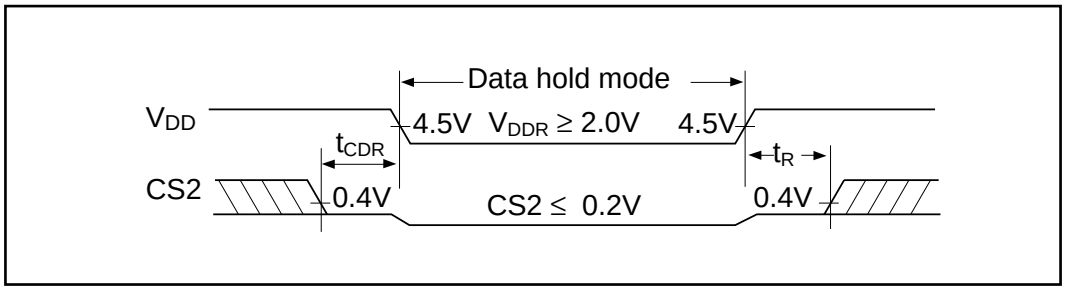
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}		2.0	—	5.5	V
Data retention current	I_{DDR}	V_{DD} = 3V $\overline{CS1}$ = CS2 ≥ V_{DD} – 0.2V or CS2 ≤ 0.2V	—	—	10	µA
Chip select data hold time	t_{CDR}		0	—	—	ns
Operation recovery time	t_R		t_{RC}*	—	—	ns

* t_{RC} = Read Cycle time

● **Data Retention Timing ($\overline{CS1}$ Control)**



● **Data Retention Timing (CS2 Control)**



■ FUNCTIONS

● Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	A0 to A12	Data I/O	Mode	I_{DD}
H	X	—	—	—	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
—	L	—	—	—	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
L	H	X	L	Stable	Input data	Write	I_{DDO}
L	H	L	H	Stable	Output data	Read	I_{DDO}
L	H	H	H	Stable	Hi-Z	Output disable	I_{DDO}

X: "H" or "L"
—: "H", "L", or "Hi-Z"

● Read Data

A read cycle begins with stable address data at the address port (A0 to A12), $\overline{CS1}$ = "L", CS2 = "H", and $\overline{OE}$ = "L". Valid data is available at the data port (I/O1 to I/O8) within 100 or 120ns depending on the device.

● Write Data

There are four ways of writing data into memory (see "Timing Charts", above):

1. Write Cycle (1) — $\overline{CS1}$ control — Write is accomplished by an active $\overline{CS1}$ pulse.
2. Write Cycle (2) — CS2 control — Write is accomplished by an active CS2 pulse.
3. Write Cycle (3) — $\overline{WE}$ control — Write is accomplished by an active $\overline{WE}$ pulse.
4. This method is a combination of the previous write cycles. Beginning with a stable address and all control signals in their non-active states ($\overline{WE}$ = "H", $\overline{CS1}$ = "H" and CS2 = "L"), pulse all three control signals.

The trailing edge of any of the write control signal pulses ($\overline{WE}$, $\overline{CS1}$, CS2) causes data on the data I/O pins to be latched into memory. Data bus contention is avoided since bringing $\overline{CS1}$ and CS2 to their inactive states places the Data I/O pins in a high-impedance state.

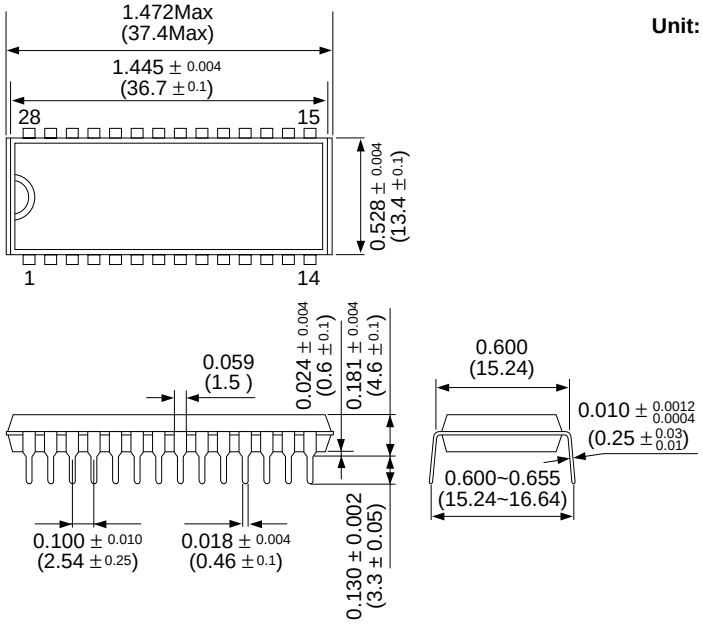
● Standby Mode

When $\overline{CS1}$ and CS2 are in their inactive states, ($\overline{CS1}$ = "H", CS2 = "L"), the SRM2264LCT10/12 is in standby mode. The only operation performed in standby mode is data retention. The data I/O pins are in a high impedance state. All other inputs can be either "H" or "L". This mode is maintained as long as the CS2 level is less than 0.2V and the $\overline{CS1}$ level is greater than V_{DD} – 0.2V. In this condition, the only current flow in the chip is caused by high-resistance paths in memory.

■ PACKAGE DIMENSIONS

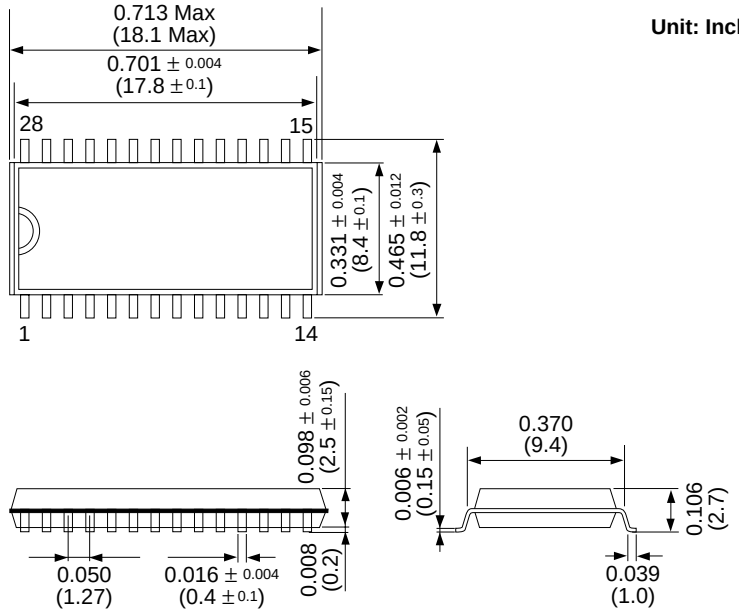
C28 **28-pin DIP**

Unit: Inches (mm)



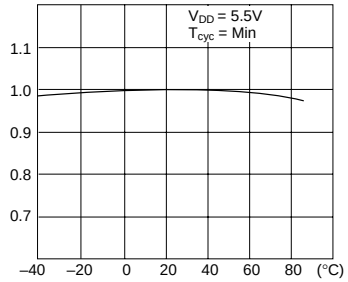
M28-2 **28-pin SOP**

Unit: Inches (mm)

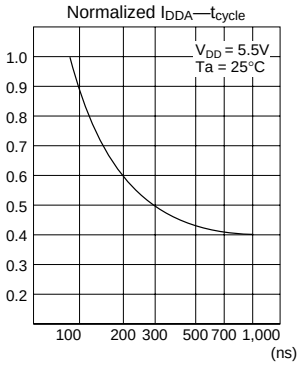


■ CHARACTERISTIC CURVES

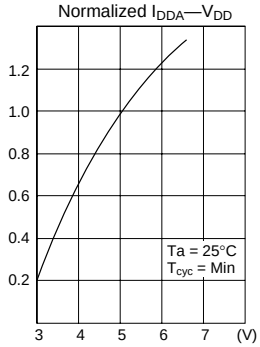
Normalized I_{DDA}—T_a



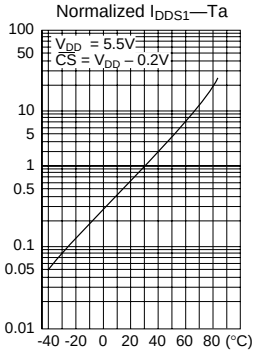
Normalized I_{DDA}—t_{cycle}



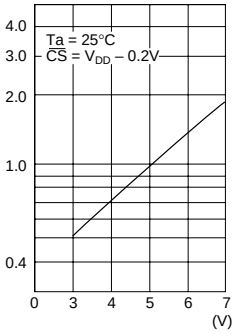
Normalized I_{DDA}—V_{DD}



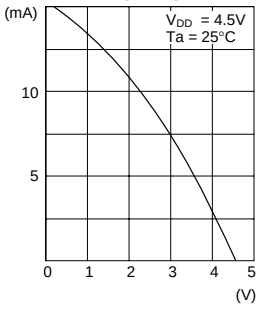
Normalized I_{DDS1}—Ta



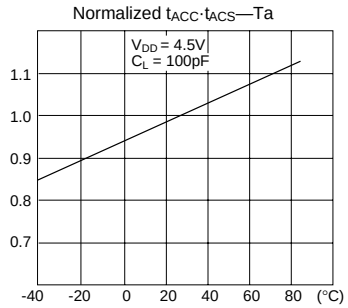
Normalized I_{DDS1}—V_{DD}



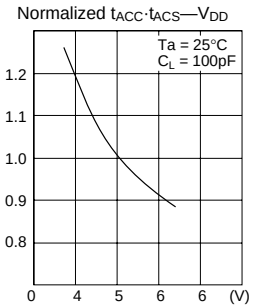
I_{OH}—V_{OH}



Normalized t_{ACC}·t_{ACS}—Ta



Normalized t_{ACC}·t_{ACS}—V_{DD}



I_{OL}—V_{OL}