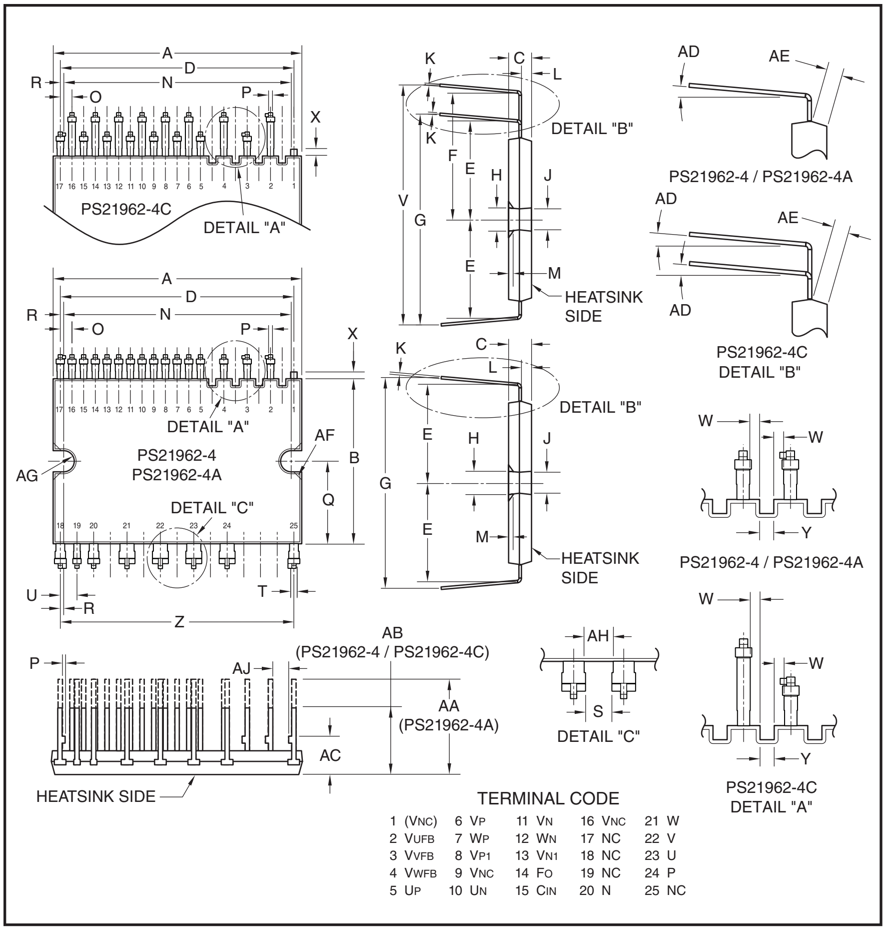
Powerex, Inc., 173 Pavilion Lane, Youngwood, Pennsylvania 15697-1800 (724) 925-7272

# Intellimod™ Module

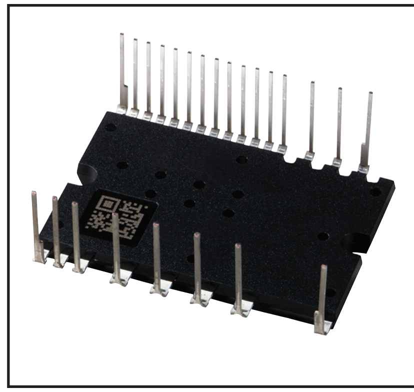
**Dual-In-Line Intelligent Power Module**
**5 Amperes/600 Volts**




**Outline Drawing and Circuit Diagram**

| Dimensions | Inches | Millimeters |
|---|---|---|
| A | 1.50±0.02 | 38.0±0.5 |
| B | 0.94±0.02 | 24.0±0.5 |
| C | 0.14 | 3.5 |
| D | 1.40 | 35.56 |
| E | 0.57±0.02 | 14.4±0.5 |
| F | 0.74±0.02 | 18.9±0.5 |
| G | 1.15±0.02 | 29.2±0.5 |
| H | 0.14 | 3.5 |
| J | 0.13 | 3.3 |
| K | 0.016 | 0.4 |
| L | 0.06±0.02 | 1.5±0.05 |
| M | 0.031 | 0.8 |
| N | 1.39±0.019 | 35.0±0.3 |
| O | 0.07±0.008 | 1.778±0.2 |
| P | 0.02 | 0.5 |
| Q | 0.47 | 12.0 |
| R | 0.011 | 0.28 |

| Dimensions | Inches | Millimeters |
|---|---|---|
| S | 0.12 | 2.8 |
| T | 0.024 | 0.6 |
| U | 0.1±0.008 | 2.54±0.2 |
| V | 1.33±0.02 | 33.7±0.5 |
| W | 0.03 | 0.678 |
| X | 0.04 | 1.0 |
| Y | 0.05 | 1.2 |
| Z | 1.40 | 35.56 |
| AA | 0.55±0.02 | 14.0±0.5 |
| AB | 0.37±0.02 | 9.5±0.5 |
| AC | 0.22±0.02 | 5.5±0.5 |
| AD | 0 ~ 5° | 0 ~ 5° |
| AE | 0.06 Min. | 1.5 Min. |
| AF | 0.05 | 1.2 |
| AG | 0.063 Rad. | 1.6 Rad. |
| AH | 0.118 Min. | 3.0 Min. |
| AJ | 0.098 Min. | 2.5 Min. |



## Description:

DIP-IPMs are intelligent power modules that integrate power devices, drivers, and protection circuitry in an ultra compact dual-in-line transfer-mold package for use in driving small three phase motors. Use of 5th generation IGBTs, DIP packaging, and application specific HVICs allow the designer to reduce inverter size and overall design time.

## Features:

- ☐ Compact Packages
- ☐ Single Power Supply
- ☐ Integrated HVICs
- ☐ Direct Connection to CPU
- ☐ Reduced $R_{th}$

## Applications:

- ☐ Refrigerators
- ☐ Air Conditioners
- ☐ Small Servo Motors
- ☐ Small Motor Control

## Ordering Information:

PS21962-4 is a 600V, 5 Ampere short pin DIP Intelligent Power Module.

PS21962-4A – long pin type
PS21962-4C – zigzag pin type

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*PS21962-4, PS21962-4A, PS21962-4C*
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*5 Amperes/600 Volts*

## Absolute Maximum Ratings, $T_j$ = 25°C unless otherwise specified

| Characteristics | Symbol | PS21962-4, PS21962-4A PS21962-4C | Units |
|---|---|---|---|
| Power Device Junction Temperature* | $T_j$ | -20 to 150 | °C |
| Storage Temperature | $T_{stg}$ | -40 to 125 | °C |
| Case Operating Temperature (Note 1) | $T_C$ | -20 to 100 | °C |
| Mounting Torque, M3 Mounting Screws | — | 6 | in-lb |
| Module Weight (Typical) | — | 10 | Grams |
| Heatsink Flatness (Note 2) | — | -50 to 100 | µm |
| Self-protection Supply Voltage Limit (Short Circuit Protection Capability)** | $V_{CC(prot.)}$ | 400 | Volts |
| Isolation Voltage, AC 1 minute, 60Hz Sinusoidal, Connection Pins to Heatsink Plate | $V_{ISO}$ | 1500 | Volts |

*The ma ximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C (@$T_C \leq$ 100°C). However, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to $T_{j(avg)} \leq$125°C (@$T_C \leq$ 100°C).
**$V_D$ = 13.5 ~ 16.5V, Inverter Part, $T_j$ = 125°C, Non-repetitive, Less than 2µs

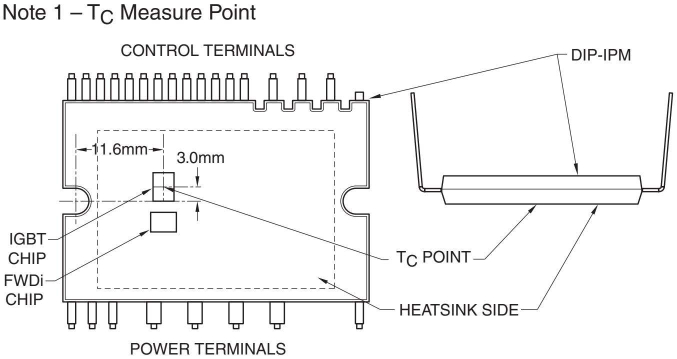
## IGBT Inverter Sector

| | | | |
|---|---|---|---|
| Collector-Emitter Voltage | $V_{CES}$ | 600 | Volts |
| Each Collector Current, ± ($T_C$ = 25°C) | $I_C$ | 5 | Amperes |
| Each Peak Collector Current, ± ($T_C$ = 25°C, Less than 1ms) | $I_{CP}$ | 10 | Amperes |
| Supply Voltage (Applied between P - N) | $V_{CC}$ | 450 | Volts |
| Supply Voltage, Surge (Applied between P - N) | $V_{CC(surge)}$ | 500 | Volts |
| Collector Dissipation ($T_C$ = 25°C, per 1 Chip) | $P_C$ | 21.3 | Watts |

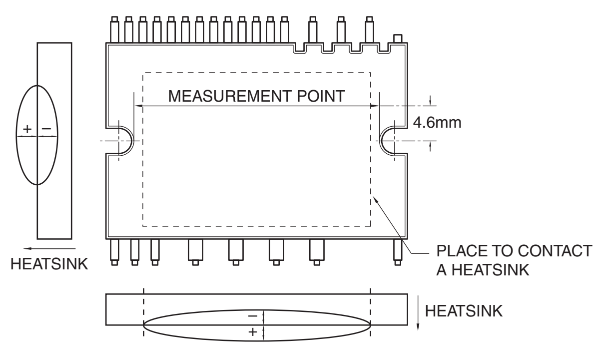
## Control Sector

| | | | |
|---|---|---|---|
| Supply Voltage (Applied between $V_{P1}$-$V_{NC}$, $V_{N1}$-$V_{NC}$) | $V_D$ | 20 | Volts |
| Supply Voltage (Applied between $V_{UFB}$-U, $V_{VFB}$-V, $V_{WFB}$-W) | $V_{DB}$ | 20 | Volts |
| Input Voltage (Applied between $U_P$, $V_P$, $W_P$-$V_{NC}$, $U_N$, $V_N$, $W_N$-$V_{NC}$) | $V_{IN}$ | -0.5 ~ $V_D$+0.5 | Volts |
| Fault Output Supply Voltage (Applied between $F_O$-$V_{NC}$) | $V_{FO}$ | -0.5 ~ $V_D$+0.5 | Volts |
| Fault Output Current (Sink Current at $F_O$ Terminal) | $I_{FO}$ | 1 | mA |
| Current Sensing Input Voltage (Applied between $C_{IN}$-$V_{NC}$) | $V_{SC}$ | -0.5 ~ $V_D$+0.5 | Volts |

Note 1 – $T_C$ Measure Point




Note 2 – Flatness Measurement Position



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## Electrical and Mechanical Characteristics, $T_j$ = 25°C unless otherwise specified

### IGBT Inverter Sector

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Collector-Emitter Saturation Voltage | $V_{CE(sat)}$ | $V_D = V_{DB}$ = 15V, $I_C$ = 5A, $V_{IN}$ = 5V, $T_j$ = 25°C | — | 1.70 | 2.20 | Volts |
| | | $V_D = V_{DB}$ = 15V, $I_C$ = 5A, $V_{IN}$ = 5V, $T_j$ = 125°C | — | 1.80 | 2.30 | Volts |
| Diode Forward Voltage | $V_{EC}$ | $-I_C$ = 5A, $V_{IN}$ = 0V | — | 1.70 | 2.20 | Volts |
| Inductive Load Switching Times | $t_{on}$ | $V_{CC}$ = 300V, $V_D = V_{DB}$ = 15V, $I_C$ = 5A, $T_j$ = 125°C, $V_{IN}$ = 0 ⇔ 5V, Inductive Load, | 0.50 | 1.00 | 1.60 | µs |
| | $t_{rr}$ | | — | 0.30 | — | µs |
| | $t_{C(on)}$ | | — | 0.30 | 0.50 | µs |
| | $t_{off}$ | | — | 1.40 | 2.00 | µs |
| | $t_{C(off)}$ | | — | 0.50 | 0.80 | µs |
| Collector Cutoff Current | $I_{CES}$ | $V_{CE} = V_{CES}$, $T_j$ = 25°C | — | — | 1.0 | mA |
| | | $V_{CE} = V_{CES}$, $T_j$ = 125°C | — | — | 10 | mA |

### Control Sector

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Circuit Current $I_D$ | $V_{IN}$ = 5V | Total of $V_{P1}$-$V_{NC}$, $V_{N1}$-$V_{NC}$ | — | — | 2.80 | mA |
| $V_D = V_{DB}$ = 15V | | $V_{UFB}$-U, $V_{VFB}$-V, $V_{WFB}$-W | — | — | 0.55 | mA |
| | $V_{IN}$ = 0V | Total of $V_{P1}$-$V_{NC}$, $V_{N1}$-$V_{NC}$ | — | — | 2.80 | mA |
| | | $V_{UFB}$-U, $V_{VFB}$-V, $V_{WFB}$-W | — | — | 0.55 | mA |
| Fault Output Voltage | $V_{FOH}$ | $V_{SC}$ = 0V, $F_O$ Terminal Pull-up to 5V by 10kΩ | 4.9 | — | — | Volts |
| | $V_{FOL}$ | $V_{SC}$ = 1V, $I_{FO}$ = 1mA | — | — | 0.95 | Volts |
| Input Current | $I_{IN}$ | $V_{IN}$ = 5V | 0.70 | 1.00 | 1.50 | mA |
| Short Circuit Trip Level* | $V_{SC(ref)}$ | $V_D$ = 15V* | 0.43 | 0.48 | 0.53 | Volts |
| Supply Circuit Under-voltage | $UV_{DBt}$ | Trip Level, $T_j$ ≤ 125°C | 10.0 | — | 12.0 | Volts |
| | $UV_{DBr}$ | Reset Level, $T_j$ ≤ 125°C | 10.5 | — | 12.5 | Volts |
| | $UV_{Dt}$ | Trip Level, $T_j$ ≤ 125°C | 10.3 | — | 12.5 | Volts |
| | $UV_{Dr}$ | Reset Level, $T_j$ ≤ 125°C | 10.8 | — | 13.0 | Volts |
| Fault Output Pulse Width** | $t_{FO}$ | | 20 | — | — | µs |
| ON Threshold Voltage | $V_{th(on)}$ | Applied between $U_P$, $V_P$, $W_P$-$V_{NC}$, $U_N$, $V_N$, $W_N$-$V_{NC}$ | — | 2.1 | 2.6 | Volts |
| OFF Threshold Voltage | $V_{th(off)}$ | | 0.8 | 1.3 | — | Volts |
| ON/OFF Threshold Hysteresis Voltage | $V_{th(hys)}$ | | 0.35 | 0.65 | — | Volts |

* Short Circuit protection is functioning only for the low-arms. Please select the value of the external shunt resistor such that the $S_C$ trip level is less than 1.7 times the current rating.
**Fault signal is asserted only for a $U_V$ or $S_C$ condition on the low side. On a $S_C$ fault the $F_O$ duration will be 20µsec. On a $U_V$ condition the fault signal will be asserted as long as the $U_V$ condition exists or for 20µsec, whichever is longer.

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## Thermal Characteristics

| Characteristic | Symbol | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Junction to Case | $R_{th(j-c)Q}$ | Inverter IGBT (Per 1/6 Module) | — | — | 4.7 | °C/Watt |
| | $R_{th(j-c)D}$ | Inverter FWDi (Per 1/6 Module) | — | — | 5.4 | °C/Watt |

## Recommended Conditions for Use

| Characteristic | Symbol | Condition | Min. | Typ. | Value | Units |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | Applied between P-N Terminals | 0 | 300 | 400 | Volts |
| Control Supply Voltage | $V_D$ | Applied between $V_{P1}$-$V_{NC}$, $V_{N1}$-$V_{NC}$ | 13.5 | 15.0 | 16.5 | Volts |
| | $V_{DB}$ | Applied between $V_{UFB}$-U, $V_{VFB}$-V, $V_{WFB}$-W | 13.0 | 15.0 | 18.5 | Volts |
| Control Supply Variation | $dV_D$, $dV_{DB}$ | | -1 | — | 1 | V/µs |
| Arm Shoot-through Blocking Time | $t_{DEAD}$ | For Each Input Signal, $T_C \leq 100°C$ | 1.5 | — | — | µs |
| Allowable Minimum Input Pulse Width* | $P_{WIN(on)}$ | | 0.5 | — | — | µs |
| | $P_{WIN(off)}$ | | 0.5 | — | — | µs |
| $V_{NC}$ Voltage Variation | $V_{NC}$ | Between $V_{NC}$-N (Including Surge) | -5.0 | — | 5.0 | Volts |

*DIP-IPM might not make response or work properly if the input signal plus width is less than the recommended minimum value.

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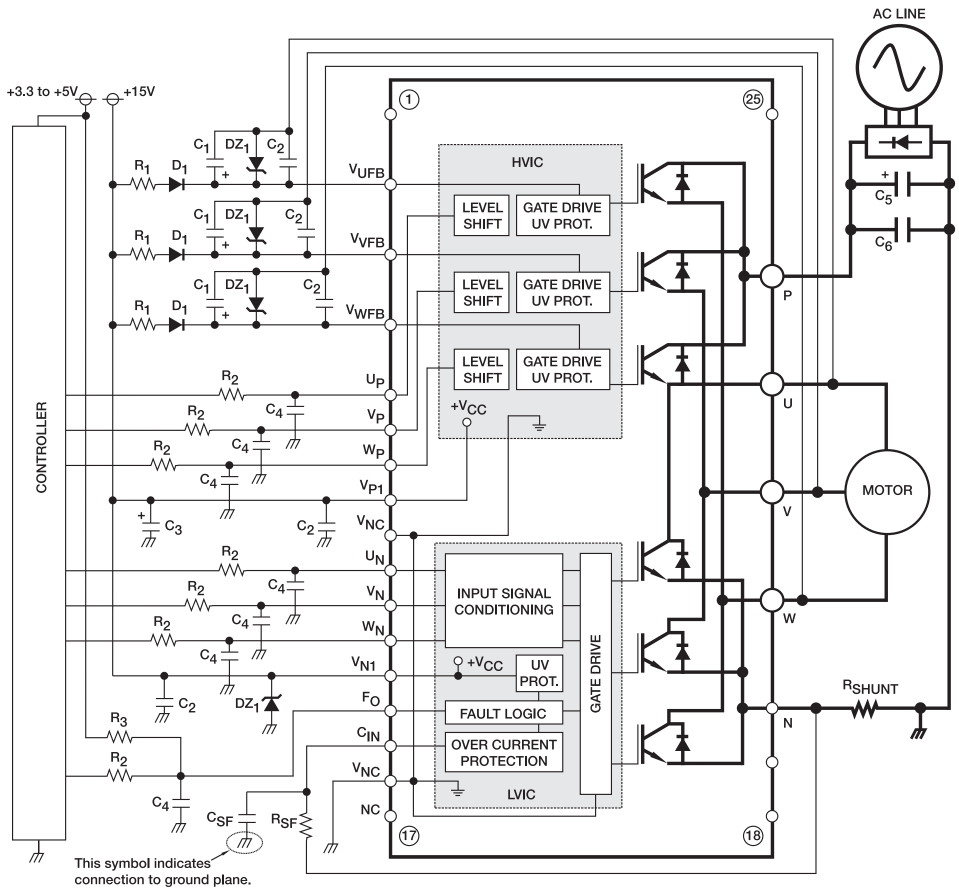
## Application Circuit




Component Selection:

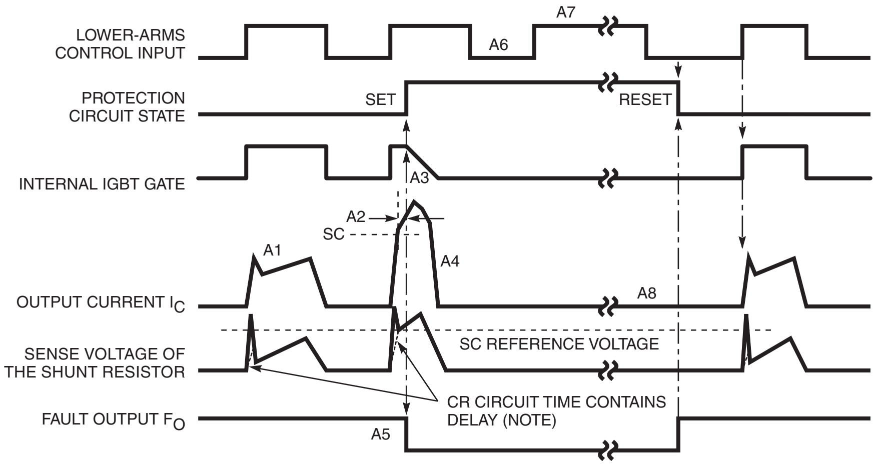
| Dsgn. | Typ. Value | Description |
|---|---|---|
| $D_1$ | 1A, 600V | Boot strap supply diode – Ultra fast recovery |
| $DZ_1$ | 24V, 1.0W | Control and boot strap supply over voltage suppression |
| $C_1$ | 10-100uF, 50V | Boot strap supply reservoir – Electrolytic, long life, low Impedance, 105°C (Note 5) |
| $C_2$ | 0.22-2.0uF, 50V | Local decoupling/High frequency noise filters – Multilayer ceramic (Note 8) |
| $C_3$ | 10-100uF, 50V | Control power supply filter – Electrolytic, long life, low Impedance, 105°C |
| $C_4$ | 100pF, 50V | Optional Input signal noise filter – Multilayer ceramic (Note 1) |
| $C_5$ | 200-2000uF, 450V | Main DC bus filter capacitor – Electrolytic, long life, high ripple current, 105°C |
| $C_6$ | 0.1-0.22uF, 450V | Surge voltage suppression capacitor – Polyester/Polypropylene film (Note 9) |
| $C_{SF}$ | 1000pF, 50V | Short circuit detection filter capacitor – Multilayer Ceramic (Note 6, Note 7) |
| $R_{SF}$ | 1.8k ohm | Short circuit detection filter resistor (Note 6, Note 7) |
| $R_{SHUNT}$ | 5-100mohm | Current sensing resistor – Non-inductive, temperature stable, tight tolerance (Note 10) |
| $R_1$ | 10 ohm | Boot strap supply inrush limiting resistor (Note 5) |
| $R_2$ | 330 ohm | Optional control input noise filter (Note 1, Note 2) |
| $R_3$ | 10k ohm | Fault output signal pull-up resistor (Note 3) |

Notes:

1) To prevent input signal oscillations minimize wiring length to controller (~2cm). Additional RC filtering (C5 etc.) may be required. If filtering is added be careful to maintain proper dead time and voltage levels. See application notes for details.
2) Internal HVIC provides high voltage level shifting allowing direct connection of all six driving signals to the controller.
3) $F_O$ output is an open collector type. Pull up resistor (R3) should be adjusted to current sink capability of the controller.
4) Use only one $V_{NC}$ Pin (either 9 or 16) and leave the other open.
5) Boot strap supply component values must be adjusted depending on the PWM frequency and technique.
6) Wiring length associated with $R_{SHUNT}$, $R_{SF}$, $C_{SF}$ must be minimized to avoid improper operation of the OC function.
7) $R_{SF}$, $C_{SF}$ set over current protection trip time. Recommend time constant is 1.5μs-2.0μs. See application notes.
8) Local decoupling/high frequency filter capacitors must be connected as close as possible to the modules pins.
9) The length of the DC link wiring between C5, C6, the DIP's P terminal and the shunt must be minimized to prevent excessive transient voltages. In particular C6 should be mounted as close to the DIP as possible.
10) Use high quality, tight tolerance current sensing resistor. Connect resistor as close as possible to the DIP's N terminal. Be careful to check for proper power rating. See application notes for calculation of resistance value.

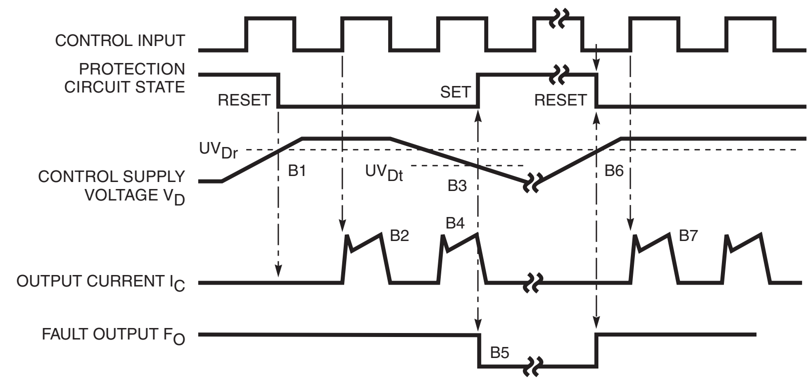
## Protection Function Timing Diagrams

Short-Circuit Protection (Lower-arms only with the external shunt resistor and RC filter)




A1: Normal operation – IGBT turn on and conducting current.
A2: Short-circuit current detected (SC trigger).
A3: IGBT gate hard interrupted.
A4: IGBT turn off.
A5: $F_O$ output with a fixed pulse width of $t_{FO(min)}$ = 20μs.
A6: Input "L" – IGBT off.
A7: Input "H" – IGBT on is blocked during the $F_O$ output period.
A8: IGBT stays in off state.

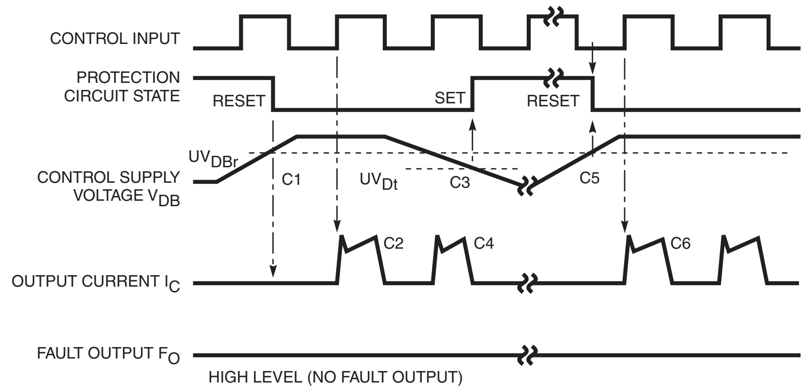
Under-Voltage Protection (Lower-side, $UV_D$)




B1: Control supply voltage rise – After the voltage level reaches $UV_{Dr}$, the drive circuit begins to work at the rising edge of the next input signal.
B2 : Normal operation – IGBT turn on and conducting current.
B3: Under-voltage trip ($UV_{Dt}$).
B4: IGBT turn off regardless of the control input level.
B5: $F_O$ output during under-voltage period, however, the minimum pulse width is 20μs.
B6: Under-voltage reset ($UV_{Dr}$).
B7: Normal operation – IGBT turn on and conducting current.

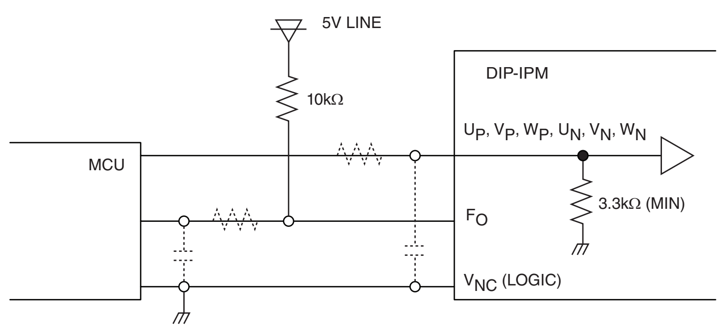
## Protection Function Timing Diagrams

Under-Voltage Protection (Upper-side, $UV_{DB}$)



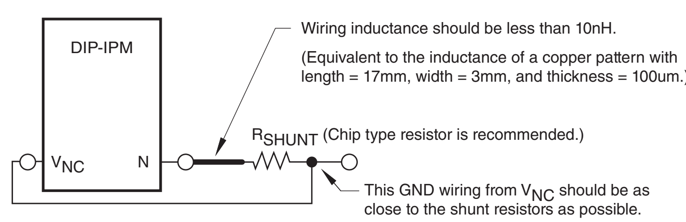

C1: Control supply voltage rises – After the voltage level reaches $UV_{DBr}$, the drive circuit begins to work at the rising edge of the next input signal.
C2: Normal operation – IGBT turn on and conducting current.
C3: Under-voltage trip ($UV_{DBt}$).
C4: IGBT stays off regardless of the control input level, but there is no $F_O$ signal output.
C5: Under-voltage reset ($UV_{Dr}$).
C6: Normal operation – IGBT turn on and conducting current.

## Typical Interface Circuit




NOTE: RC coupling at each input (parts shown dotted) may change depending on the PWM control scheme used in the application and the wiring impedance of the printed circuit board. The DIP-IPM input signal section integrates a 3.3kΩ (min) pull-down resistor. Therefore, when using an external filtering resistor, care must be taken to satisfy the turn-on threshold voltage requirement.

## Wiring Method Around Shunt Resistor



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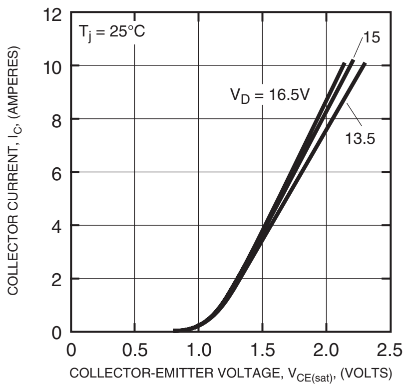
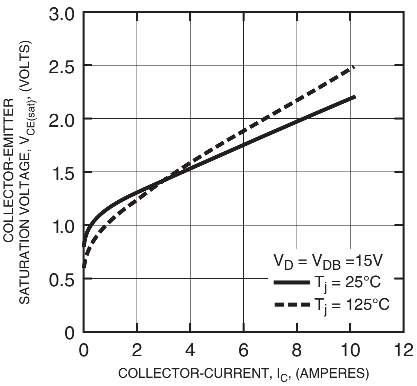
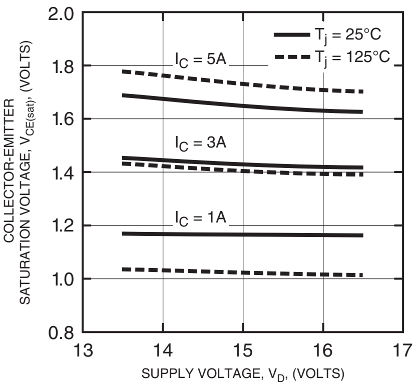
**OUTPUT CHARACTERISTICS**
**(TYPICAL - INVERTER PART)**



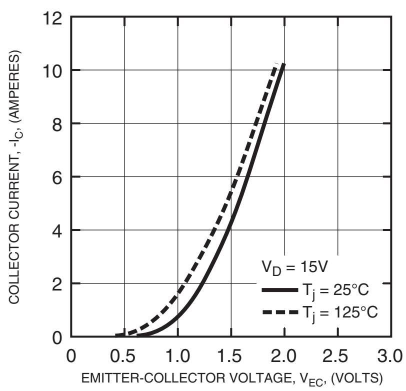

**COLLECTOR-EMITTER**
**SATURATION VOLTAGE CHARACTERISTICS**
**(TYPICAL - INVERTER PART)**



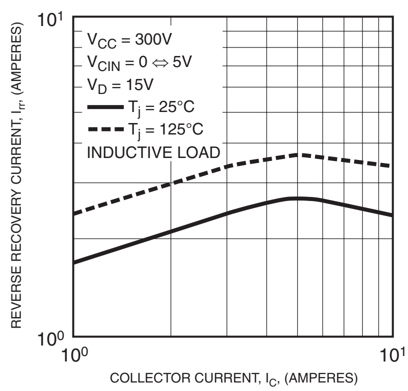

**COLLECTOR-EMITTER SATURATION VOLTAGE**
**VS. SUPPLY VOLTAGE CHARACTERISTICS**
**(TYPICAL - INVERTER PART)**



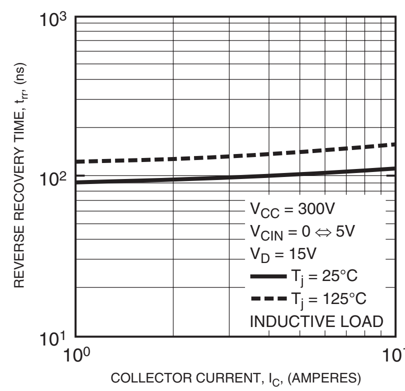

**FREE-WHEEL DIODE**
**FORWARD CHARACTERISTICS**
**(TYPICAL - INVERTER PART)**



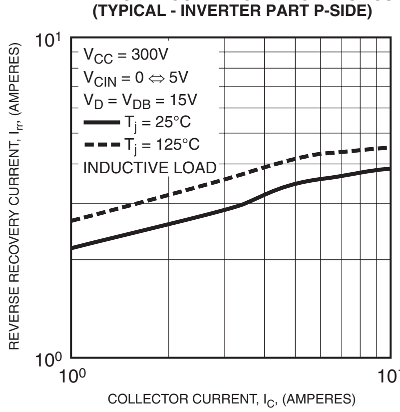

**REVERSE RECOVERY CHARACTERISTICS**
**(TYPICAL - INVERTER PART N-SIDE)**



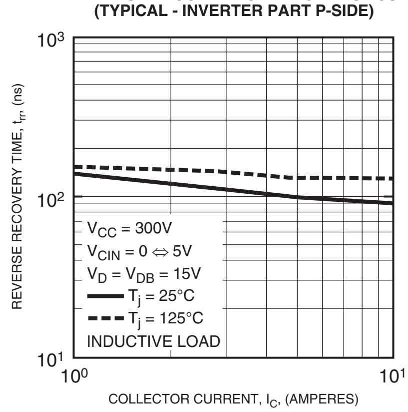

**REVERSE RECOVERY CHARACTERISTICS**
**(TYPICAL - INVERTER PART N-SIDE)**



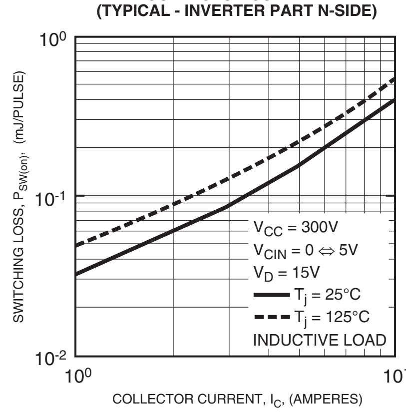

**REVERSE RECOVERY CHARACTERISTICS**
**(TYPICAL - INVERTER PART P-SIDE)**




**REVERSE RECOVERY CHARACTERISTICS**
**(TYPICAL - INVERTER PART P-SIDE)**




**SWITCHING LOSS (ON) VS.**
**COLLECTOR CURRENT**
**(TYPICAL - INVERTER PART N-SIDE)**



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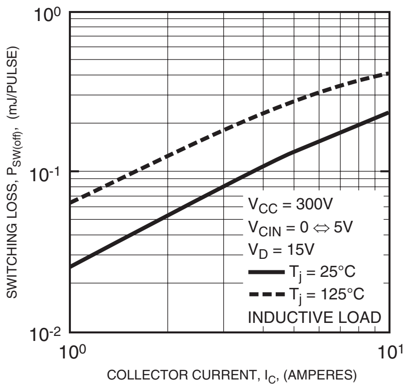
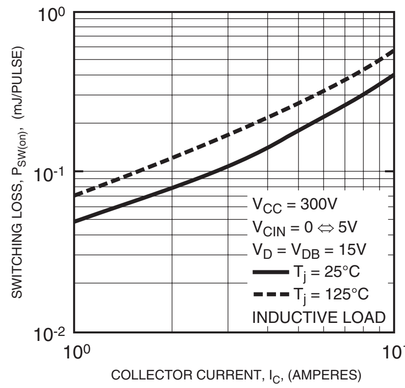
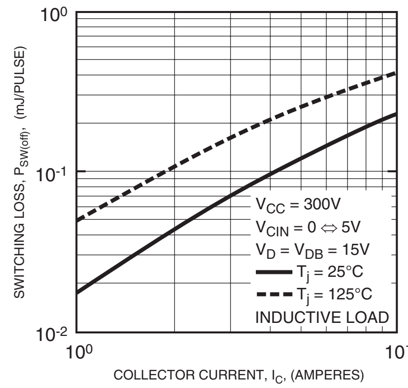
**SWITCHING LOSS (OFF) VS. COLLECTOR CURRENT (TYPICAL - INVERTER PART N-SIDE)**



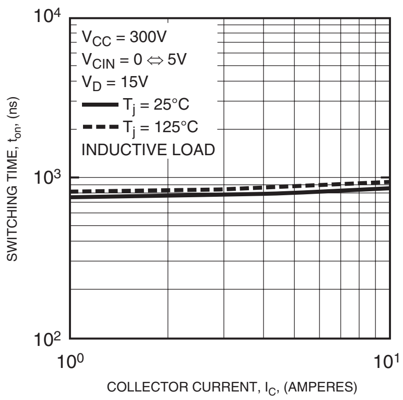

**SWITCHING LOSS (ON) VS. COLLECTOR CURRENT (TYPICAL - INVERTER PART P-SIDE)**



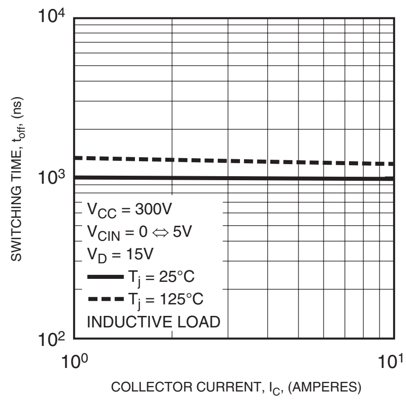

**SWITCHING LOSS (OFF) VS. COLLECTOR CURRENT (TYPICAL - INVERTER PART P-SIDE)**



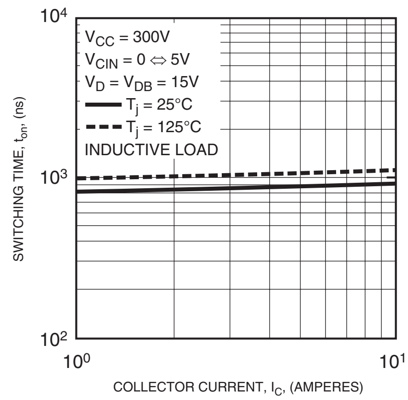

**SWITCHING TIME (ON) VS. COLLECTOR CURRENT (TYPICAL - INVERTER PART N-SIDE)**



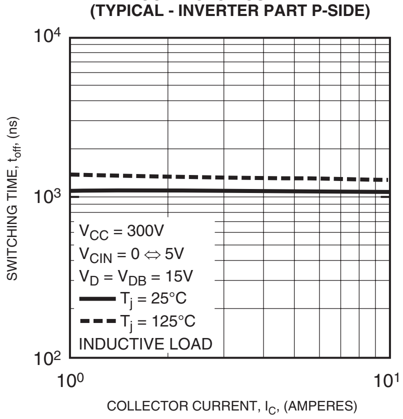

**SWITCHING TIME (OFF) VS. COLLECTOR CURRENT (TYPICAL - INVERTER PART N-SIDE)**



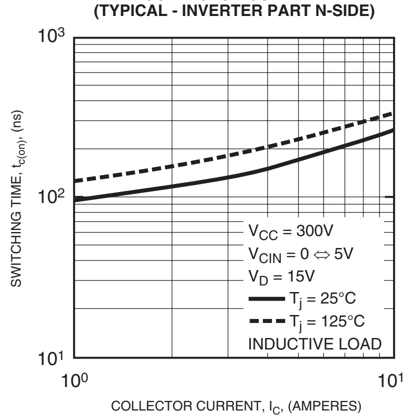

**SWITCHING TIME (ON) VS. COLLECTOR CURRENT (TYPICAL - INVERTER PART P-SIDE)**



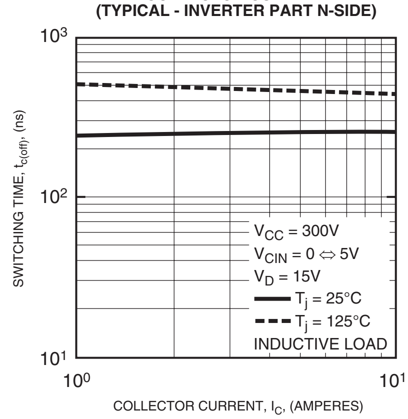

**SWITCHING TIME (OFF) VS. COLLECTOR CURRENT (TYPICAL - INVERTER PART P-SIDE)**




**SWITCHING TIME (ON) VS. COLLECTOR CURRENT (TYPICAL - INVERTER PART N-SIDE)**




**SWITCHING TIME (OFF) VS. COLLECTOR CURRENT (TYPICAL - INVERTER PART N-SIDE)**



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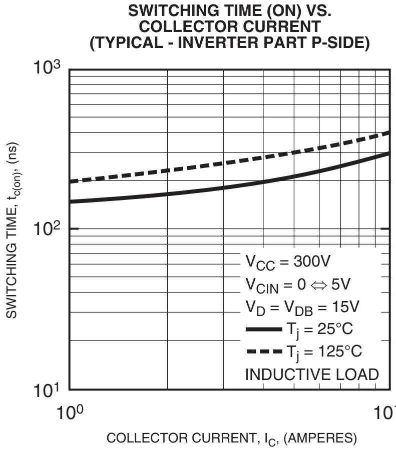
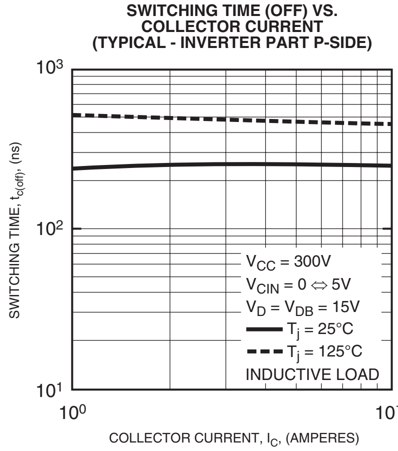
*PS21962-4, PS21962-4A, PS21962-4C*
*Intellimod™ Module*
*Dual-In-Line Intelligent Power Module*
*5 Amperes/600 Volts*



# PS21962-4/-4A/-4C/-4W

**TRANSFER-MOLD TYPE**
**INSULATED TYPE**

**PS21962-4**

### INTEGRATED POWER FUNCTIONS

600V/5A low-loss 5th generation IGBT inverter bridge for three phase DC-to-AC power conversion

### INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

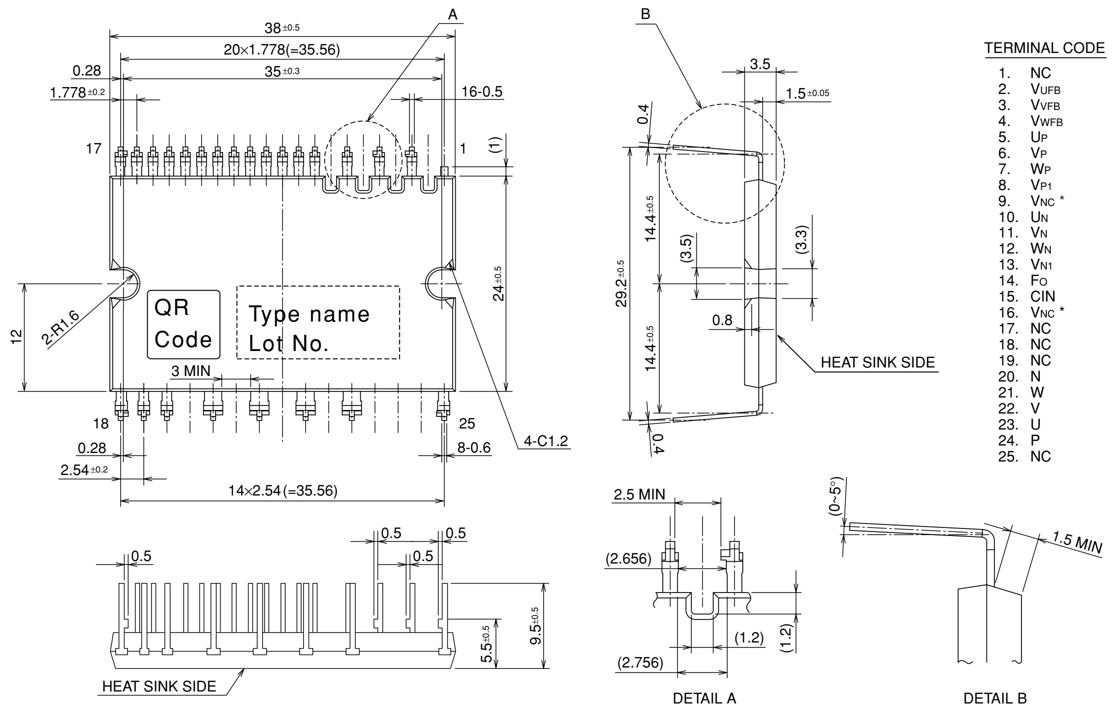
- For upper-leg IGBTS :Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection.
- For lower-leg IGBTS : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling : Corresponding to an SC fault (Lower-leg IGBT) or a UV fault (Lower-side supply).
- Input interface : 3V, 5V line (High Active).
- UL Approved : Yellow Card No. E80276

## APPLICATION

AC100V~200V three-phase inverter drive for small power motor control.

**Fig. 1 PACKAGE OUTLINES (PS21962-4)**

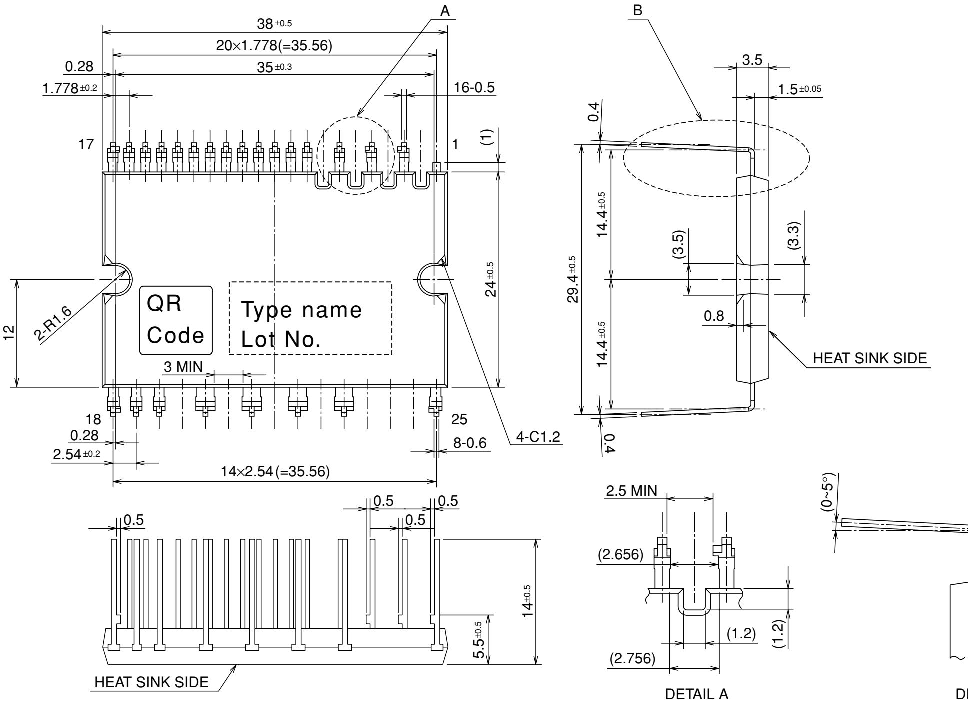
Dimensions in mm




*) Two VNC terminals (9 & 16 pin) are connected inside DIP-IPM, please connect either one to the 15V power supply GND outside and leave another one open.

**Fig. 2 LONG TERMINAL TYPE PACKAGE OUTLINES (PS21962-4A)**

Dimensions in mm

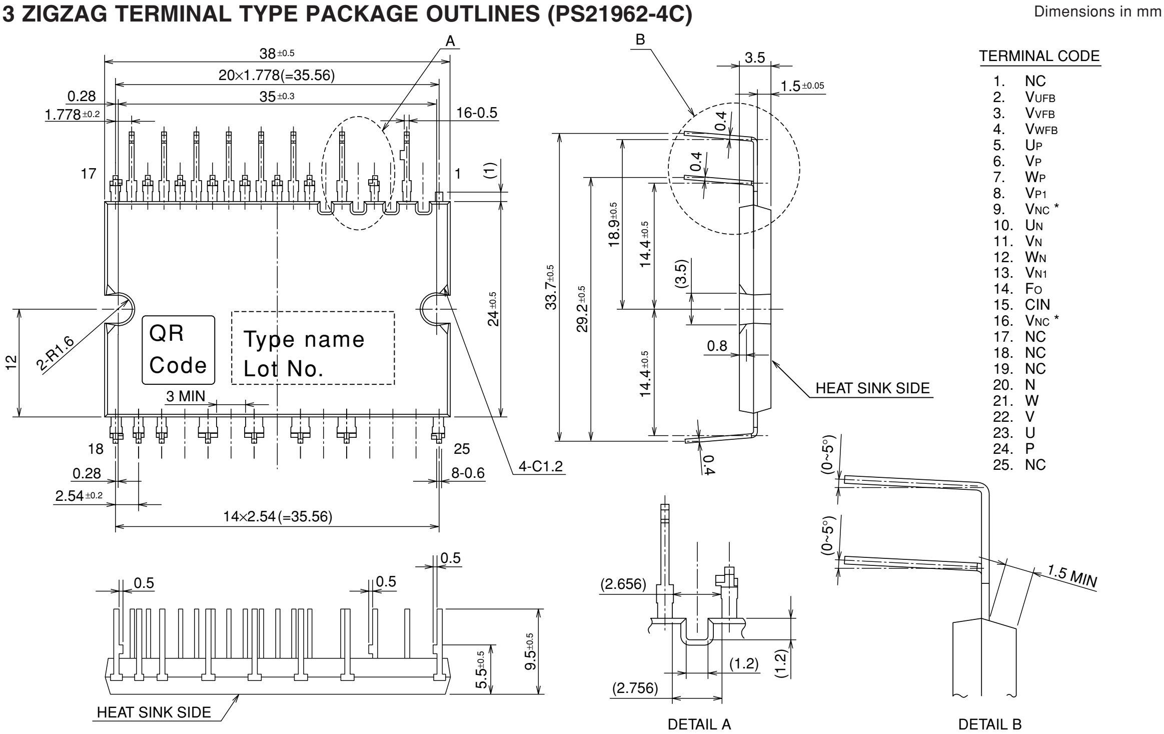



TERMINAL CODE
1. NC
2. $V_{UFB}$
3. $V_{VFB}$
4. $V_{WFB}$
5. $U_P$
6. $V_P$
7. $W_P$
8. $V_{P1}$
9. $V_{NC}$ *
10. $U_N$
11. $V_N$
12. $W_N$
13. $V_{N1}$
14. $F_O$
15. CIN
16. $V_{NC}$ *
17. NC
18. NC
19. NC
20. N
21. W
22. V
23. U
24. P
25. NC

*) Two $V_{NC}$ terminals (9 & 16 pin) are connected inside DIP-IPM, please connect either one to the 15V power supply GND outside and leave another one open.

**Fig. 3 ZIGZAG TERMINAL TYPE PACKAGE OUTLINES (PS21962-4C)**

Dimensions in mm

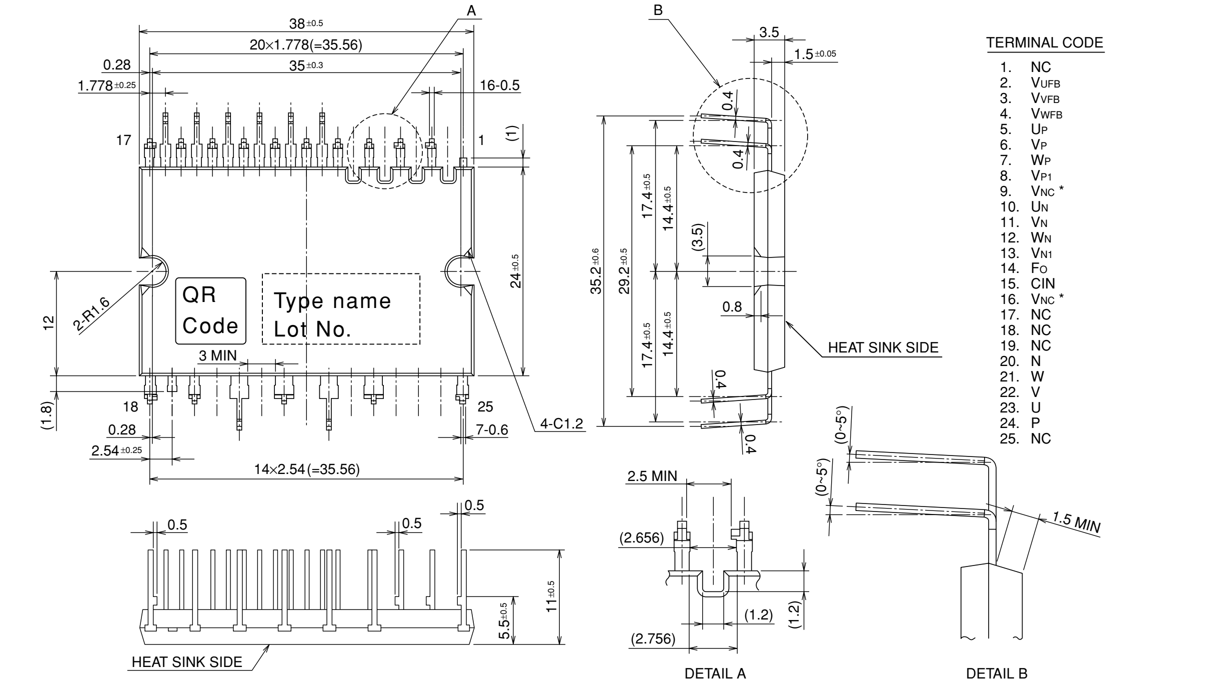



TERMINAL CODE
1. NC
2. $V_{UFB}$
3. $V_{VFB}$
4. $V_{WFB}$
5. $U_P$
6. $V_P$
7. $W_P$
8. $V_{P1}$
9. $V_{NC}$ *
10. $U_N$
11. $V_N$
12. $W_N$
13. $V_{N1}$
14. $F_O$
15. CIN
16. $V_{NC}$ *
17. NC
18. NC
19. NC
20. N
21. W
22. V
23. U
24. P
25. NC

*) Two $V_{NC}$ terminals (9 & 16 pin) are connected inside DIP-IPM, please connect either one to the 15V power supply GND outside and leave another one open.

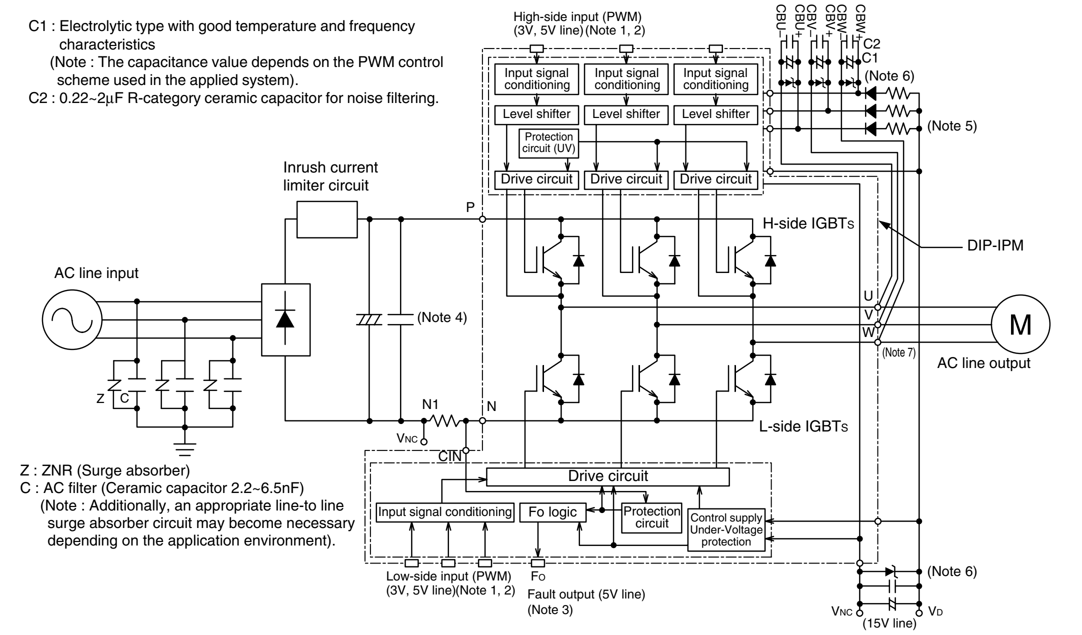
## Fig. 4 BOTH SIDES ZIGZAG TERMINAL TYPE PACKAGE OUTLINES (PS21962-4W)

Dimensions in mm




*) Two VNC terminals (9 & 16 pin) are connected inside DIP-IPM, please connect either one to the 15V power supply GND outside and leave another one open.

## Fig. 5 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)




**Note1:** Input logic is high-active. There is a 3.3kΩ (min) pull-down resistor built-in each input circuit. When using an external CR filter, please make it satisfy the input threshold voltage.

**2:** By virtue of integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler or transformer isolation is possible. (see also Fig. 11)

**3:** This output is open drain type. The signal line should be pulled up to the positive side of the 5V power supply with approximately 10kΩ resistor. (see also Fig. 11)

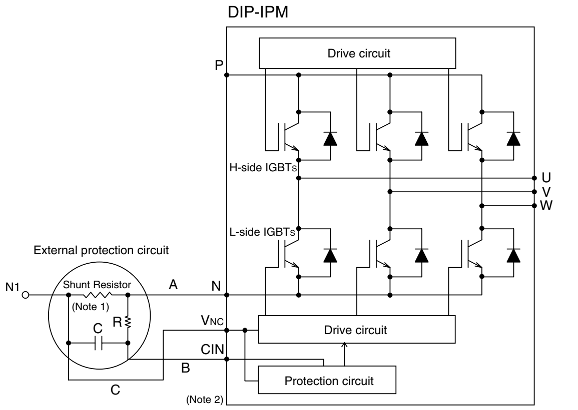
**4:** The wiring between the power DC link capacitor and the P, N1 terminals should be as short as possible to protect the DIP-IPM against catastrophic high surge voltages. For extra precaution, a small film type snubber capacitor (0.1~0.22µF, high voltage type) is recommended to be mounted close to these P & N1 DC power input pins.

**5:** High voltage (600V or more) and fast recovery type (less than 100ns) diodes should be used in the bootstrap circuit.

**6:** It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.

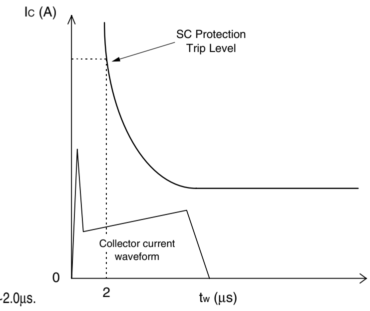
**7:** Bootstrap negative electrodes should be connected to U, V, W terminals directly and separated from the main output wires.

**Fig. 6 EXTERNAL PART OF THE DIP-IPM PROTECTION CIRCUIT**




**Note1:** In the recommended external protection circuit, please select the RC time constant in the range 1.5~2.0μs.
**2:** To prevent erroneous protection operation, the wiring of A, B, C should be as short as possible.

Short Circuit Protective Function (SC) :
SC protection is achieved by sensing the L-side DC-Bus current (through the external shunt resistor) after allowing a suitable filtering time (defined by the RC circuit).
When the sensed shunt voltage exceeds the SC trip-level, all the L-side IGBTs are turned OFF and a fault signal (Fo) is output. Since the SC fault may be repetitive, it is recommended to stop the system when the Fo signal is received and check the fault.




**MAXIMUM RATINGS** ($T_j$ = 25°C, unless otherwise noted)

**INVERTER PART**

| Symbol | Parameter | Condition | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Applied between P-N | 450 | V |
| $V_{CC(surge)}$ | Supply voltage (surge) | Applied between P-N | 500 | V |
| $V_{CES}$ | Collector-emitter voltage | | 600 | V |
| $\pm I_C$ | Each IGBT collector current | $T_C$ = 25°C | 5 | A |
| $\pm I_{CP}$ | Each IGBT collector current (peak) | $T_C$ = 25°C, less than 1ms | 10 | A |
| $P_C$ | Collector dissipation | $T_C$ = 25°C, per 1 chip | 21.3 | W |
| $T_j$ | Junction temperature | (Note 1) | –20~+125 | °C |

**Note 1 :** The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C (@ $T_C \le$ 100°C). However, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to $T_{j(ave)} \le$ 125°C (@ $T_C \le$ 100°C).

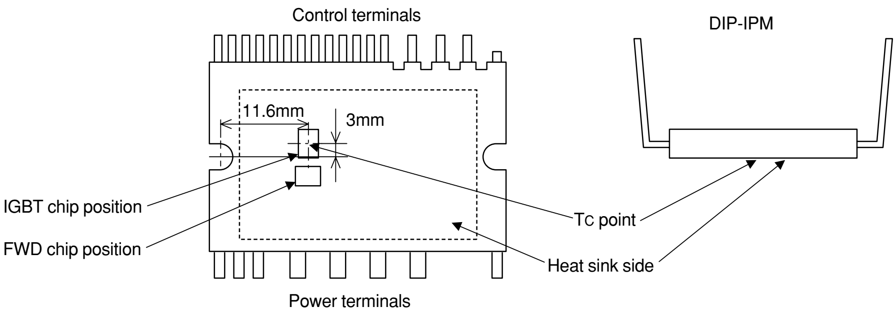
**CONTROL (PROTECTION) PART**

| Symbol | Parameter | Condition | Ratings | Unit |
|---|---|---|---|---|
| $V_D$ | Control supply voltage | Applied between $V_{P1}$-$V_{NC}$, $V_{N1}$-$V_{NC}$ | 20 | V |
| $V_{DB}$ | Control supply voltage | Applied between $V_{UFB}$-U, $V_{VFB}$-V, $V_{WFB}$-W | 20 | V |
| $V_{IN}$ | Input voltage | Applied between $U_P$, $V_P$, $W_P$, $U_N$, $V_N$, $W_N$-$V_{NC}$ | –0.5~$V_D$+0.5 | V |
| $V_{FO}$ | Fault output supply voltage | Applied between $F_O$-$V_{NC}$ | –0.5~$V_D$+0.5 | V |
| $I_{FO}$ | Fault output current | Sink current at $F_O$ terminal | 1 | mA |
| $V_{SC}$ | Current sensing input voltage | Applied between CIN-$V_{NC}$ | –0.5~$V_D$+0.5 | V |

## TOTAL SYSTEM

| Symbol | Parameter | Condition | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC(PROT)}$ | Self protection supply voltage limit (short circuit protection capability) | $V_D$ = 13.5~16.5V, Inverter part<br>$T_j$ = 125°C, non-repetitive, less than 2µs | 400 | V |
| $T_C$ | Module case operation temperature | (Note 2) | –20~+100 | °C |
| $T_{stg}$ | Storage temperature | | –40~+125 | °C |
| $V_{iso}$ | Isolation voltage | 60Hz, Sinusoidal, 1 minute,<br>Between pins and heat-sink plate | 1500 | $V_{rms}$ |

**Note 2:** $T_C$ measurement point




## THERMAL RESISTANCE

| Symbol | Parameter | Condition | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $R_{th(j-c)Q}$ | Junction to case thermal resistance (Note 3) | Inverter IGBT part (per 1/6 module) | — | — | 4.7 | °C/W |
| $R_{th(j-c)F}$ | | Inverter FWD part (per 1/6 module) | — | — | 5.4 | °C/W |

**Note 3 :** Grease with good thermal conductivity should be applied evenly with about +100µm~+200µm on the contacting surface of DIP-IPM and heat-sink.
The contacting thermal resistance between DIP-IPM case and heat sink ($R_{th(c-f)}$) is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ (per 1/6 module) is about 0.3°C/W when the grease thickness is 20µm and the thermal conductivity is 1.0W/m·k.

## ELECTRICAL CHARACTERISTICS ($T_j$ = 25°C, unless otherwise noted)

## INVERTER PART

| Symbol | Parameter | Condition | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | $V_D$ = $V_{DB}$ = 15V | $I_C$ = 5A, $T_j$ = 25°C | — | 1.70 | 2.20 | V |
| | | $V_{IN}$ = 5V | $I_C$ = 5A, $T_j$ = 125°C | — | 1.80 | 2.30 | |
| $V_{EC}$ | FWD forward voltage | $T_j$ = 25°C, $-I_C$ = 5A, $V_{IN}$ = 0V | | — | 1.70 | 2.20 | V |
| $t_{on}$ | Switching times | $V_{CC}$ = 300V, $V_D$ = $V_{DB}$ = 15V<br>$I_C$ = 5A, $T_j$ = 125°C, $V_{IN}$ = 0 ↔ 5V<br>Inductive load (upper-lower arm) | | 0.50 | 1.00 | 1.60 | µs |
| $t_{rr}$ | | | | — | 0.30 | — | µs |
| $t_{c(on)}$ | | | | — | 0.30 | 0.50 | µs |
| $t_{off}$ | | | | — | 1.40 | 2.00 | µs |
| $t_{c(off)}$ | | | | — | 0.50 | 0.80 | µs |
| $I_{CES}$ | Collector-emitter cut-off current | $V_{CE}$ = $V_{CES}$ | $T_j$ = 25°C | — | — | 1 | mA |
| | | | $T_j$ = 125°C | — | — | 10 | |

### CONTROL (PROTECTION) PART

| Symbol | Parameter | Condition | | Limits Min. | Limits Typ. | Limits Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_D$ | Circuit current | $V_D = V_{DB} = 15V$, $V_{IN} = 5V$ | Total of $V_{P1}$-$V_{NC}$, $V_{N1}$-$V_{NC}$ | — | — | 2.80 | mA |
| | | | $V_{UFB}$-U, $V_{VFB}$-V, $V_{WFB}$-W | — | — | 0.55 | mA |
| | | $V_D = V_{DB} = 15V$, $V_{IN} = 0V$ | Total of $V_{P1}$-$V_{NC}$, $V_{N1}$-$V_{NC}$ | — | — | 2.80 | mA |
| | | | $V_{UFB}$-U, $V_{VFB}$-V, $V_{WFB}$-W | — | — | 0.55 | mA |
| $V_{FOH}$ | Fault output voltage | $V_{SC} = 0V$, FO terminal pull-up to 5V by 10kΩ | | 4.9 | — | — | V |
| $V_{FOL}$ | | $V_{SC} = 1V$, $I_{FO} = 1mA$ | | — | — | 0.95 | V |
| $V_{SC(ref)}$ | Short circuit trip level | $T_j = 25°C$, $V_D = 15V$ (Note 4) | | 0.43 | 0.48 | 0.53 | V |
| $I_{IN}$ | Input current | $V_{IN} = 5V$ | | 0.70 | 1.00 | 1.50 | mA |
| $UV_{DBt}$ | Control supply under-voltage protection | $T_j \leq 125°C$ | Trip level | 10.0 | — | 12.0 | V |
| $UV_{DBr}$ | | | Reset level | 10.5 | — | 12.5 | V |
| $UV_{Dt}$ | | | Trip level | 10.3 | — | 12.5 | V |
| $UV_{Dr}$ | | | Reset level | 10.8 | — | 13.0 | V |
| $t_{FO}$ | Fault output pulse width | (Note 5) | | 20 | — | — | µs |
| $V_{th(on)}$ | ON threshold voltage | Applied between $U_P$, $V_P$, $W_P$, $U_N$, $V_N$, $W_N$-$V_{NC}$ | | — | 2.1 | 2.6 | V |
| $V_{th(off)}$ | OFF threshold voltage | | | 0.8 | 1.3 | — | V |
| $V_{th(hys)}$ | ON/OFF threshold hysteresis voltage | | | 0.35 | 0.65 | — | V |

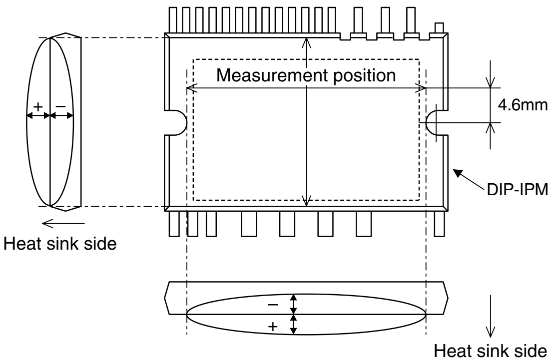
**Note 4 :** Short circuit protection is functioning only for the lower-arms. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.
**5 :** Fault signal is asserted corresponding to a short circuit or lower side control supply under-voltage failure.

### MECHANICAL CHARACTERISTICS AND RATINGS

| Parameter | Condition | | Limits Min. | Limits Typ. | Limits Max. | Unit |
|---|---|---|---|---|---|---|
| Mounting torque | Mounting screw : M3 (Note 6) | Recommended : 0.69 N·m | 0.59 | — | 0.78 | N·m |
| Weight | | | — | 10 | — | g |
| Heat-sink flatness | (Note 7) | | –50 | — | 100 | µm |

**Note 6 :** Plain washers (ISO 7089~7094) are recommended.

**Note 7:** Flatness measurement position



## RECOMMENDED OPERATION CONDITIONS

| Symbol | Parameter | Condition | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{CC}$ | Supply voltage | Applied between P-N | | 0 | 300 | 400 | V |
| $V_D$ | Control supply voltage | Applied between $V_{P1}$-$V_{NC}$, $V_{N1}$-$V_{NC}$ | | 13.5 | 15.0 | 16.5 | V |
| $V_{DB}$ | Control supply voltage | Applied between $V_{UFB}$-U, $V_{VFB}$-V, $V_{WFB}$-W | | 13.0 | 15.0 | 18.5 | V |
| $\Delta V_D$, $\Delta V_{DB}$ | Control supply variation | | | –1 | — | 1 | V/µs |
| $t_{dead}$ | Arm shoot-through blocking time | For each input signal, $T_C \leq 100°C$ | | 1.5 | — | — | µs |
| $f_{PWM}$ | PWM input frequency | $T_C \leq 100°C$, $T_j \leq 125°C$ | | — | — | 20 | kHz |
| $I_O$ | Allowable r.m.s. current | $V_{CC}$ = 300V, $V_D$ = $V_{DB}$ = 15V, P.F = 0.8, sinusoidal PWM, $T_j \leq 125°C$, $T_C \leq 100°C$ (Note 8) | $f_{PWM}$ = 5kHz | — | — | 2.5 | Arms |
| | | | $f_{PWM}$ = 15kHz | — | — | 1.5 | |
| PWIN(on) | Allowable minimum input pulse width | (Note 9) | | 0.5 | — | — | µs |
| PWIN(off) | | | | 0.5 | — | — | |
| $V_{NC}$ | $V_{NC}$ variation | Between $V_{NC}$-N (including surge) | | –5.0 | — | 5.0 | V |

**Note 8 :** The allowable r.m.s. current value depends on the actual application conditions.
**9 :** IPM might not make response if the input signal pulse width is less than the recommended minimum value.

### Fig. 7 THE DIP-IPM INTERNAL CIRCUIT

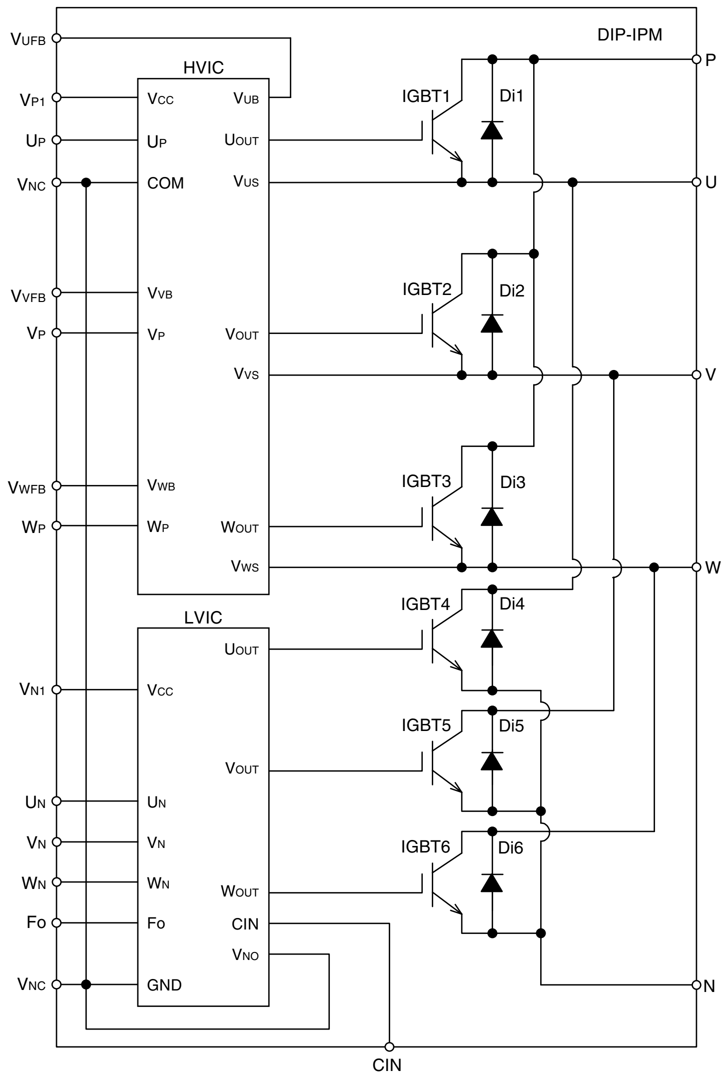
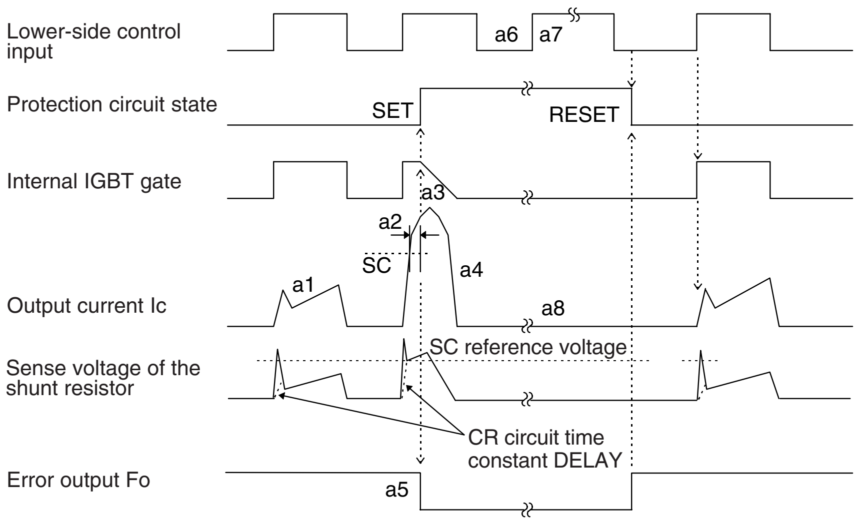


**Fig. 8 TIMING CHART OF THE DIP-IPM PROTECTIVE FUNCTIONS**

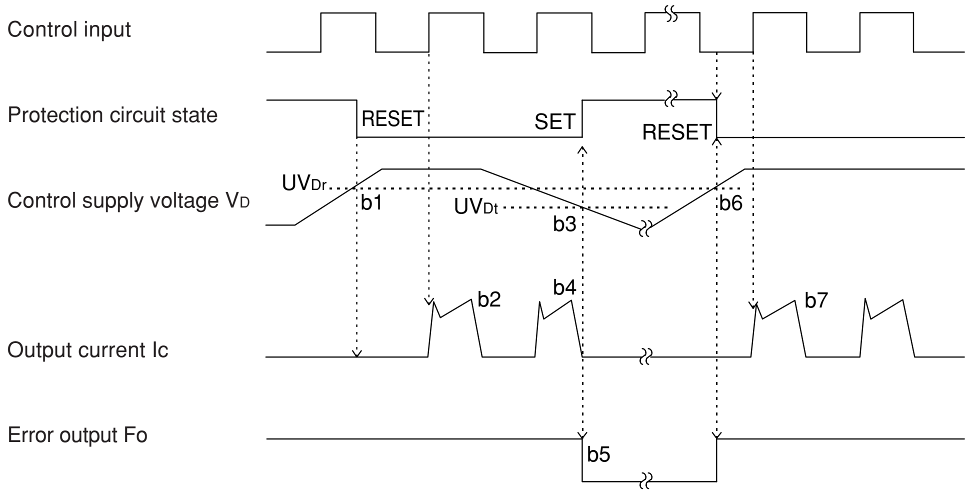
**[A] Short-Circuit Protection (Lower-side only with the external shunt resistor and CR filter)**

a1. Normal operation : IGBT ON and carrying current.
a2. Short circuit detection (SC trigger).
a3. IGBT gate hard interruption.
a4. IGBT turns OFF.
a5. FO outputs ($t_{FO(min)}$ = 20μs).
a6. Input “L” : IGBT OFF.
a7. Input “H” : IGBT ON.
a8. IGBT OFF in spite of input “H”.




**[B] Under-Voltage Protection (Lower-side, $UV_D$)**

b1. Control supply voltage rising : After the voltage level reaches $UV_{Dr}$, the circuits start to operate when next input is applied.
b2. Normal operation : IGBT ON and carrying current.
b3. Under voltage trip ($UV_{Dt}$).
b4. IGBT OFF in spite of control input condition.
b5. FO outputs ($t_{FO}$ ≥ 20μs and FO outputs continuously during UV period).
b6. Under voltage reset ($UV_{Dr}$).
b7. Normal operation : IGBT ON and carrying current.



### [C] Under-Voltage Protection (Upper-side, $UV_{DB}$)

c1. Control supply voltage rising : After the voltage level reaches $UV_{DBr}$, the circuits start to operate when next input is applied.
c2. Normal operation : IGBT ON and carrying current.
c3. Under voltage trip ($UV_{DBt}$).
c4. IGBT OFF in spite of control input signal level, but there is no $F_O$ signal outputs.
c5. Under voltage reset ($UV_{DBr}$).
c6. Normal operation : IGBT ON and carrying current.

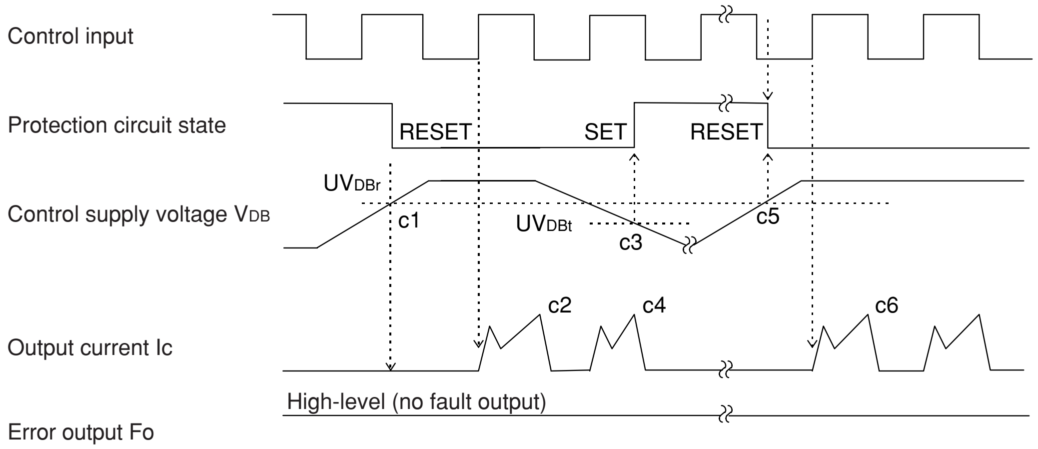
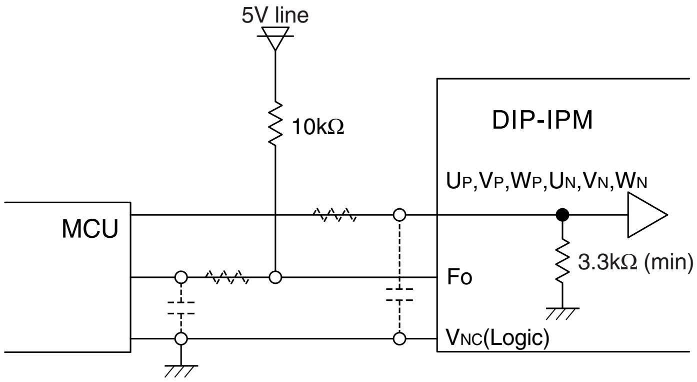
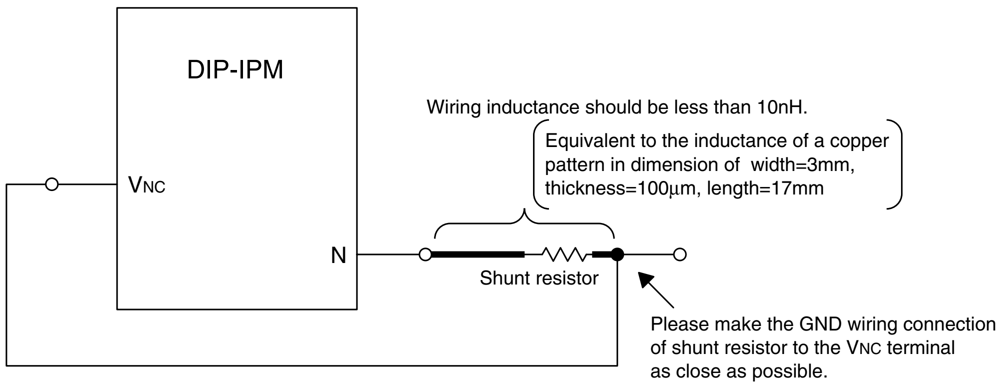



**Fig. 9 RECOMMENDED MCU I/O INTERFACE CIRCUIT**

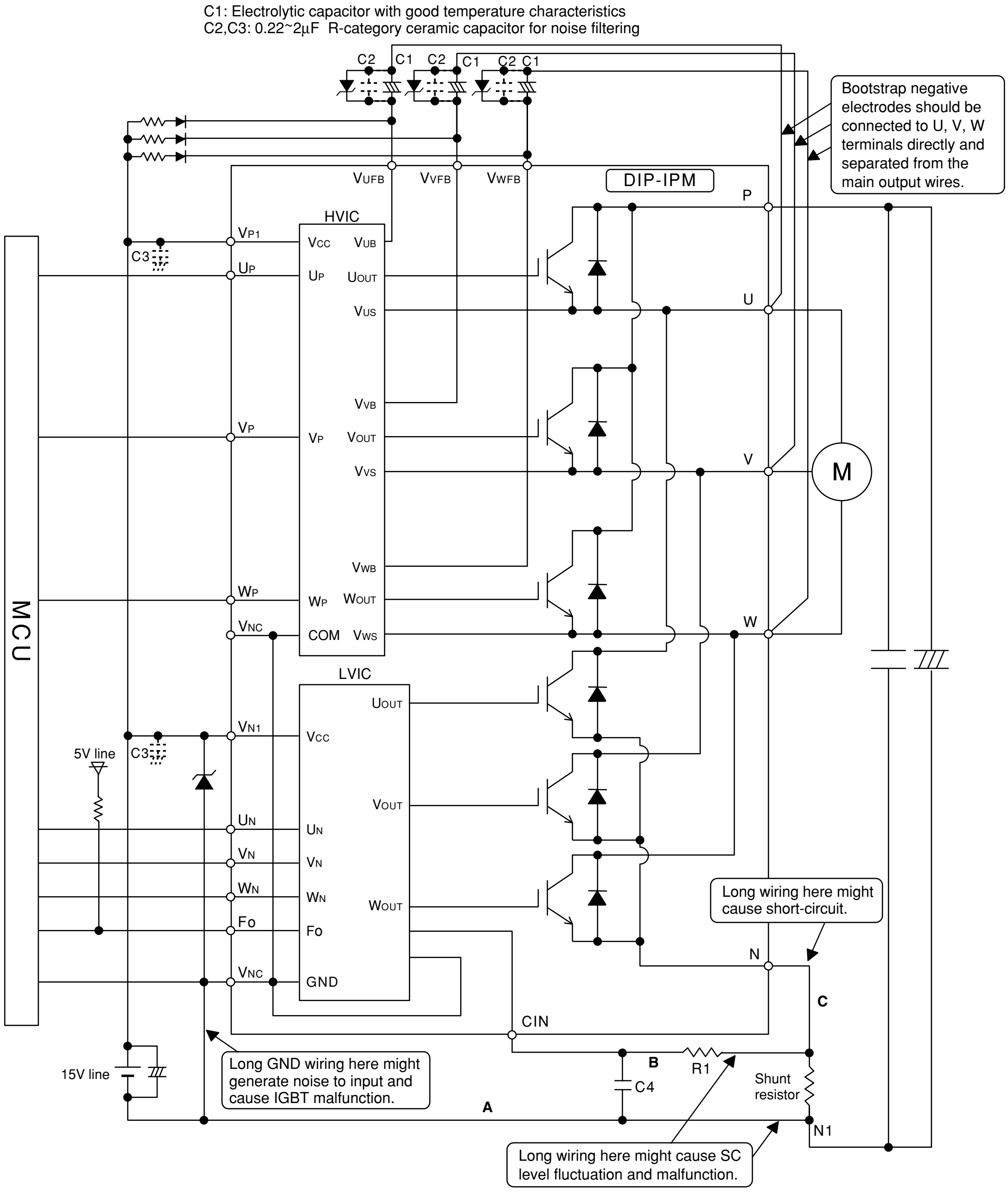



**Note :** The setting of RC coupling at each input (parts shown dotted) depends on the PWM control scheme and the wiring impedance of the printed circuit board.
The DIP-IPM input section integrates a 3.3kΩ (min) pull-down resistor. Therefore, when using an external filtering resistor, pay attention to the turn-on threshold voltage.

**Fig. 10 WIRING CONNECTION OF SHUNT RESISTOR**



## Fig. 11 AN EXAMPLE OF TYPICAL DIP-IPM APPLICATION CIRCUIT




**Note 1** : Input drive is High-Active type. There is a 3.3kΩ(min.) pull-down resistor integrated in the IC input circuit. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.

**2** : Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.

**3** : FO output is open drain type. It should be pulled up to the positive side of a 5V power supply by a resistor of about 10kΩ.

**4** : To prevent erroneous protection, the wiring of A, B, C should be as short as possible.

**5** : The time constant R1C4 of the protection circuit should be selected in the range of 1.5-2µs. SC interrupting time might vary with the wiring pattern. Tight tolerance, temp-compensated type is recommended for R1, C4.

**6** : All capacitors should be mounted as close to the terminals of the DIP-IPM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2, C3: good temperature, frequency and DC bias characteristic ceramic type are recommended.)

**7** : To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1-0.22µF snubber between the P-N1 terminals is recommended.

**8** : Two VNC terminals (9 & 16 pin) are connected inside DIP-IPM, please connect either one to the 15V power supply GND outside and leave another one open.

**9** : It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.

**10** : If control GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point.