

## 4-1/2 Digit Analog-to-Digital Converters with On-Chip LCD Drivers

### Features

- Count Resolution:  $\pm 19,999$
- Resolution on 200mV Scale:  $10\mu\text{V}$
- True Differential Input and Reference
- Low Power Consumption:  $500\mu\text{A}$  at 9V
- Direct LCD Driver for 4-1/2 Digits, Decimal Points, Low Battery Indicator, and Continuity Indicator
- Over Range and Under Range Outputs
- Range Select Input: 10:1
- High Common Mode Rejection Ratio: 110dB
- External Phase Compensation Not Required

### Applications

- Full Featured Multimeters
- Digital Measurement Devices

### Device Selection Table

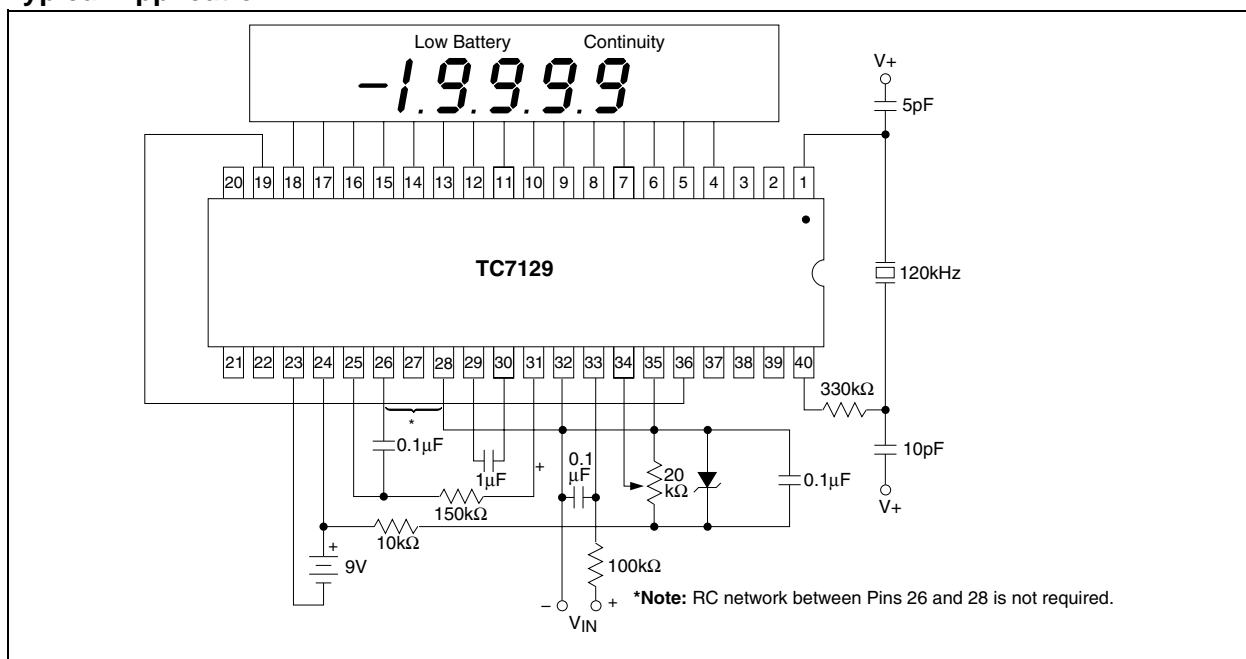
Package Code	Pin Layout	Package	Temperature Range
TC7129CPL	Normal	40-Pin PDIP	0°C to +70°C
TC7129CKW	Formed	44-Pin PQFP	0°C to +70°C
TC7129CLW	—	44-Pin PLCC	0°C to +70°C

### General Description

The TC7129 is a 4-1/2 digit analog-to-digital converter (ADC) that directly drives a multiplexed liquid crystal display (LCD). Fabricated in high performance, low power CMOS, the TC7129 ADC is designed specifically for high resolution, battery powered digital multimeter applications. The traditional dual slope method of A/D conversion has been enhanced with a successive integration technique to produce readings accurate to better than 0.005% of full scale, and resolution down to  $10\mu\text{V}$  per count.

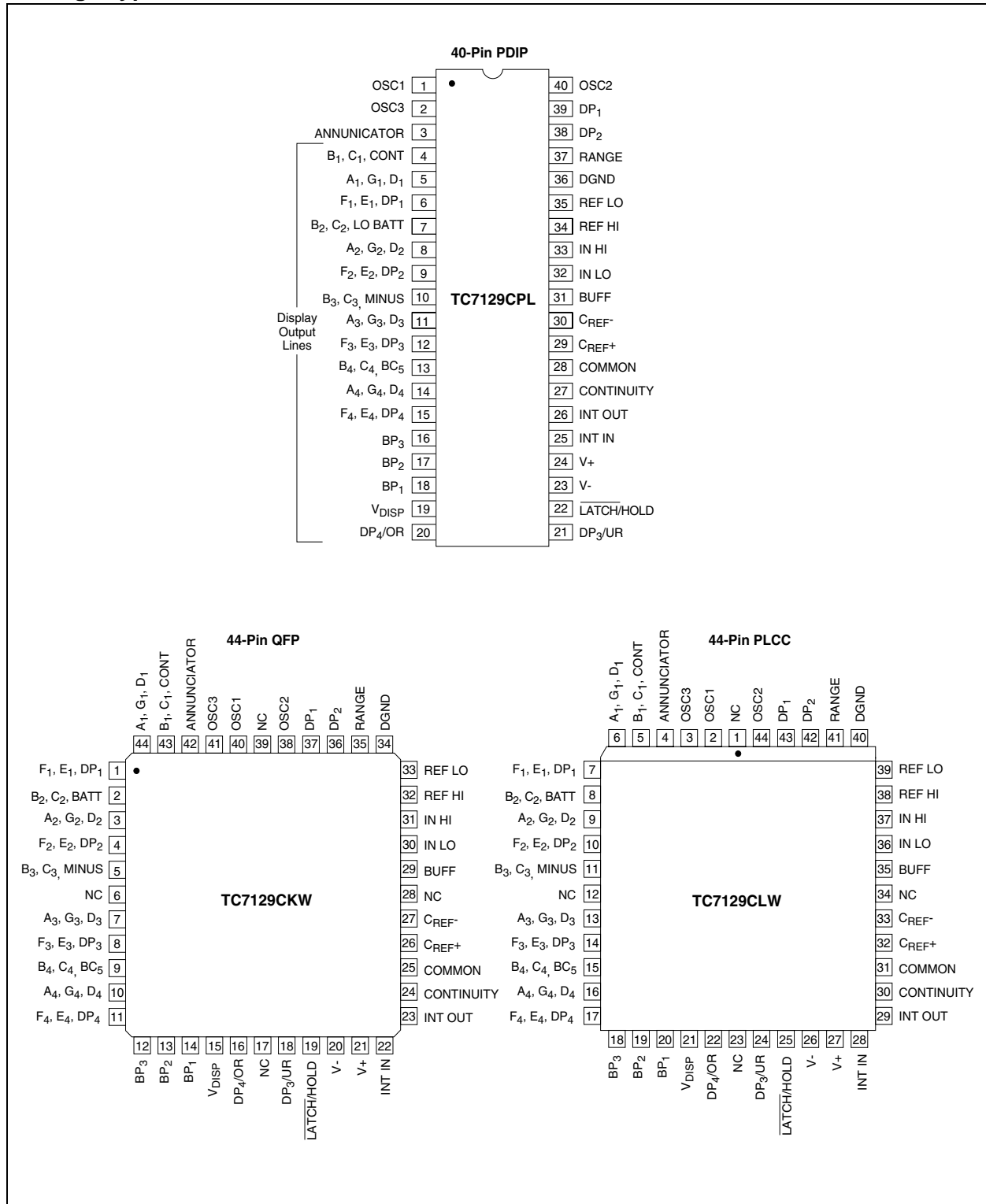
The TC7129 includes features important to multimeter applications. It detects and indicates low battery condition. A continuity output drives an annunciator on the display, and can be used with an external driver to sound an audible alarm. Over range and under range outputs and a range change input provide the ability to create auto-ranging instruments. For snapshot readings, the TC7129 includes a latch-and-hold input to freeze the present reading. This combination of features makes the TC7129 the ideal choice for full featured multimeter and digital measurement applications.

### Typical Application



# TC7129

## Package Type



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings\*

Supply Voltage (V+ to V-)	15V
Reference Voltage (REF HI or REF LO)	V+ to V-
Input Voltage (IN HI or IN LO) (Note 1)	V+ to V-
V <sub>DISP</sub>	V+ to (DGND - 0.3V)
Digital Input (Pins 1, 2, 19, 20, 21, 22, 27, 37, 39, 40)	DGND to V+
Analog Input (Pins 25, 29, 30)	V+ to V-
Package Power Dissipation (T <sub>A</sub> ≤ 70°C)	
Plastic DIP	1.23W
PLCC	1.23W
Plastic QFP	1.00W
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

## TC7129 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: V+ to V- = 9V, V <sub>REF</sub> = 1V, T <sub>A</sub> = +25°C, f <sub>CLK</sub> = 120kHz, unless otherwise indicated. Pin numbers refer to 40-pin DIP.						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
<b>Input</b>						
	Zero Input Reading	-0000	0000	+0000	Counts	V <sub>IN</sub> = 0V, 200mV Scale
	Zero Reading Drift	—	±0.5	—	μV/°C	V <sub>IN</sub> = 0V, 0°C < T <sub>A</sub> < +70°C
	Ratiometric Reading	9997	9999	10000	Counts	V <sub>IN</sub> = V <sub>REF</sub> = 1000mV, Range = 2V
	Range Change Accuracy	0.9999	1.0000	1.0001	Ratio	V <sub>IN</sub> = 1V on High Range, V <sub>IN</sub> = 0.1V on Low Range
RE	Rollover Error	—	1	2	Counts	V <sub>IN</sub> <sup>-</sup> = V <sub>IN</sub> <sup>+</sup> = 199mV
NL	Linearity Error	—	1	—	Counts	200mV Scale
CMRR	Common Mode Rejection Ratio	—	110	—	dB	V <sub>CM</sub> = 1V, V <sub>IN</sub> = 0V, 200mV Scale
CMVR	Common Mode Voltage Range	—	(V-) + 1.5	—	V	V <sub>IN</sub> = 0V
		—	(V+) - 1	—	V	200mV Scale
e <sub>N</sub>	Noise (Peak-to-Peak Value not Exceeded 95% of Time)	—	14	—	μV <sub>P-P</sub>	V <sub>IN</sub> = 0V 200mV Scale
I <sub>IN</sub>	Input Leakage Current	—	1	10	pA	V <sub>IN</sub> = 0V, Pins 32, 33
	Scale Factor Temperature Coefficient	—	2	7	ppm/°C	V <sub>IN</sub> = 199mV, 0°C < T <sub>A</sub> < +70°C External V <sub>REF</sub> = 0ppm/°C
<b>Power</b>						
V <sub>COM</sub>	Common Voltage	2.8	3.2	3.5	V	V+ to Pin 28
	Common Sink Current	—	0.6	—	mA	ΔCommon = +0.1V
	Common Source Current	—	10	—	μA	ΔCommon = -0.1V
DGND	Digital Ground Voltage	4.5	5.3	5.8	V	V+ to Pin 36, V+ to V- = 9V
	Sink Current	—	1.2	—	mA	ΔDGND = +0.5V
	Supply Voltage Range	6	9	12	V	V+ to V-
I <sub>S</sub>	Supply Current Excluding Common Current	—	0.8	1.3	mA	V+ to V- = 9V

**Note 1:** Input voltages may exceed supply voltages, provided input current is limited to ±400μA. Currents above this value may result in invalid display readings, but will not destroy the device if limited to ±1mA. Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

# TC7129

## TC7129 ELECTRICAL SPECIFICATIONS (CONTINUED)

**Electrical Characteristics:**  $V_+$  to  $V_- = 9V$ ,  $V_{REF} = 1V$ ,  $T_A = +25^\circ C$ ,  $f_{CLK} = 120kHz$ , unless otherwise indicated.  
Pin numbers refer to 40-pin DIP.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$f_{CLK}$	Clock Frequency	—	120	360	kHz	
	$V_{DISP}$ Resistance	—	50	—	$k\Omega$	$V_{DISP}$ to $V_+$
	Low Battery Flag Activation Voltage	6.3	7.2	7.7	V	$V_+$ to $V_-$
<b>Digital</b>						
	Continuity Comparator Threshold Voltages	100	200	—	mV	$V_{OUT}$ Pin 27 = High
		—	200	400	mV	$V_{OUT}$ Pin 27 = Low
	Pull-down Current	—	2	10	$\mu A$	Pins 37, 38, 39
	"Weak Output" Current Sink/Source	—	3/3	—	$\mu A$	Pins 20, 21 Sink/Source
		—	3/9	—	$\mu A$	Pin 27 Sink/Source
	Pin 22 Source Current	—	40	—	$\mu A$	
	Pin 22 Sink Current	—	3	—	$\mu A$	

**Note 1:** Input voltages may exceed supply voltages, provided input current is limited to  $\pm 400\mu A$ . Currents above this value may result in invalid display readings, but will not destroy the device if limited to  $\pm 1mA$ . Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

**TABLE 2-1: PIN FUNCTION TABLE**

Pin No. 40-Pin PDIP	Pin No. 44-Pin PQFP	Pin No. 44-Pin PLCC	Symbol	Function
1	40	2	OSC1	Input to first clock inverter.
2	41	3	OSC3	Output of second clock inverter.
3	42	4	ANNUNCIATOR	Backplane square wave output for driving annunciators.
4	43	5	B <sub>1</sub> , C <sub>1</sub> , CONT	Output to display segments.
5	44	6	A <sub>1</sub> , G <sub>1</sub> , D <sub>1</sub>	Output to display segments.
6	1	7	F <sub>1</sub> , E <sub>1</sub> , DP <sub>1</sub>	Output to display segments.
7	2	8	B <sub>2</sub> , C <sub>2</sub> , LO BATT	Output to display segments.
8	3	9	A <sub>2</sub> , G <sub>2</sub> , D <sub>2</sub>	Output to display segments.
9	4	10	F <sub>2</sub> , E <sub>2</sub> , DP <sub>2</sub>	Output to display segments.
10	5	11	B <sub>3</sub> , C <sub>3</sub> , MINUS	Output to display segments.
11	7	13	A <sub>3</sub> , G <sub>3</sub> , D <sub>3</sub>	Output to display segments.
12	8	14	F <sub>3</sub> , E <sub>3</sub> , DP <sub>3</sub>	Output to display segments.
13	9	15	B <sub>4</sub> , C <sub>4</sub> , BC <sub>5</sub>	Output to display segments.
14	10	16	A <sub>4</sub> , D <sub>4</sub> , G <sub>4</sub>	Output to display segments.
15	11	17	F <sub>4</sub> , E <sub>4</sub> , DP <sub>4</sub>	Output to display segments.
16	12	18	BP <sub>3</sub>	Backplane #3 output to display.
17	13	19	BP <sub>2</sub>	Backplane #2 output to display.
18	14	20	BP <sub>1</sub>	Backplane #1 output to display.
19	15	21	V <sub>DISP</sub>	Negative rail for display drivers.
20	16	22	DP <sub>4</sub> /OR	Input: When HI, turns on most significant decimal point. Output: Pulled HI when result count exceeds ±19,999.
21	18	24	DP <sub>3</sub> /UR	Input: Second most significant decimal point on when HI. Output: Pulled HI when result count is less than ±1000.
22	19	25	LATCH/HOLD	Input: When floating, ADC operates in the Free Run mode. When pulled HI, the last displayed reading is held. When pulled LO, the result counter contents are shown incrementing during the de-integrate phase of cycle. Output: Negative going edge occurs when the data latches are updated. Can be used for converter status signal.
23	20	26	V-	Negative power supply terminal.
24	21	27	V+	Positive power supply terminal and positive rail for display drivers.
25	22	28	INT IN	Input to integrator amplifier.
26	23	29	INT OUT	Output of integrator amplifier.
27	24	30	CONTINUITY	Input: When LO, continuity flag on the display is OFF. When HI, continuity flag is ON. Output: HI when voltage between inputs is less than +200mV. LO when voltage between inputs is more than +200mV.
28	25	31	COMMON	Sets Common mode voltage of 3.2V below V+ for DE, 10X, etc. Can be used as pre-regulator for external reference.
29	26	32	C <sub>REF+</sub>	Positive side of external reference capacitor.
30	27	33	C <sub>REF-</sub>	Negative side of external reference capacitor.
31	29	35	BUFFER	Output of buffer amplifier.
32	30	36	IN LO	Negative input voltage terminal.
33	31	37	IN HI	Positive input voltage terminal.
34	32	38	REF HI	Positive reference voltage.
35	33	39	REF LO	Negative reference voltage

# TC7129

---

---

**TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)**

Pin No. 40-Pin PDIP	Pin No. 44-Pin PQFP	Pin No. 44-Pin PLCC	Symbol	Function
36	34	40	DGND	Internal ground reference for digital section. See Section 4.3, $\pm 5V$ Power Supply.
37	35	41	RANGE	3 $\mu A$ pull-down for 200mV scale. Pulled HI externally for 2V scale.
38	36	42	DP <sub>2</sub>	Internal 3 $\mu A$ pull-down. When HI, decimal point 2 will be on.
39	37	43	DP <sub>1</sub>	Internal 3 $\mu A$ pull-down. When HI, decimal point 1 will be on.
40	38	44	OSC2	Output of first clock inverter. Input of second clock inverter.
—	6,17, 28, 39	12, 23, 34, 1	NC	No connection.

## 3.0 DETAILED DESCRIPTION

(All Pin Designations Refer to 40-Pin PDIP.)

The TC7129 is designed to be the heart of a high resolution analog measurement instrument. The only additional components required are a few passive elements: a voltage reference, an LCD, and a power source. Most component values are not critical; substitutes can be chosen based on the information given below.

The basic circuit for a digital multimeter application is shown in Figure 3-1. See Section 4.0, Typical Applications for variations. Typical values for each component are shown. The sections below give component selection criteria.

### 3.1 Oscillator ( $X_{OSC}$ , $C_{O1}$ , $C_{O2}$ , $R_O$ )

The primary criterion for selecting the crystal oscillator is to choose a frequency that achieves maximum rejection of line frequency noise. To do this, the integration phase should last an integral number of line cycles. The integration phase of the TC7129 is 10,000 clock cycles on the 200mV range and 1000 clock cycles on the 2V range. One clock cycle is equal to two oscillator cycles. For 60Hz rejection, the oscillator frequency should be chosen so that the period of one line cycle equals the integration time for the 2V range:

#### EQUATION 3-1:

$$\frac{1}{60} \text{ second} = 16.7\text{msec} = \frac{1000 \text{ clock cycles} * 2 \text{ OSC cycles/clock cycle}}{\text{OSC Frequency}}$$

This equation gives an oscillator frequency of 120kHz. A similar calculation gives an optimum frequency of 100kHz for 50Hz rejection.

The resistor and capacitor values are not critical; those shown work for most applications. In some situations, the capacitor values may have to be adjusted to compensate for parasitic capacitance in the circuit. The capacitors can be low cost ceramic devices.

Some applications can use a simple RC network instead of a crystal oscillator. The RC oscillator has more potential for jitter, especially in the least significant digit. See Section 4.8, RC Oscillator.

### 3.2 Integrating Resistor ( $R_{INT}$ )

The integrating resistor sets the charging current for the integrating capacitor. Choose a value that provides a current between 5 $\mu$ A and 20 $\mu$ A at 2V, the maximum full scale input. The typical value chosen gives a charging current of 13.3 $\mu$ A:

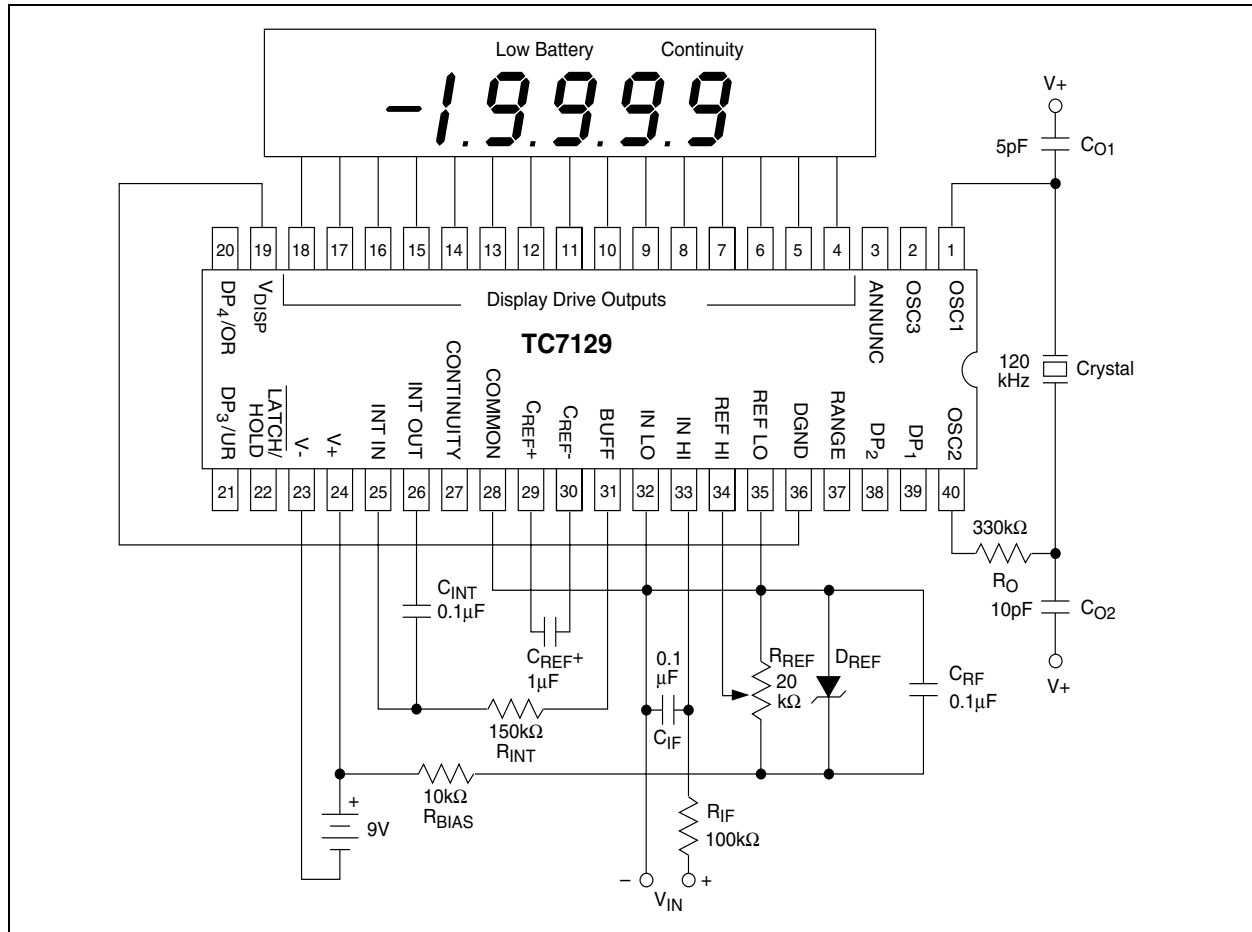
#### EQUATION 3-2:

$$I_{\text{CHARGE}} = \frac{2V}{150k\Omega} = 13.3\mu A$$

Too high a value for  $R_{INT}$  increases the sensitivity to noise pickup and increases errors due to leakage current. Too low a value degrades the linearity of the integration, leading to inaccurate readings.

# TC7129

FIGURE 3-1: STANDARD CIRCUIT



### 3.3 Integrating Capacitor ( $C_{INT}$ )

The charge stored in the integrating capacitor during the integrate phase is directly proportional to the input voltage. The primary selection criterion for  $C_{INT}$  is to choose a value that gives the highest voltage swing while remaining within the high linearity portion of the integrator output range. An integrator swing of 2V is the recommended value. The capacitor value can be calculated using the following equation:

#### EQUATION 3-3:

$$C_{INT} = \frac{t_{INT} \times I_{INT}}{V_{SWING}}$$

Where  $t_{INT}$  is the integration time.

Using the values derived above (assuming 60Hz operation), the equation becomes:

#### EQUATION 3-4:

$$C_{INT} = \frac{16.7\text{msec} \times 13.3\mu\text{A}}{2\text{V}} = 0.1\mu\text{A}$$

The capacitor should have low dielectric absorption to ensure good integration linearity. Polypropylene and Teflon capacitors are usually suitable. A good measurement of the dielectric absorption is to connect the reference capacitor across the inputs by connecting:

#### Pin to Pin:

20 → 33 ( $C_{REF+}$  to IN HI)

30 → 32 ( $C_{REF-}$  to IN LO)

A reading between 10,000 and 9998 is acceptable; anything lower indicates unacceptably high dielectric absorption.

### 3.4 Reference Capacitor ( $C_{REF}$ )

The reference capacitor stores the reference voltage during several phases of the measurement cycle. Low leakage is the primary selection criterion for this component. The value must be high enough to offset the effect of stray capacitance at the capacitor terminals. A value of at least 1μF is recommended.



### 3.5 Voltage Reference ( $D_{REF}$ , $R_{REF}$ , $R_{BIAS}$ , $C_{RF}$ )

The reference potentiometer ( $R_{REF}$ ) provides an adjustment for adjusting the reference voltage; any value above 20k $\Omega$  is adequate. The bias resistor ( $R_{BIAS}$ ) limits the current through  $D_{REF}$  to less than 150 $\mu$ A. The reference filter capacitor ( $C_{RF}$ ) forms an RC filter with  $R_{BIAS}$  to help eliminate noise.

### 3.6 Input Filter ( $R_{IF}$ , $C_{IF}$ )

For added stability, an RC input noise filter is usually included in the circuit. The input filter resistor value should not exceed 100k $\Omega$ . A typical RC time constant value is 16.7msec to help reject line frequency noise. The input filter capacitor should have low leakage for a high-impedance input.

### 3.7 Battery

The typical circuit uses a 9V battery as a power source. Any value between 6V and 12V can be used. For operation from batteries with voltages lower than 6V and for operation from power supplies, see Section 4.2, Powering the TC7129.

## 4.0 TYPICAL APPLICATIONS

### 4.1 TC7129 as a Replacement Part

The TC7129 is a direct pin-for-pin replacement part for the ICL7129. Note, however, that part requires a capacitor and resistor between Pins 26 and 28 for phase compensation. Since the TC7129 uses internal phase compensation, these parts are not required and, in fact, **must be removed** from the circuit for stable operation.

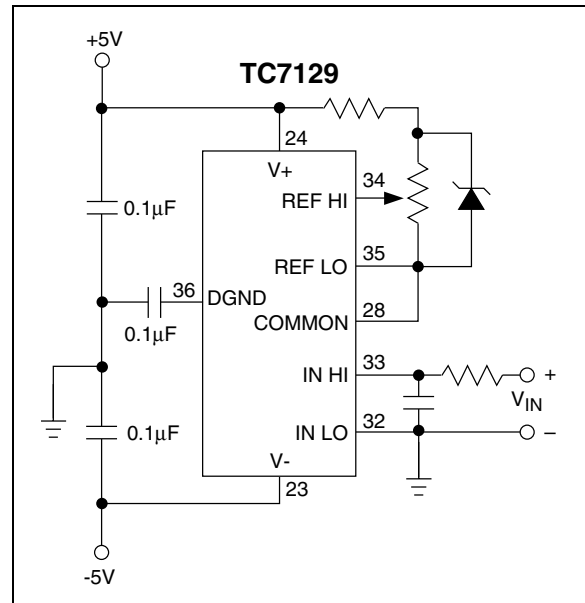
### 4.2 Powering the TC7129

While the most common power source for the TC7129 is a 9V battery, there are other possibilities. Some of the more common ones are explained below.

### 4.3 $\pm$ 5V Power Supply

Measurements are made with respect to power supply ground. DGND (Pin 36) is set internally to about 5V less than  $V_+$  (Pin 24); it is not intended as a power supply input and must not be tied directly to power supply ground. It can be used as a reference for external logic, as explained in Section 4.6, Connecting to External Logic (see Figure 4-1).

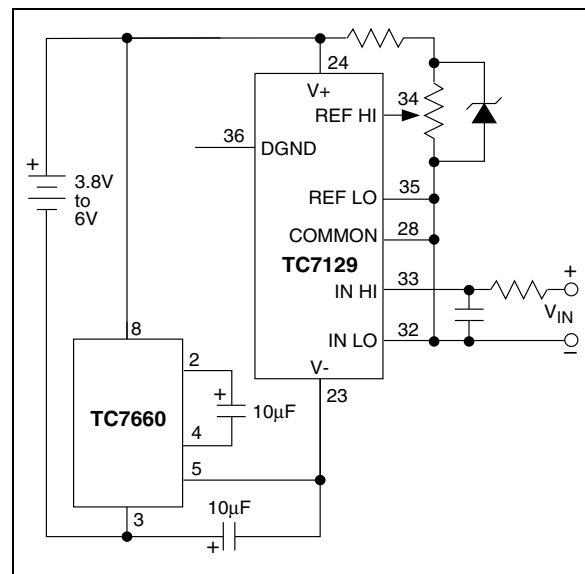
**FIGURE 4-1: POWERING THE TC7129 FROM A  $\pm$ 5V POWER SUPPLY**



### 4.4 Low Voltage Battery Source

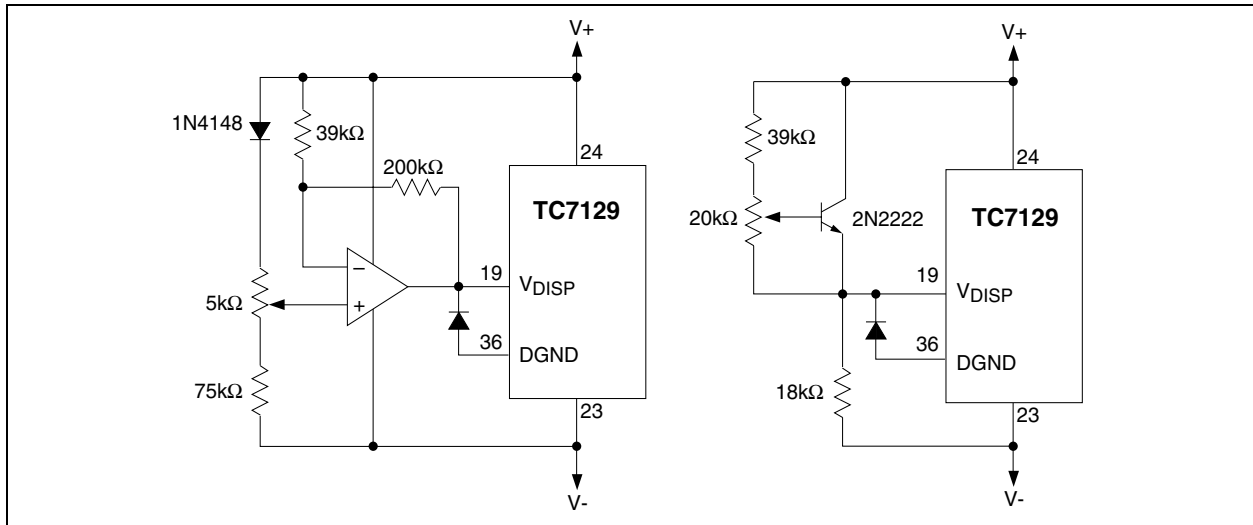
A battery with voltage between 3.8V and 6V can be used to power the TC7129, when used with a voltage doubler circuit, as shown in Figure 4-2. The voltage doubler uses the TC7660 DC-to-DC voltage converter and two external capacitors.

**FIGURE 4-2: POWERING THE TC7129 FROM A LOW VOLTAGE BATTERY**





**FIGURE 4-6: TEMPERATURE COMPENSATING CIRCUITS**



## 4.8 RC Oscillator

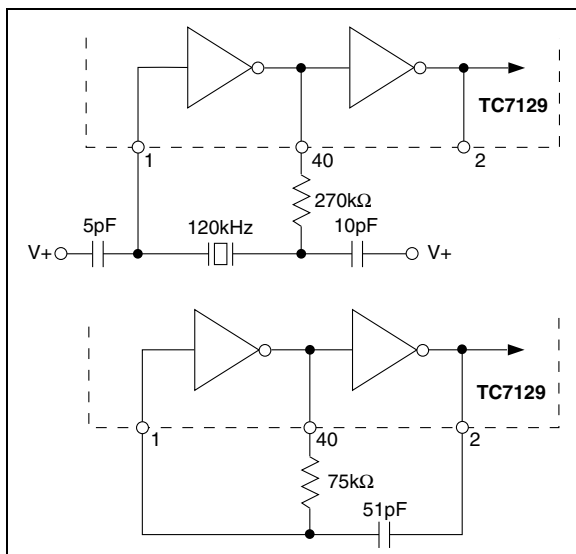
For applications in which 3-1/2 digit (100μV) resolution is sufficient, an RC oscillator is adequate. A recommended value for the capacitor is 51pF. Other values can be used as long as they are sufficiently larger than the circuit parasitic capacitance. The resistor value is calculated as:

**EQUATION 4-1:**

$$R = \frac{0.45}{\text{Freq} * C}$$

For 120kHz frequency and C = 51pF, the calculated value of R is 75kΩ. The RC oscillator and the crystal oscillator circuits are shown in Figure 4-7.

**FIGURE 4-7: OSCILLATOR CIRCUITS**



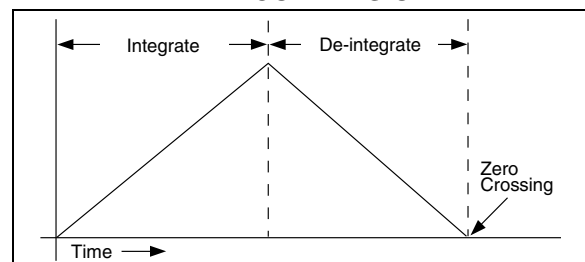
## 4.9 Measuring Techniques

Two important techniques are used in the TC7129: successive integration and digital auto-zeroing. Successive integration is a refinement to the traditional dual slope conversion technique.

### 4.10 Dual Slope Conversion

A dual slope conversion has two basic phases: integrate and de-integrate. During the integrate phase, the input signal is integrated for a fixed period of time; the integrated voltage level is thus proportional to the input voltage. During the de-integrate phase, the integrated voltage is ramped down at a fixed slope, and a counter counts the clock cycles until the integrator voltage crosses zero. The count is a measurement of the time to ramp the integrated voltage to zero, and is, therefore, proportional to the input voltage being measured. This count can then be scaled and displayed as a measurement of the input voltage. Figure 4-8 shows the phases of the dual slope conversion.

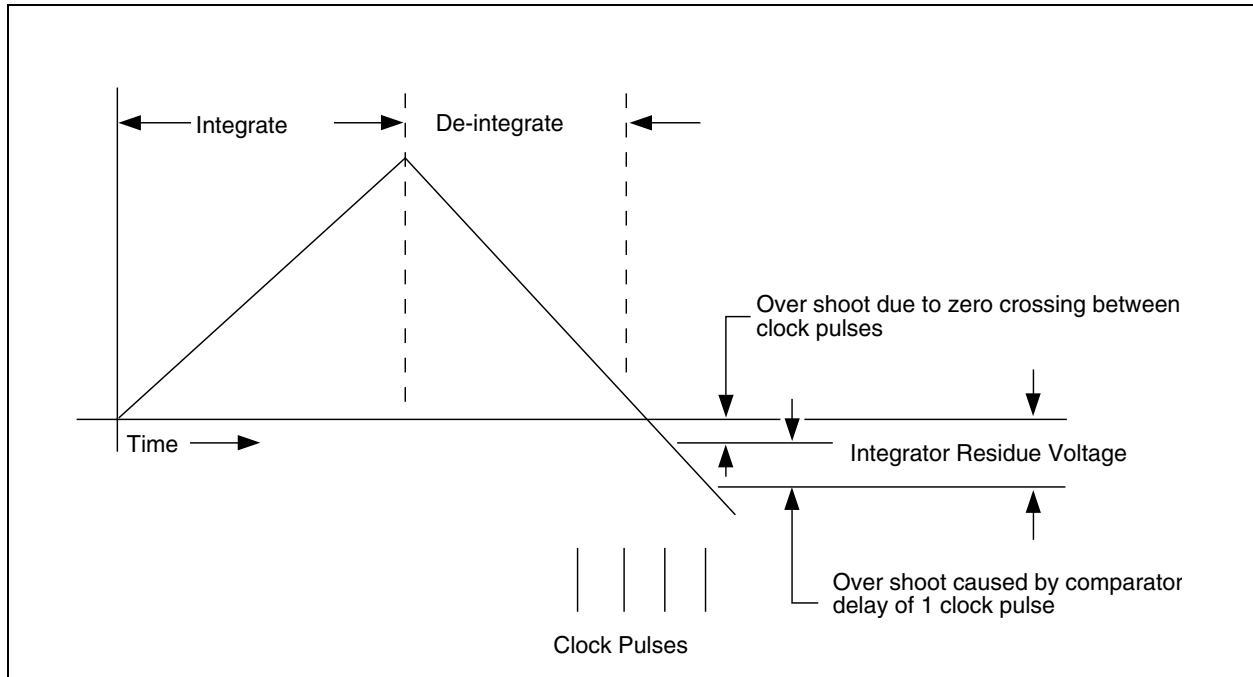
**FIGURE 4-8: DUAL SLOPE CONVERSION**



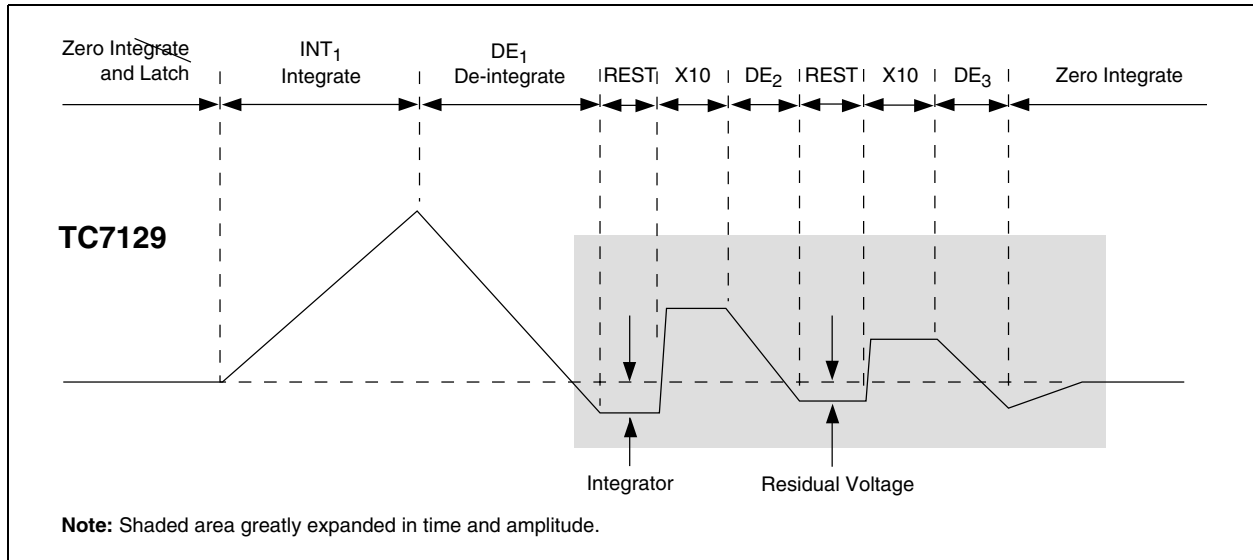
The dual slope method has a fundamental limitation. The count can only stop on a clock cycle, so that measurement accuracy is limited to the clock frequency. In addition, a delay in the zero crossing comparator can add to the inaccuracy. Figure 4-9 shows these errors in an actual measurement.

# TC7129

**FIGURE 4-9: ACCURACY ERRORS IN DUAL SLOPE CONVERSION**



**FIGURE 4-10: INTEGRATION WAVEFORM**



## 4.11 Successive Integration

The successive integration technique picks up where dual slope conversion ends. The over shoot voltage shown in Figure 4-9, called the "integrator residue voltage," is measured to obtain a correction to the initial count. Figure 4-10 shows the cycles in a successive integration measurement.

The waveform shown is for a negative input signal. The sequence of events during the measurement cycle is shown in Table 4-1.

**TABLE 4-1: MEASUREMENT CYCLE SEQUENCE**

Phase	Description
INT <sub>1</sub>	Input signal is integrated for fixed time (1000 clock cycles on 2V scale, 10,000 on 200 mV).
DE <sub>1</sub>	Integrator voltage is ramped to zero. Counter counts up until zero crossing to produce reading accurate to 3-1/2 digits. Residue represents an over shoot of the actual input voltage.
REST	Rest; circuit settles.
X10	Residue voltage is amplified 10 times and inverted.
DE <sub>2</sub>	Integrator voltage is ramped to zero. Counter counts down until zero crossing to correct reading to 4-1/2 digits. Residue represents an under shoot of the actual input voltage.
REST	Rest; circuit settles.
X10	Residue voltage is amplified 10 times and inverted.
DE <sub>3</sub>	Integrator voltage is ramped to zero. Counter counts up until zero crossing to correct reading to 5-1/2 digits. Residue is discarded.

## 4.12 Digital Auto-Zeroing

To eliminate the effect of amplifier offset errors, the TC7129 uses a digital auto-zeroing technique. After the input voltage is measured as described above, the measurement is repeated with the inputs shorted internally. The reading with inputs shorted is a measurement of the internal errors and is subtracted from the previous reading to obtain a corrected measurement. Digital auto-zeroing eliminates the need for an external auto-zeroing capacitor used in other ADCs.

## 4.13 Inside the TC7129

Figure 4-11 shows a simplified block diagram of the TC7129.

# TC7129

FIGURE 4-11: TC7129 FUNCTIONAL BLOCK DIAGRAM

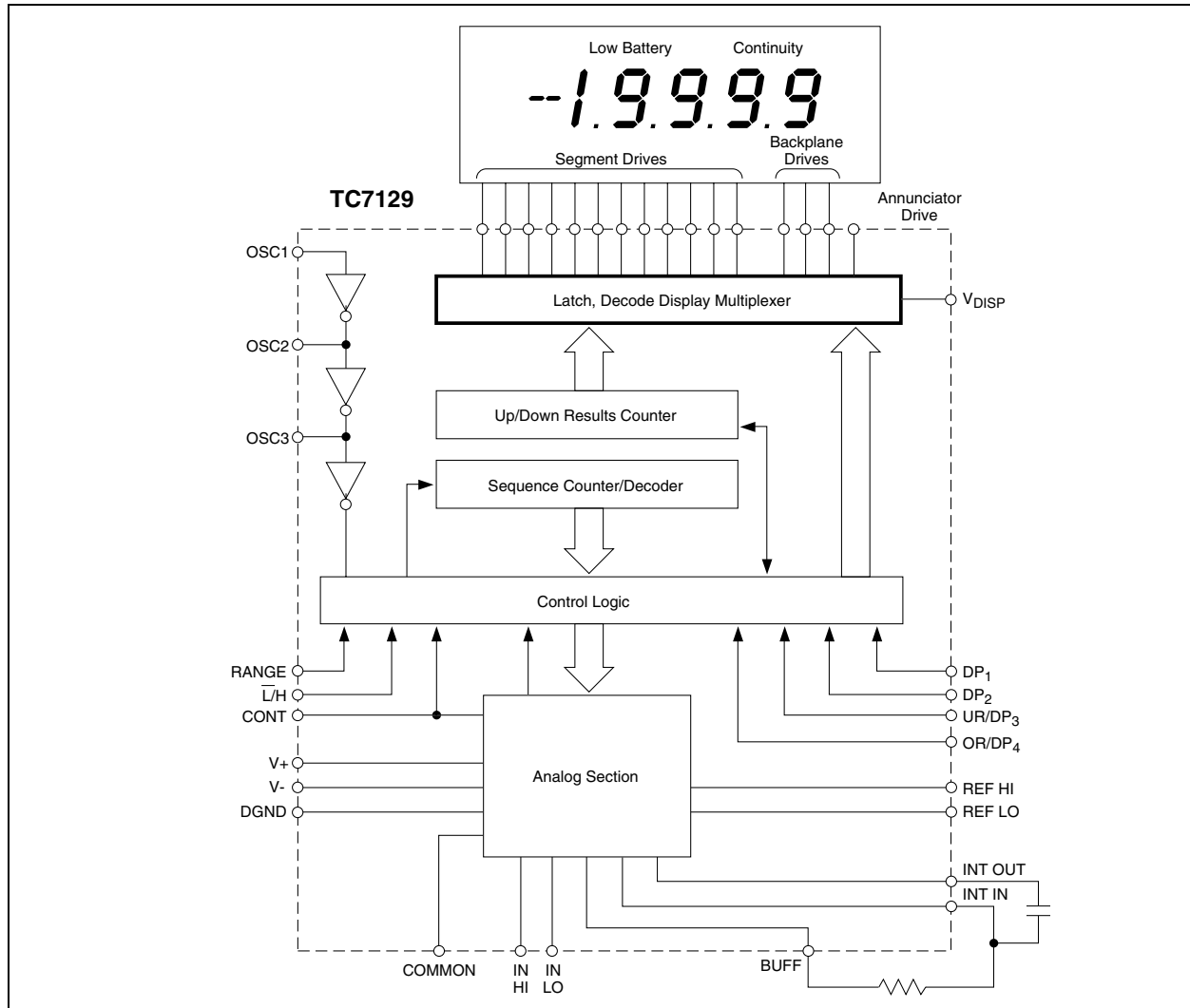
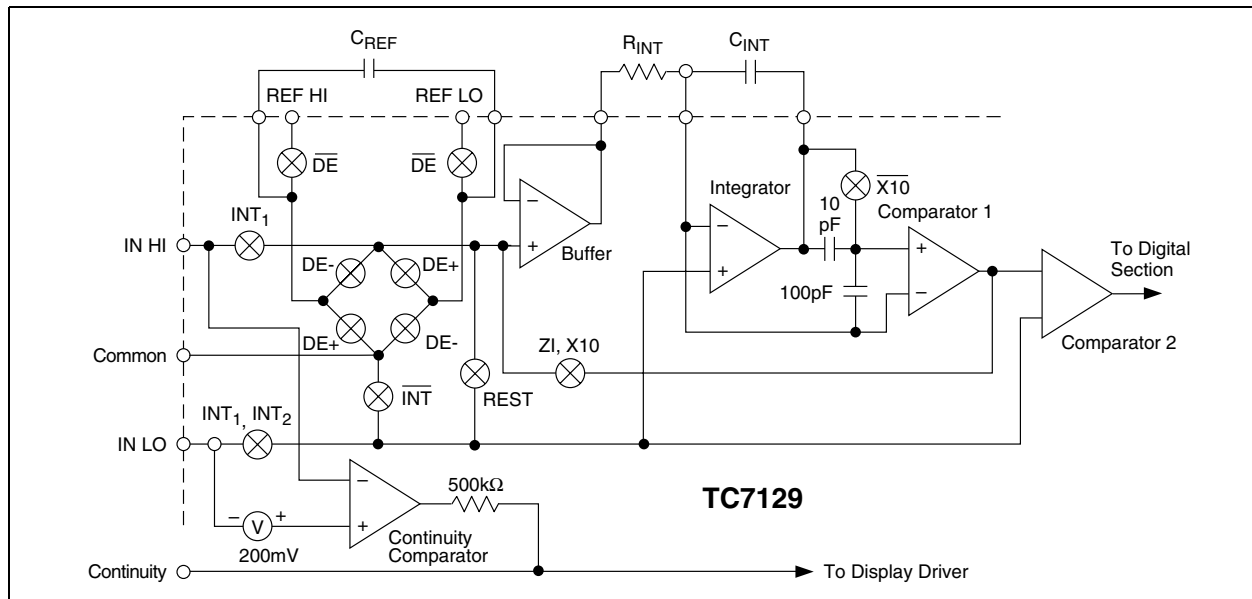


FIGURE 4-12: INTEGRATOR BLOCK DIAGRAM



## 4.14 Integrator Section

The integrator section includes the integrator, comparator, input buffer amplifier, and analog switches (see Table 4-2), used to change the circuit configuration during the separate measurement phases described earlier. See Integrator Block Diagram (Figure 4-12).

**TABLE 4-2: SWITCH LEGENDS**

Label	Description
Label	Meaning.
DE	Open during all de-integrate phases.
DE-	Closed during all de-integrate phases when input voltage is negative.
DE+	Closed during all de-integrate phases when input voltage is positive.
INT <sub>1</sub>	Closed during the first integrate phase (measurement of the input voltage).
INT <sub>2</sub>	Closed during the second integrate phase (measurement of the amplifier offset).
INT	Open during both integrate phases.
REST	Closed during the rest phase.
ZI	Closed during the zero integrate phase.
X10	Closed during the X10 phase.
X10	Open during the X10 phase.

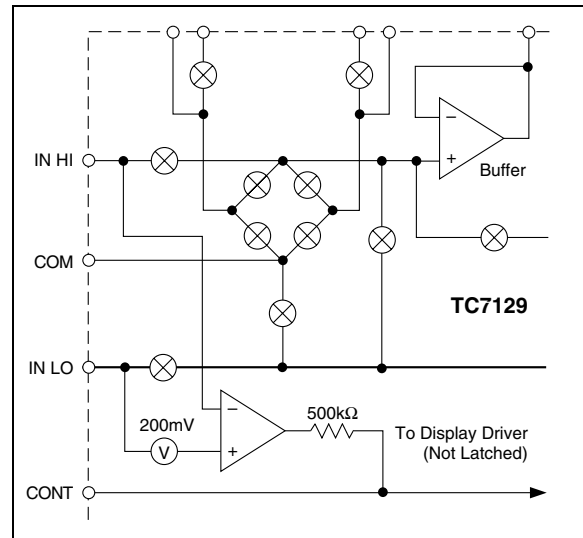
The buffer amplifier has a Common mode input voltage range from 1.5V above V- to 1V below V+. The integrator amplifier can swing to within 0.3V of the rails, although for best linearity, the swing is usually limited to within 1V. Both amplifiers can supply up to 80μA of output current, but should be limited to 20μA for good linearity.

## 4.15 Continuity Indicator

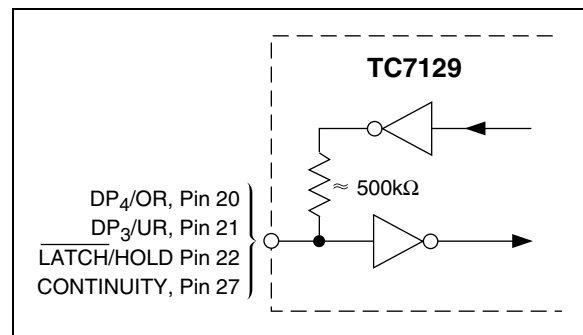
A comparator with a 200mV threshold is connected between IN HI (Pin 33) and IN LO (Pin 32). Whenever the voltage between inputs is less than 200mV, the CONTINUITY output (Pin 27) will be pulled HIGH, activating the continuity annunciator on the display. The continuity pin can also be used as an input to drive the continuity annunciator directly from an external source (see Figure 4-13).

A schematic of the input/output nature of this pin is also shown in Figure 4-14.

**FIGURE 4-13: CONTINUITY INDICATOR CIRCUIT**



**FIGURE 4-14: INPUT/OUTPUT PIN SCHEMATIC**

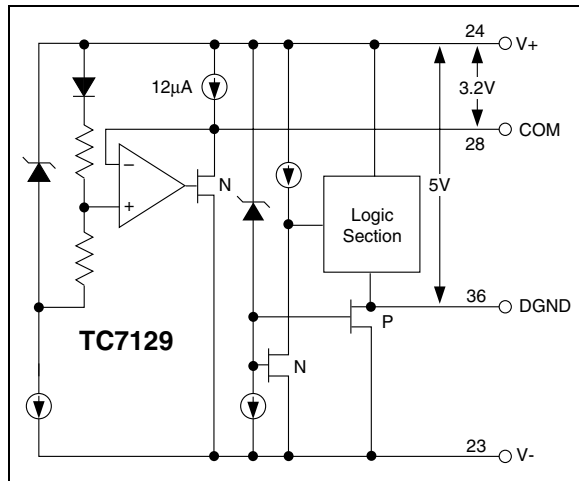


## 4.16 Common and Digital Ground

The common and digital ground (DGND) outputs are generated from internal zener diodes. The voltage between V+ and DGND is the internal supply voltage for the digital section of the TC7129. Common can source approximately 12μA; DGND has essentially no source capability (see Figure 4-15).

# TC7129

**FIGURE 4-15: DIGITAL GROUND (DGND) AND COMMON OUTPUTS**



## 4.17 Low Battery

The low battery annunciator turns on when supply voltage between  $V^-$  and  $V^+$  drops below 6.8V. The internal zener has a threshold of 6.3V. When the supply voltage drops below 6.8V, the transistor tied to  $V^-$  turns OFF, pulling the "Low Battery" point HIGH.

## 4.18 Sequence and Results Counter

A sequence counter and associated control logic provide signals that operate the analog switches in the integrator section. The comparator output from the integrator gates the results counter. The results counter is a six-section up/down decade counter, which holds the intermediate results from each successive integration.

## 4.19 Over Range and Under Range Outputs

When the results counter holds a value greater than  $\pm 19,999$ , the  $DP_4/OR$  output (Pin 20) is driven HIGH. When the results counter value is less than  $\pm 1000$ , the  $DP_3/UR$  output (Pin 21) is driven HIGH. Both signals are valid on the falling edge of  $\overline{LATCH/HOLD}$  ( $\overline{L/H}$ ) and do not change until the end of the next conversion cycle. The signals are updated at the end of each conversion, unless the  $\overline{L/H}$  input (Pin 22) is held HIGH. Pins 20 and 21 can also be used as inputs for external control of decimal points 3 and 4. Figure 4-14 shows a schematic of the input/output nature of these pins.

## 4.20 LATCH/Hold

The  $\overline{L/H}$  output goes LOW during the last 100 cycles of each conversion. This pulse latches the conversion data into the display driver section of the TC7129. This pin can also be used as an input. When driven HIGH, the display will not be updated; the previous reading is displayed. When driven LOW, the display reading is not latched; the sequence counter reading will be displayed. Since the counter is counting much faster than the backplanes are being updated, the reading shown in this mode is somewhat erratic.

## 4.21 Display Driver

The TC7129 drives a triplexed LCD with three backplanes. The LCD can include decimal points, polarity sign, and annunciators for continuity and low battery. Figure 4-16 shows the assignment of the display segments to the backplanes and segment drive lines. The backplane drive frequency is obtained by dividing the oscillator frequency by 1200. This results in a backplane drive frequency of 100Hz for 60Hz operation (120kHz crystal) and 83.3Hz for 50Hz operation (100kHz crystal).

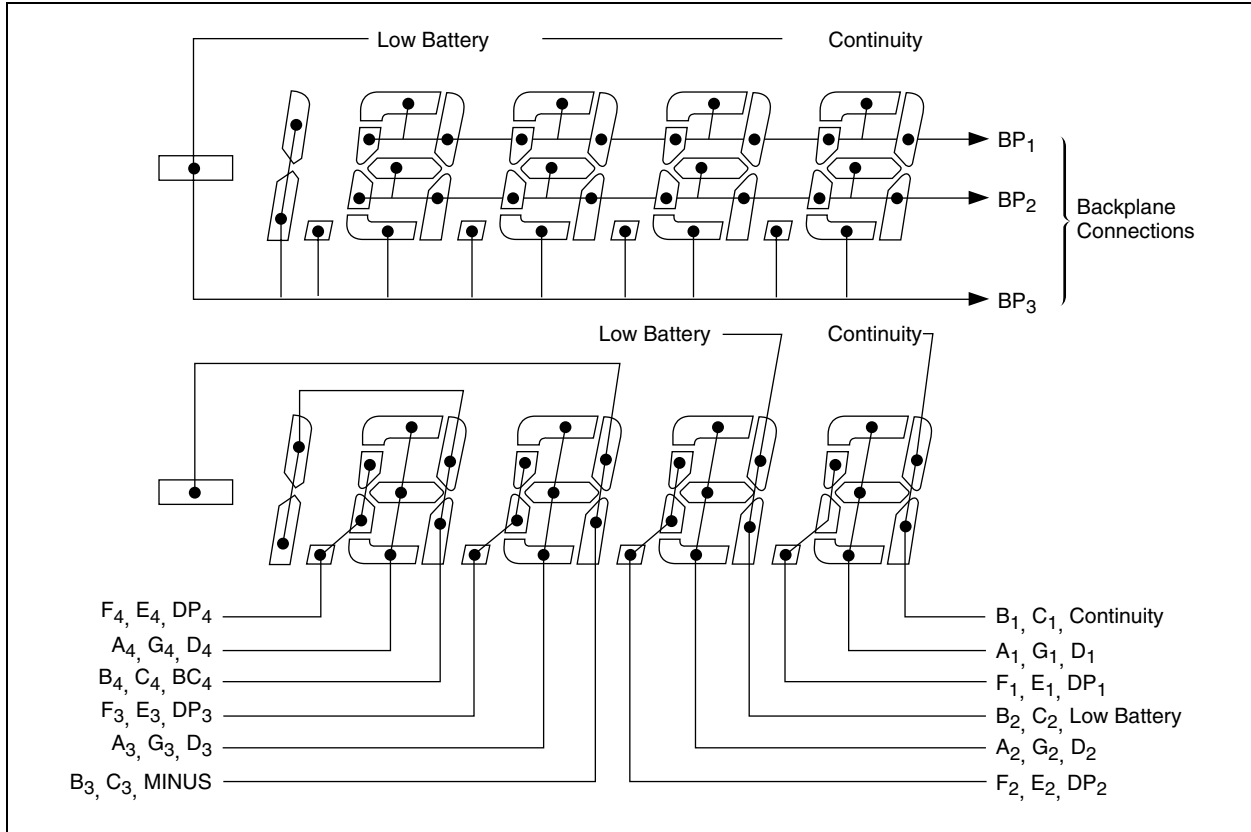
Backplane waveforms are shown in Figure 4-17. These appear on outputs  $BP_1$ ,  $BP_2$ ,  $BP_3$  (Pins 16, 17, and 18). They remain the same, regardless of the segments being driven.

Other display output lines (Pins 4 through 15) have waveforms that vary depending on the displayed values. Figure 4-18 shows a set of waveforms for the A, G, D outputs (Pins 5, 8, 11, and 14) for several combinations of "ON" segments.

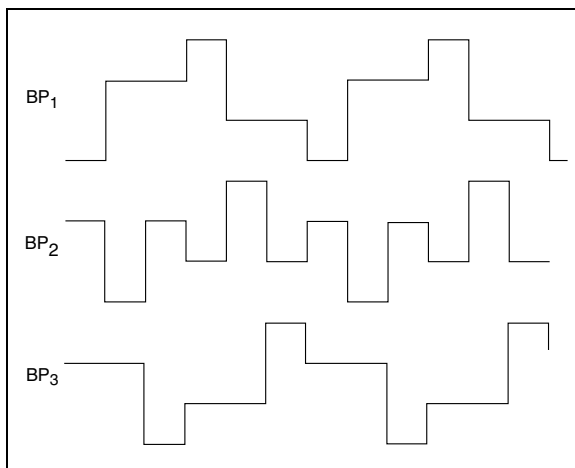
The ANNUNCIATOR DRIVE output (Pin 3) is a square wave, running at the backplane frequency (100Hz or 83.3Hz) with a peak-to-peak voltage equal to DGND voltage. Connecting an annunciator to Pin 3 turns it ON; connecting it to its backplane turns it OFF.



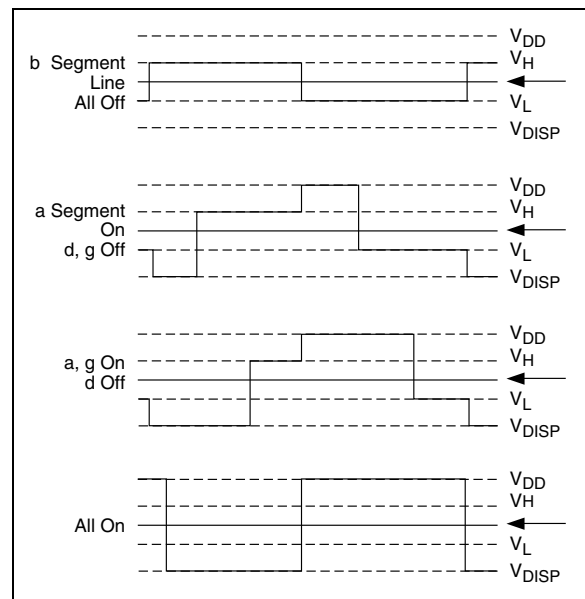
**FIGURE 4-16: DISPLAY SEGMENT ASSIGNMENTS**



**FIGURE 4-17: BACKPLANE WAVEFORMS**



**FIGURE 4-18: TYPICAL DISPLAY OUTPUT WAVEFORMS**



# TC7129

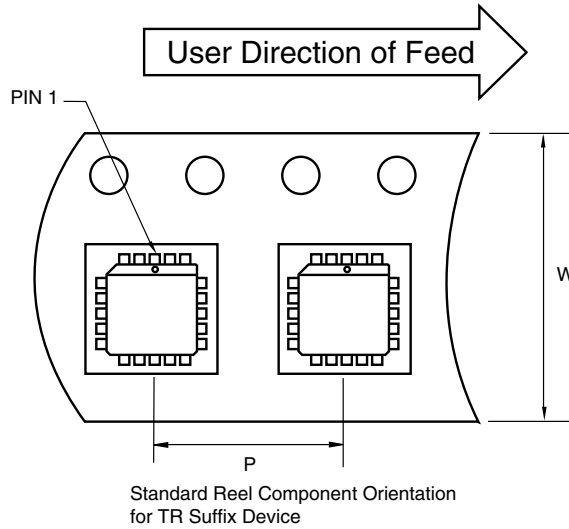
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

Package marking data not available a this time.

### 5.2 Taping Forms

#### Component Taping Orientation for 44-Pin PLCC Devices

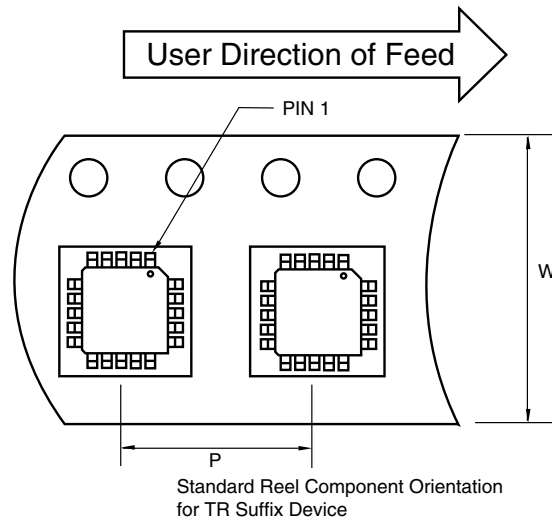


#### Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
44-Pin PLCC	32 mm	24 mm	500	13 in

**Note:** Drawing does not represent total number of pins.

#### Component Taping Orientation for 44-Pin PQFP Devices



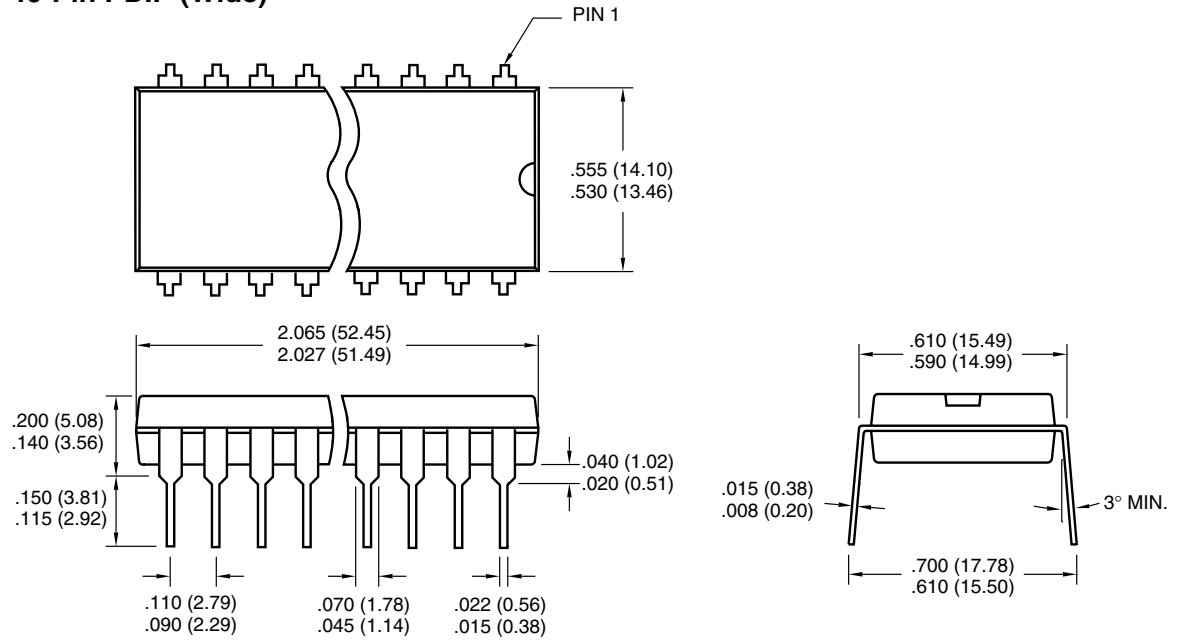
#### Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
44-Pin PQFP	24 mm	16 mm	500	13 in

**Note:** Drawing does not represent total number of pins.

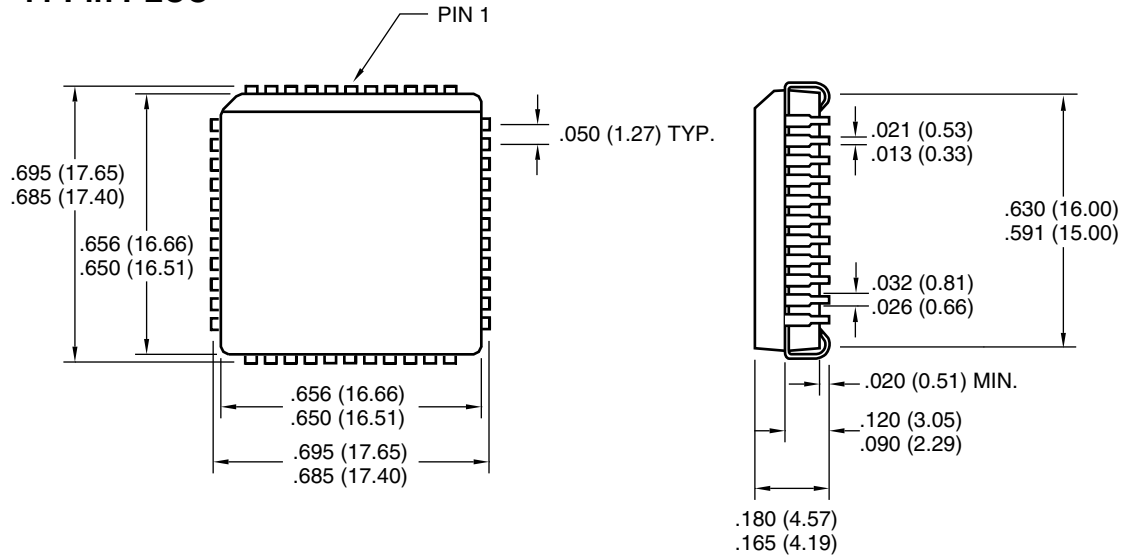
## 5.3 Package Dimensions

### 40-Pin PDIP (Wide)



Dimensions: inches (mm)

### 44-Pin PLCC

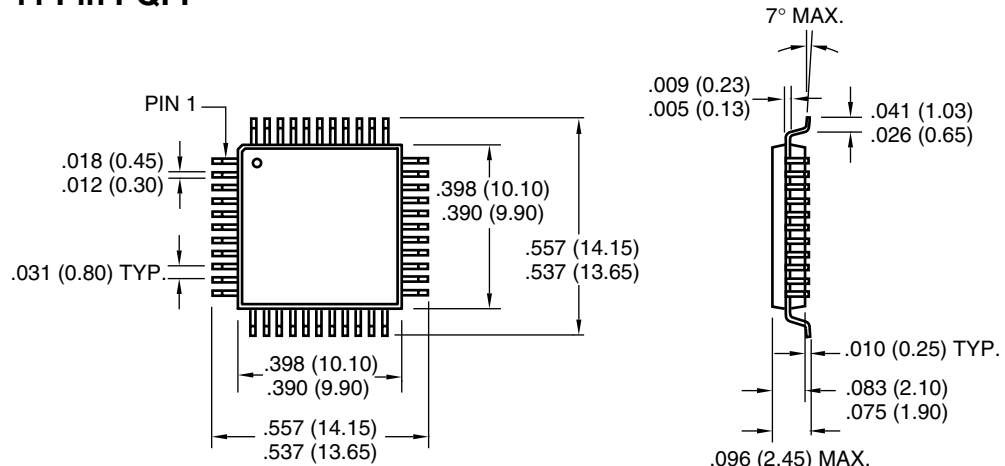


Dimensions: inches (mm)

# TC7129

## 5.3 Package Dimensions (Continued)

### 44-Pin PQFP



Dimensions: inches (mm)

NOTES:

## SALES AND SUPPORT

### **Data Sheets**

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site ([www.microchip.com](http://www.microchip.com))

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

### **New Customer Notification System**

Register on our web site ([www.microchip.com/cn](http://www.microchip.com/cn)) to receive the most current information on our products.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

## Trademarks

The Microchip name and logo, the Microchip logo, FilterLab, KEELOQ, microID, MPLAB, PIC, PICmicro, PICMASTER, PICSTART, PRO MATE, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

dsPIC, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, MXDEV, PICC, PICDEM, PICDEM.net, rfPIC, Select Mode and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A.

Serialized Quick Turn Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2002, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.



*Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.*



# MICROCHIP

## WORLDWIDE SALES AND SERVICE

### AMERICAS

#### Corporate Office

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200 Fax: 480-792-7277  
Technical Support: 480-792-7627  
Web Address: <http://www.microchip.com>

#### Rocky Mountain

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7966 Fax: 480-792-7456

#### Atlanta

500 Sugar Mill Road, Suite 200B  
Atlanta, GA 30350  
Tel: 770-640-0034 Fax: 770-640-0307

#### Boston

2 Lan Drive, Suite 120  
Westford, MA 01886  
Tel: 978-692-3848 Fax: 978-692-3821

#### Chicago

333 Pierce Road, Suite 180  
Itasca, IL 60143  
Tel: 630-285-0071 Fax: 630-285-0075

#### Dallas

4570 Westgrove Drive, Suite 160  
Addison, TX 75001  
Tel: 972-818-7423 Fax: 972-818-2924

#### Detroit

Tri-Atria Office Building  
32255 Northwestern Highway, Suite 190  
Farmington Hills, MI 48334  
Tel: 248-538-2250 Fax: 248-538-2260

#### Kokomo

2767 S. Albright Road  
Kokomo, Indiana 46902  
Tel: 765-864-8360 Fax: 765-864-8387

#### Los Angeles

18201 Von Karman, Suite 1090  
Irvine, CA 92612  
Tel: 949-263-1888 Fax: 949-263-1338

#### New York

150 Motor Parkway, Suite 202  
Hauppauge, NY 11788  
Tel: 631-273-5305 Fax: 631-273-5335

#### San Jose

Microchip Technology Inc.  
2107 North First Street, Suite 590  
San Jose, CA 95131  
Tel: 408-436-7950 Fax: 408-436-7955

#### Toronto

6285 Northam Drive, Suite 108  
Mississauga, Ontario L4V 1X5, Canada  
Tel: 905-673-0699 Fax: 905-673-6509

### ASIA/PACIFIC

#### Australia

Microchip Technology Australia Pty Ltd  
Suite 22, 41 Rawson Street  
Epping 2121, NSW  
Australia  
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

#### China - Beijing

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Beijing Liaison Office  
Unit 915  
Bei Hai Wan Tai Bldg.  
No. 6 Chaoyangmen Beidajie  
Beijing, 100027, No. China  
Tel: 86-10-85282100 Fax: 86-10-85282104

#### China - Chengdu

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Chengdu Liaison Office  
Rm. 2401, 24th Floor,  
Ming Xing Financial Tower  
No. 88 TIDU Street  
Chengdu 610016, China  
Tel: 86-28-6766200 Fax: 86-28-6766599

#### China - Fuzhou

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Fuzhou Liaison Office  
Unit 28F, World Trade Plaza  
No. 71 Wusi Road  
Fuzhou 350001, China  
Tel: 86-591-7503506 Fax: 86-591-7503521

#### China - Shanghai

Microchip Technology Consulting (Shanghai)  
Co., Ltd.  
Room 701, Bldg. B  
Far East International Plaza  
No. 317 Xian Xia Road  
Shanghai, 200051  
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

#### China - Shenzhen

Microchip Technology Consulting (Shanghai)  
Co., Ltd., Shenzhen Liaison Office  
Rm. 1315, 13/F, Shenzhen Kerry Centre,  
Renminnan Lu  
Shenzhen 518001, China  
Tel: 86-755-2350361 Fax: 86-755-2366086

#### Hong Kong

Microchip Technology Hongkong Ltd.  
Unit 901-6, Tower 2, Metroplaza  
223 Hing Fong Road  
Kwai Fong, N.T., Hong Kong  
Tel: 852-2401-1200 Fax: 852-2401-3431

#### India

Microchip Technology Inc.  
India Liaison Office  
Divyasree Chambers  
1 Floor, Wing A (A3/A4)  
No. 11, O'Shaugnessey Road  
Bangalore, 560 025, India  
Tel: 91-80-2290061 Fax: 91-80-2290062

### Japan

Microchip Technology Japan K.K.  
Benex S-1 6F  
3-18-20, Shinyokohama  
Kohoku-Ku, Yokohama-shi  
Kanagawa, 222-0033, Japan  
Tel: 81-45-471-6166 Fax: 81-45-471-6122

### Korea

Microchip Technology Korea  
168-1, Youngbo Bldg. 3 Floor  
Samsung-Dong, Kangnam-Ku  
Seoul, Korea 135-882  
Tel: 82-2-554-7200 Fax: 82-2-558-5934

### Singapore

Microchip Technology Singapore Pte Ltd.  
200 Middle Road  
#07-02 Prime Centre  
Singapore, 188980  
Tel: 65-6334-8870 Fax: 65-6334-8850

### Taiwan

Microchip Technology Taiwan  
11F-3, No. 207  
Tung Hua North Road  
Taipei, 105, Taiwan  
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

### EUROPE

#### Denmark

Microchip Technology Nordic ApS  
Regus Business Centre  
Lautrup høj 1-3  
Ballerup DK-2750 Denmark  
Tel: 45 4420 9895 Fax: 45 4420 9910

#### France

Microchip Technology SARL  
Parc d'Activite du Moulin de Massy  
43 Rue du Saule Trapu  
Batiment A - 1er Etage  
91300 Massy, France  
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

#### Germany

Microchip Technology GmbH  
Gustav-Heinemann Ring 125  
D-81739 Munich, Germany  
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

#### Italy

Microchip Technology SRL  
Centro Direzionale Colleoni  
Palazzo Taurus 1 V. Le Colleoni 1  
20041 Agrate Brianza  
Milan, Italy  
Tel: 39-039-65791-1 Fax: 39-039-6899883

#### United Kingdom

Arizona Microchip Technology Ltd.  
505 Eskdale Road  
Winnersh Triangle  
Wokingham  
Berkshire, England RG41 5TU  
Tel: 44 118 921 5869 Fax: 44-118 921-5820

03/01/02

