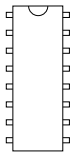
A6821

Data Sheet
26185.112B

DABiC-5 8-Bit Serial Input Latched Sink Drivers

Package A
16-pin DIP



Package LW
16-pin Wide Body SOIC

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{OUT} ..... **50 V**
Logic Supply Voltage, V_{DD} ..... **7 V**
Input Voltage Range, V_{IN} ..... **–0.3 V to V_{DD} +0.3 V**
Continuous Output Current (each output), I_{OUT} ... **500 mA**
Package Power Dissipation, P_D
A6821SA/A6821EA..... **2.1 W**
A6821SLW..... **1.5 W**
Operating Temperature Range
Ambient Temperature, T_A ..... **–20°C to +85°C**
Storage Temperature, T_S ..... **–55°C to +150°C**

Caution: CMOS devices have input-static protection, but are susceptible to damage when exposed to extremely high static-electrical charges.

A merged combination of bipolar and MOS technology gives these devices an interface flexibility beyond the reach of standard logic buffers and power driver arrays. Typical applications include driving multiplexed LED displays or incandescent lamps.

The A6821 has an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sinking Darlington output drivers.

The CMOS inputs are compatible with standard CMOS logic levels. TTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

The A6821SA is furnished in a standard 16-pin plastic DIP. The A6821EA is a 16-pin plastic DIP, capable of operation from -40°C to +85°C. The A6821SLW is a 16-lead wide-body SOIC, for surface-mount applications. These devices are lead (Pb) free, with 100% matte tin plated leadframes.

FEATURES

- 3.3 V to 5 V logic supply range
- Power on reset (POR)
- To 10 MHz data input rate
- CMOS, TTL compatible
- –40°C operation available
- Schmitt trigger inputs for improved noise immunity
- Low-power CMOS logic and latches
- High-voltage current-sink outputs
- Internal pull-up/pull down resistors

APPLICATIONS

- Multiplexed LED displays
- Incandescent lamps

Use the following complete part numbers when ordering:

Part Number	Package	Ambient
A6821SA-T	16-pin DIP	–20°C to +85°C
A6821EA-T	16-pin DIP	–40°C to +85°C
A6821SLW-T	16-pin wide body SOIC	–20°C to +85°C

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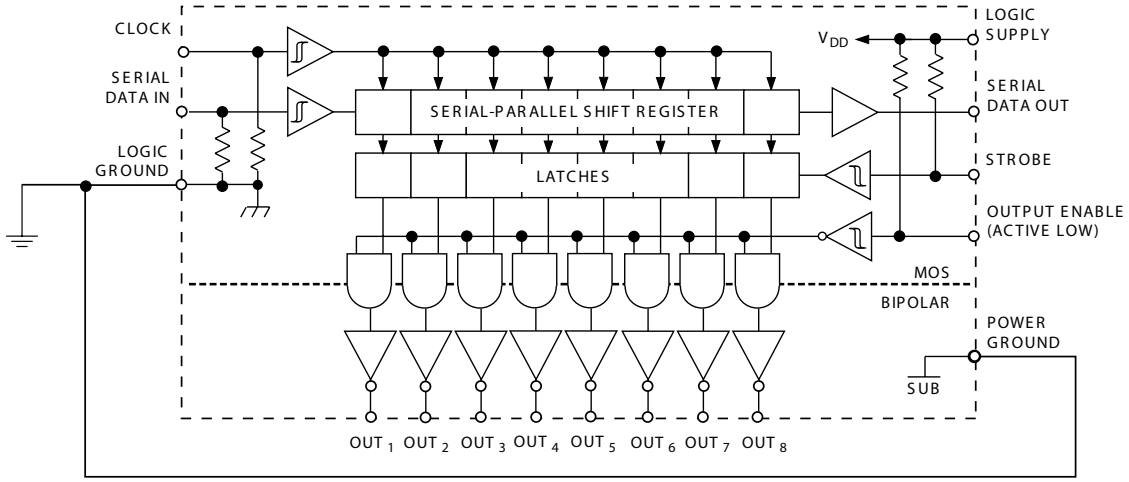
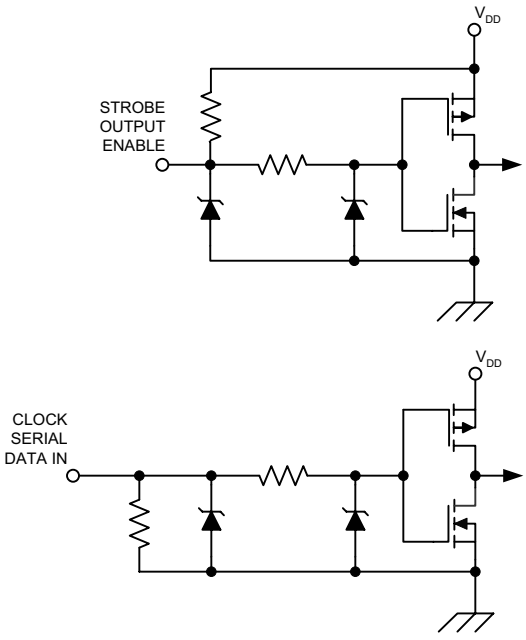
DABiC-5 8-Bit Serial Input Latched Sink Drivers

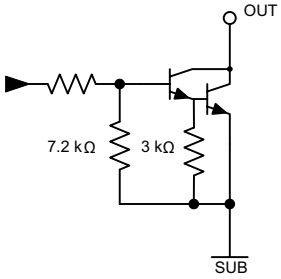
Functional Block Diagram



Typical Input Circuits



Typical Output Driver



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A6821
DABiC-5 8-Bit Serial Input Latched Sink Drivers

ELECTRICAL CHARACTERISTICS[1] Unless otherwise noted: T_A = 25°C, logic supply operating voltage V_{dd} = 3.0 V to 5.5 V

Characteristic	Symbol	Test Conditions	V_{dd} = 3.3 V			V_{dd} = 5 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 50 V	–	–	10	–	–	10	µA
Collector–Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100 mA	–	–	1.1	–	–	1.1	V
		I_{OUT} = 200 mA	–	–	1.3	–	–	1.3	V
		I_{OUT} = 350 mA	–	–	1.6	–	–	1.6	V
Input Voltage	$V_{IN(1)}$		2.2	–	–	3.3	–	–	V
	$V_{IN(0)}$		–	–	1.1	–	–	1.7	V
Input Resistance	R_{IN}		50	–	–	50	–	–	kΩ
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = –200 µA	2.8	3.05	–	4.5	4.75	–	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	–	0.15	0.3	–	0.15	0.3	V
Maximum Clock Frequency[2]	f_c		10	–	–	10	–	–	MHz
Logic Supply Current	$I_{DD(1)}$	One output on, OE = L, ST = H	–	–	2.0	–	–	2.0	mA
	$I_{DD(0)}$	All outputs off, OE = H, ST = H, P1 through P8 = L	–	–	100	–	–	100	µA
Output Enable-to-Output Delay	$t_{dis(BQ)}$	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
	$t_{en(BQ)}$	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
Strobe-to-Output Delay	$t_{p(STH-QL)}$	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
	$t_{p(STH-QH)}$	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
Output Fall Time	t_f	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
Output Rise Time	t_r	V_{CC} = 50 V, R1 = 500 Ω, C1 ≤ 30 pF	–	–	1.0	–	–	1.0	µs
Clock-to-Serial Data Out Delay	$t_{p(CH-SQX)}$	I_{OUT} = ±200 µA	–	50	–	–	50	–	ns

[1]Positive (negative) current is defined as conventional current going into (coming out of) the specified device pin.
[2]Operation at a clock frequency greater than the specified minimum value is possible but not warranteed.

Truth Table

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ... I_8	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ... I_8	Output Enable Input	Output Contents I_1 I_2 I_3 ... I_8
H	⌐	H R_1 R_2 ... R_7	R_7				
L	⌐	L R_1 R_2 ... R_7	R_7				
X	⌙	R_1 R_2 R_3 ... R_8	R_8				
		X X X ... X	X	L	R_1 R_2 R_3 ... R_8		
		P_1 P_2 P_3 ... P_8	P_8	H	P_1 P_2 P_3 ... P_8	L	P_1 P_2 P_3 ... P_8
					X X X ... X	H	H H H ... H

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State
OE = Output Enable
ST = Strobe

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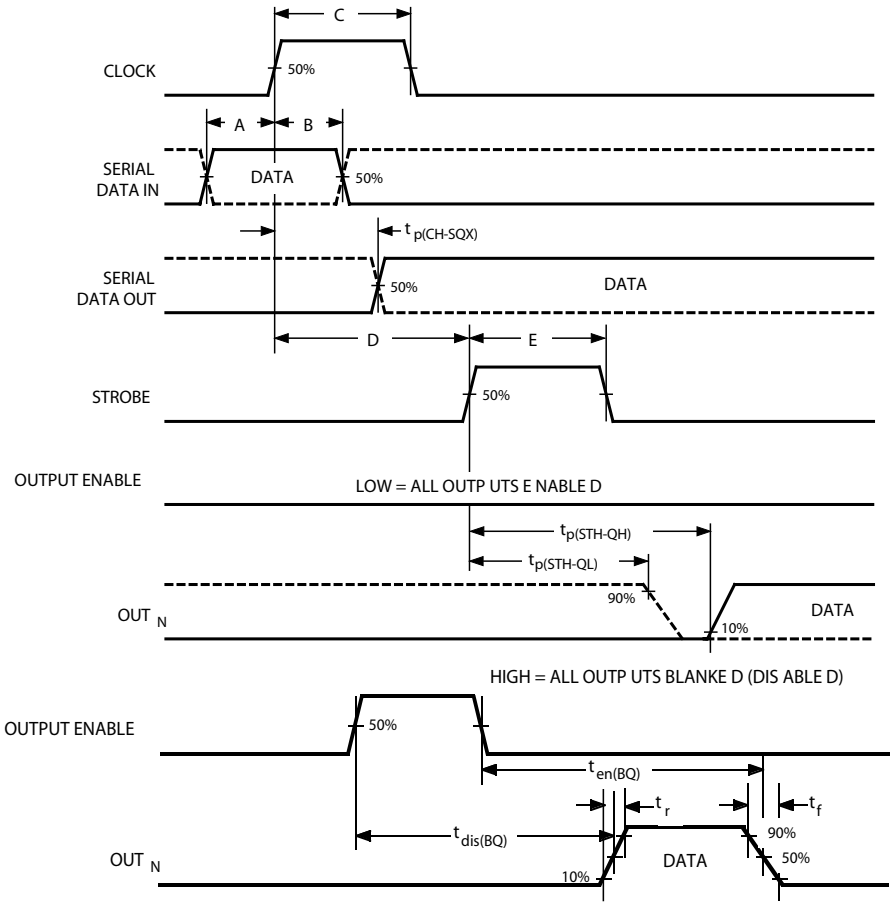
Timing Requirements and Specifications
(Logic Levels are V_{DD} and Ground)



Key	Description	Symbol	Time (ns)
A	Data Active Time Before Clock Pulse (Data Set-Up Time)	$t_{su(D)}$	25
B	Data Active Time After Clock Pulse (Data Hold Time)	$t_{h(D)}$	25
C	Clock Pulse Width	$t_{w(CH)}$	50
D	Time Between Clock Activation and Strobe	$t_{su(C)}$	100
E	Strobe Pulse Width	$t_{w(STH)}$	50

NOTE: Timing is representative of a 10 MHz clock. Higher speeds may be attainable; operation at high temperatures will reduce the specified maximum clock frequency.

Powering-on with the inputs in the low state ensures that the registers and latches power-on in the low state (POR).

Serial Data present at the input is transferred to the shift register on the logical 0 to logical 1 transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF). The information stored in the latches or shift register is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

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Maximum Allowable Duty Cycle, I_{OUT} = 200 mA, V_{DD} = 5 V

Number of Outputs ON	Ambient Temperature				
	25°C	40°C	50°C	60°C	70°C
A6821SA/A6821EA					
8	90%	79%	72%	65%	57%
7	100%	90%	82%	74%	65%
6	100%	100%	96%	86%	76%
5	100%	100%	100%	100%	91%
4	100%	100%	100%	100%	100%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%
A6821SLW					
8	67%	59%	54%	49%	43%
7	77%	68%	62%	56%	49%
6	90%	79%	72%	65%	57%
5	100%	95%	86%	78%	68%
4	100%	100%	100%	98%	86%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

Terminal List Table

Name	Description	Pin
CLK	Clock	1
	Serial Data In	2
	Logic Ground*	3
VDD	Logic Supply	4
	Serial Data Out	5
ST	Strobe	6
$\overline{OE}$	Output Enable (active low)	7
SUB	Power Ground*	8
OUT_8	Serial Data Output	9
OUT_7	Serial Data Output	10
OUT_6	Serial Data Output	11
OUT_5	Serial Data Output	12
OUT_4	Serial Data Output	13
OUT_3	Serial Data Output	14
OUT_2	Serial Data Output	15
OUT_1	Serial Data Output	16

* There is an indeterminate resistance between logic ground and power ground. For proper operation, these terminals must be externally connected together.

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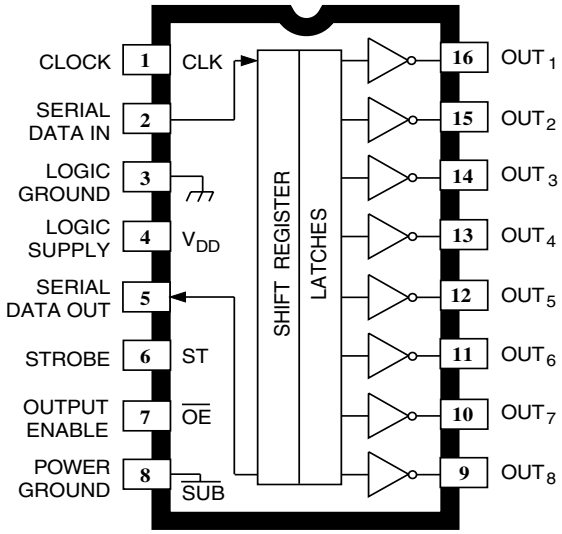
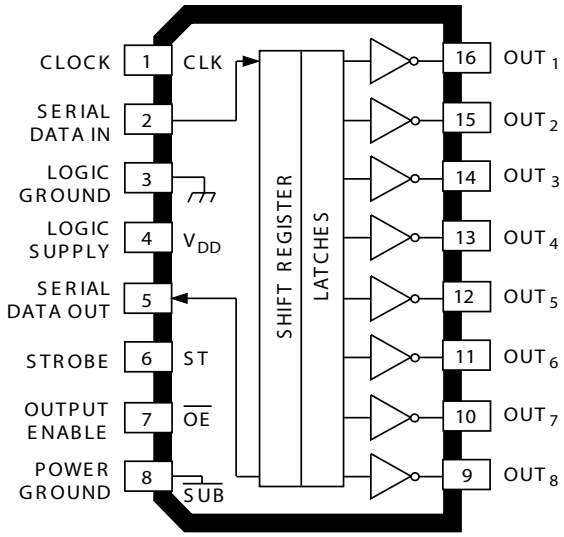
Package A
16-pin DIP



Package LW
16-pin Wide Body SOIC



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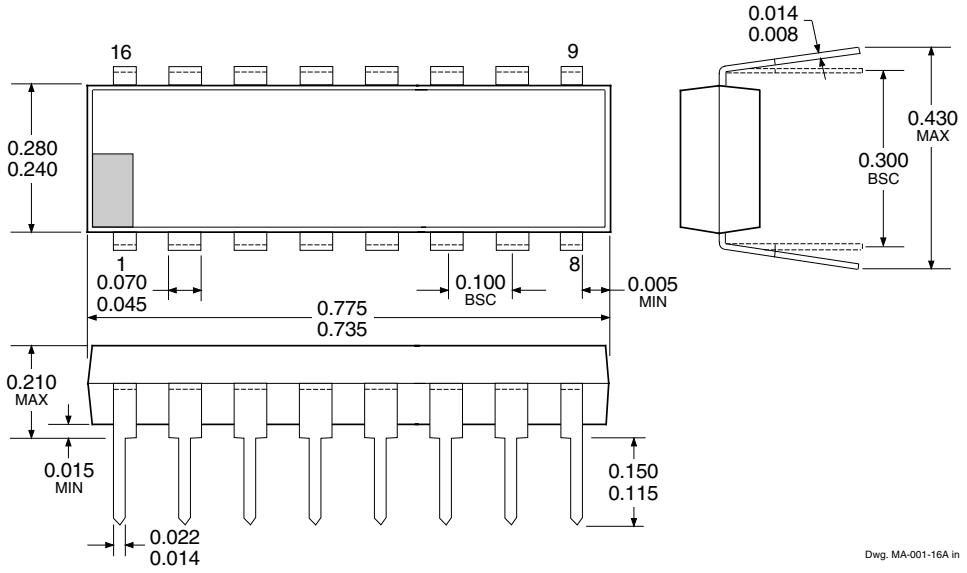
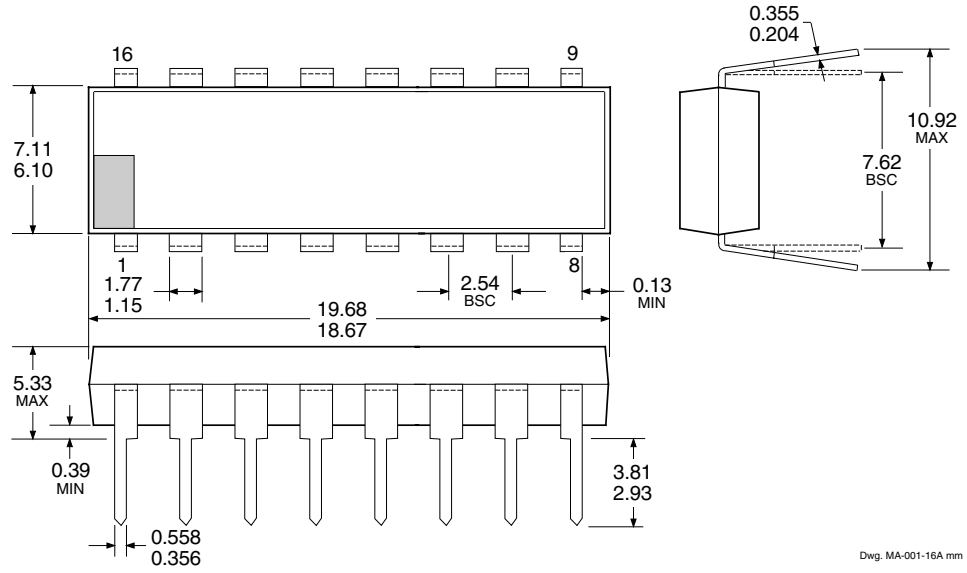
Package A
16-pin DIP

Dimensions in Inches
(controlling dimensions)



Dimensions in Millimeters
(for reference only)



NOTES: 1. Lead thickness is measured at seating plane or below.
2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.

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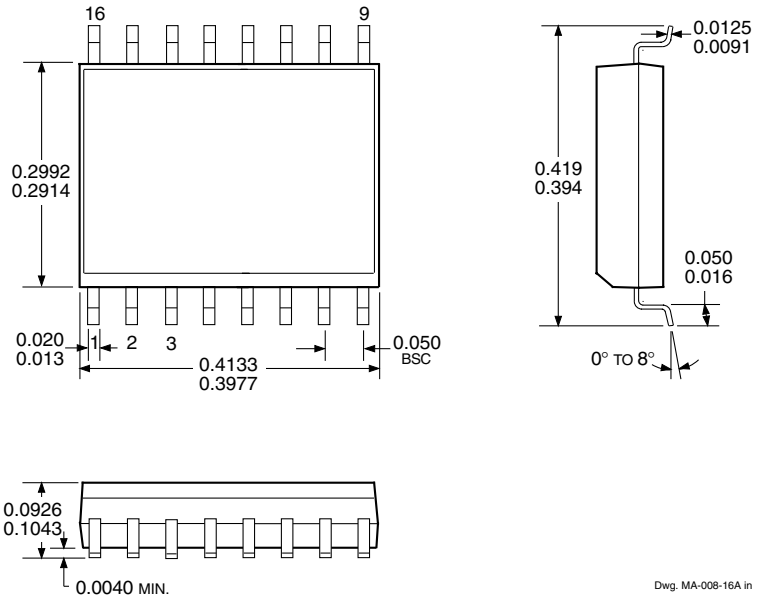
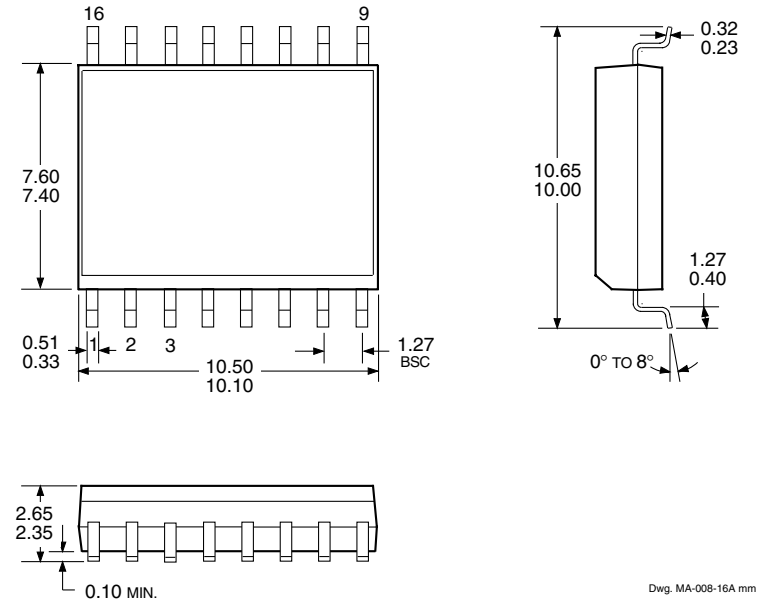
Package LW
16-pin Wide Body SOIC

Dimensions in Inches
(for reference only)



Dwg. MA-008-16A in

Dimensions in Millimeters
(controlling dimensions)



Dwg. MA-008-16A mm

NOTES: 1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.

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MIC5821/5822

8-Bit Serial-Input Latched Drivers

Final Information

General Description

BiCMOS technology gives the MIC5821/5822 family flexibility beyond the reach of standard logic buffers and power driver arrays. These devices each have an eight-bit CMOS shift register, CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sink Darlington output drivers. The 500mA outputs are suitable for use with incandescent bulbs and other moderate to high current loads. The drivers can be operated with a split supply where the negative supply is down to –20V. Except for maximum driver output voltage ratings, the MIC5821 and MIC5822 are identical.

These devices have greatly improved data-input rates. With a 5V logic supply they will typically operate faster than 5 MHz. With a 12V supply significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL and DTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

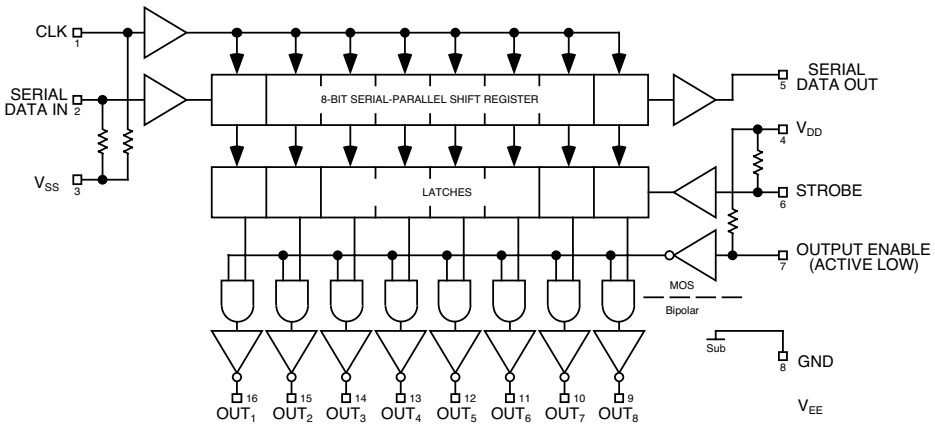
Features

- 3.3 MHz Minimum Data-Input Rate
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Down or Pull-Up Resistors
- Low-Power CMOS Logic and Latches
- High-Voltage Current-Sink Outputs
- Single or Split Supply Operation

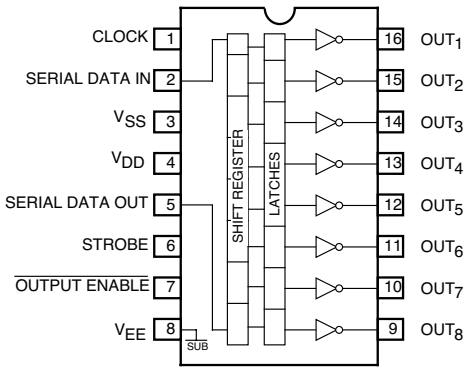
Ordering Information

Part Number		Temp Range	Package
Standard	**Pb-Free**		
MIC5821BN	MIC5821YN	–40°C to +85°C	16-Pin Plastic DIP
MIC5822BN	MIC5822YN	–40°C to +85°C	16-Pin Plastic DIP

Functional Diagram

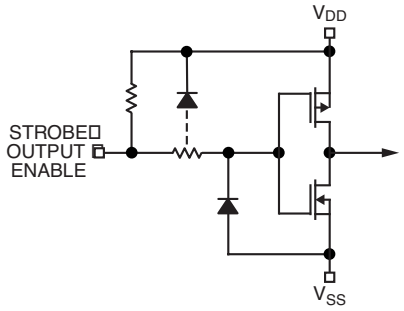


Pin Configuration



(Plastic DIP)

Typical Input Circuits

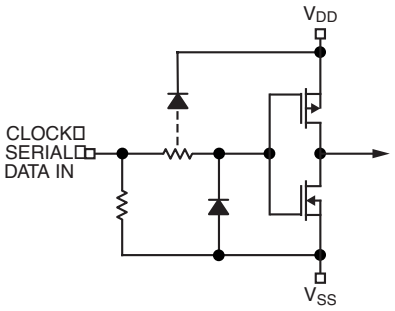


Absolute Maximum Ratings (Note 1)

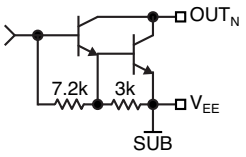
at 25°C Free-Air Temperature and V_{SS} = 0V

Output Voltage, V_{CE}	(MIC5821)	50V
	(MIC5822)	80V
Output Voltage, $V_{CE\ SUS}$	(MIC5821)(Note 3)	35V
	(MIC5822)(Note 3)	50V
Logic Supply Voltage, V_{DD}		15V
Input Voltage Range, V_{IN}		–0.3V to V_{DD} + 0.3V
$V_{DD} - V_{EE}$		25V
Emitter Supply Voltage, V_{EE}		–20V
Continuous Output Current, I_{OUT}		500mA
Package Power Dissipation, $P_{D(Note\ 1)}$		1.67W
Operating Temperature Range, T_A		–55°C to +85°C
Storage Temperature Range, T_S		–65°C to +150°C

Note 1: Derate at the rate of 16.7mW/°C above T_A = 25°C.
Note 2: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.
Note 3: For inductive load applications.
Note 4: Specification for packaged product only.



Typical Output Driver



Maximum Allowable Duty Cycle (Plastic DIP)

Number of Outputs ON (I_{OUT} = 200mA V_{DD} = 12V)	Maximum Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	73%	62%	55%	47%	40%
7	83%	71%	62%	54%	46%
6	97%	82%	72%	63%	53%
5	100%	98%	87%	75%	63%
4	100%	100%	100%	93%	79%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

Electrical Characteristics (Note 4) at T_A = 25°C V_{DD} = 5V, V_{EE} = V_{SS} = 0V (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits		
				Min.	Max.	Unit
Output Leakage Current	I_{CEX}	MIC5821	V_{OUT} = 50V		50	μA
			V_{OUT} = 50V, T_A = +70°C		100	
		MIC5822	V_{OUT} = 80V		50	
			V_{OUT} = 80V, T_A = +70°C		100	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	Both	I_{OUT} = 100mA		1.1	V
			I_{OUT} = 200mA		1.3	
			I_{OUT} = 350mA, V_{DD} = 7.0V		1.6	
Input Voltage	$V_{IN(0)}$	Both			0.8	V
	$V_{IN(1)}$	Both	V_{DD} = 12V	10.5		
			V_{DD} = 10V	8.5		
			V_{DD} = 5.0V	3.5		
Input Resistance	R_{IN}	Both	V_{DD} = 12V	50		kΩ
			V_{DD} = 10V	50		
			V_{DD} = 5.0V	50		
Supply Current	$I_{DD(ON)}$	Both	One Driver ON, V_{DD} = 12V		4.5	mA
			One Driver ON, V_{DD} = 10V		3.9	
			One Driver ON, V_{DD} = 5.0V		2.4	
			All Drivers ON, V_{DD} = 12V		16	
			All Drivers ON, V_{DD} = 10V		14	
			All Drivers ON, V_{DD} = 5.0V		8	
	$I_{DD(OFF)}$	Both	All Drivers OFF, V_{DD} = 5.0V, All Inputs = 0V		1.6	
			All Drivers OFF, V_{DD} = 12V, All Inputs= 0V		2.9	

Electrical Characteristics (Note 4) T_A = –55°C, V_{DD} = 5V, V_{SS} = V_{EE} = 0V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Unit
Output Leakage Current	I_{CEX}	V_{OUT} = 80V		50	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100mA		1.3	V
		I_{OUT} = 200mA		1.5	
		I_{OUT} = 350mA, V_{DD} = 7.0V		1.8	
Input Voltage	$V_{IN0)}$			0.8	V
	$V_{IN(1)}$	V_{DD} = 12V	10.5		
		V_{DD} = 5.0V	3.5		
Input Resistance	RIN	V_{DD} = 12V	35		kΩ
		V_{DD} = 10V	35		
		V_{DD} = 5.0V	35		
Supply Current	$I_{DD(ON)}$	One Driver ON, V_{DD} = 12V		5.5	mA
		One Driver ON, V_{DD} = 10V		4.5	
		One Driver ON, V_{DD} = 5.0V		3.0	
		All Drivers ON, V_{DD} = 12V		16	
		All Drivers ON, V_{DD} = 10V		14	
		All Drivers ON, V_{DD} = 5.0V		10	
	$I_{DD(OFF)}$	All Drivers OFF, V_{DD} = 12V		3.5	
		All Drivers OFF, V_{DD} = 5.0V		2.0	

Electrical Characteristics (Note 4) T_A = +125°C, V_{DD} = 5V, V_{SS} = V_{EE} = 0V (unless otherwise noted)

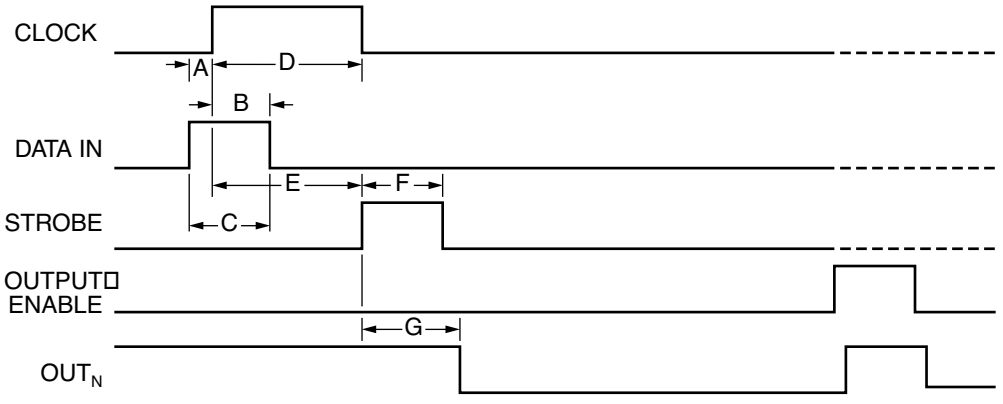
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Unit
Output Leakage Current	I_{CEX}	V_{OUT} = 80V		500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100mA		1.3	V
		I_{OUT} = 200mA		1.5	
		I_{OUT} = 350mA, V_{DD} = 7.0V		1.8	
Input Voltage	$V_{IN(0)}$			0.8	V
	$V_{IN(1)}$	V_{DD} = 12V	10.5		
		V_{DD} = 5.0V	3.5		
Input Resistance	R_{IN}	V_{DD} = 12V	50		kΩ
		V_{DD} = 10V	50		
		V_{DD} = 5.0V	50		
Supply Current	$I_{DD(ON)}$	One Driver ON, V_{DD} = 12V		4.5	mA
		One Driver ON, V_{DD} = 10V		3.9	
		One Driver ON, V_{DD} = 5.0V		2.4	
		All Drivers ON, V_{DD} = 12V		16	
		All Drivers ON, V_{DD} = 10V		14	
		All Drivers ON, V_{DD} = 5.0V		8	
	$I_{DD(OFF)}$	All Drivers OFF, V_{DD} = 12V		2.9	
		All Drivers OFF, V_{DD} = 5.0V		1.6	

MIC5821/5822 Family Truth Table

Serial Data Input	Clock Input	Shift Register Contents I_1	I_2	I_3	.....	I_8	Serial Data Output	Strobe Input	Latch Contents I_1	I_2	I_3	.....	I_8	Output Enable	Output Contents I_1	I_2	I_3	.....	I_8
H	⎍	H	R_1	R_2	.....	R_7	R_7												
L	⎍	L	R_1	R_2	.....	R_7	R_7												
X	⎎	R_1	R_2	R_3	.....	R_8	R_8												
		X	X	X	.....	X	X	L	R_1	R_2	R_3	.....	R_8						
		P_1	P_2	P_3	.....	P_8	P_8	H	P_1	P_2	P_3	.....	P_8	L	P_1	P_2	P_3	.....	P_8
									X	X	X	.....	X	H	H	H	H	.....	H

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

Timing Diagram



Timing Conditions

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS})

	V_{DD} = 5.0V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C. Minimum Data Pulse Width	150 ns
D. Minimum Clock Pulse Width	150 ns
E. Minimum Time Between Clock Activation and Strobe	300 ns
F. Minimum Strobe Pulse Width	100 ns
G. Typical Time Between Strobe Activation and Output Transition	500 ns

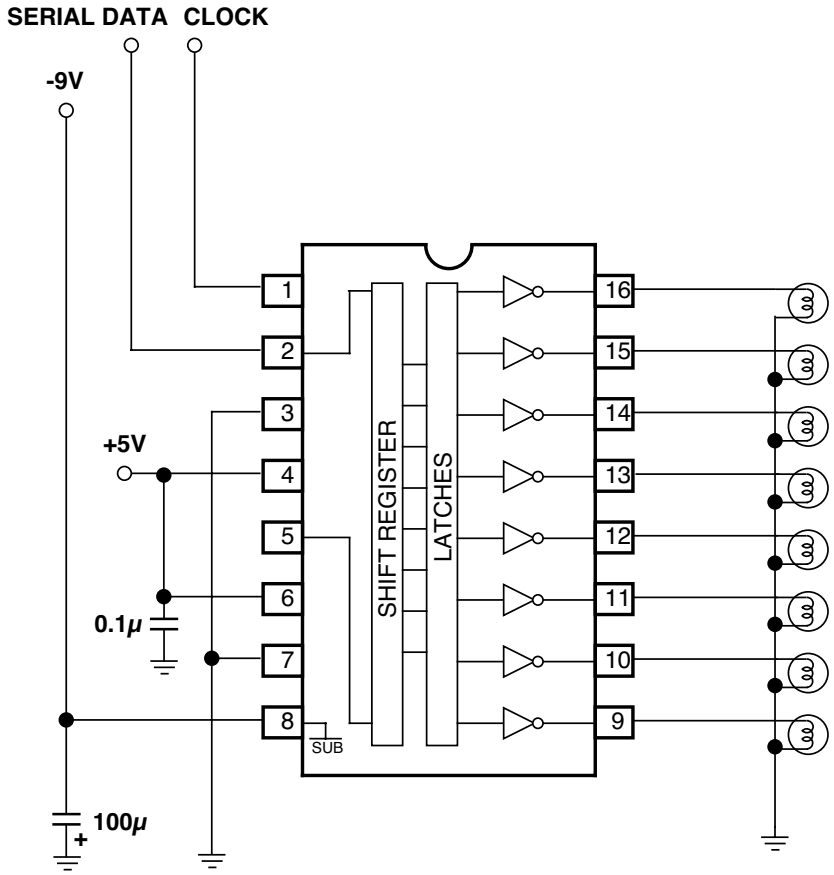
SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial entry.

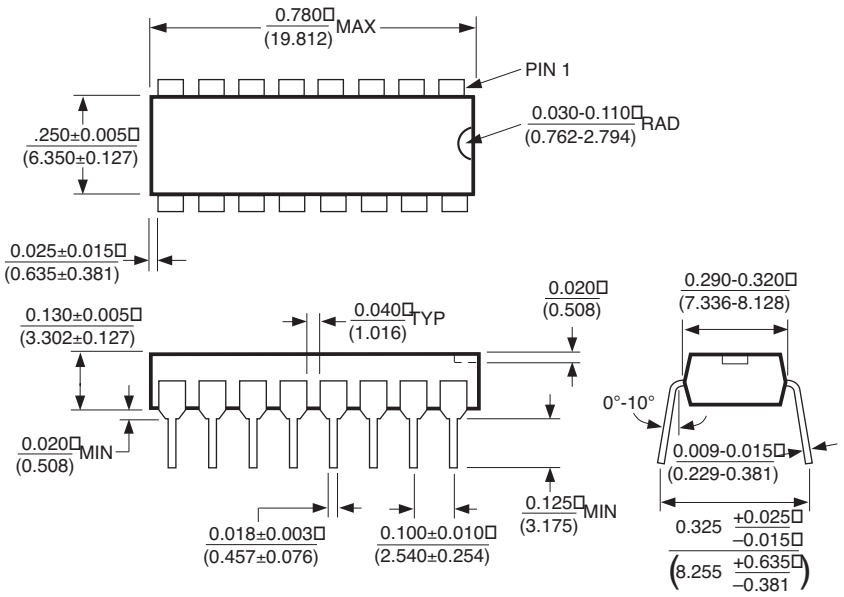
When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

Typical Applications

MIC5822 Level Shifting Lamp Driver with Darlington Emitters Tied to a Negative Supply



Package Information



16-Pin Plastic DIP (N)

MICREL INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB http://www.micrel.com

A5821

BiMOS II 8-Bit Serial Input Latched Driver

Discontinued Product

These parts are no longer in production The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: October 31, 2005

Recommended Substitutions:

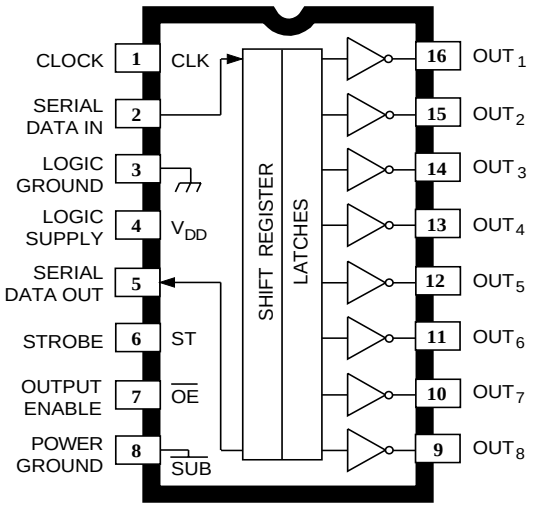
For new customers or new applications, refer to the A6821.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

5821

Data Sheet
26185.12F

BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVERS



Dwg. PP-026A

Note the DIP package and the SOIC package are electrically identical and share common terminal number assignments.

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature

Output Voltage, V_{OUT} ..... **50 V**
Logic Supply Voltage, V_{DD} ..... **15 V**
Input Voltage Range,
V_{IN} ..... **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current,
I_{OUT} ..... **500 mA**
Package Power Dissipation, P_D
Package Code 'A' ..... **2.1 W**
Package Code 'LW' ..... **1.5 W**
Operating Temperature Range,
T_A ..... **-20°C to +85°C**
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

A merged combination of bipolar and MOS technology gives these devices an interface flexibility beyond the reach of standard logic buffers and power driver arrays. The UCN5821A and UCN5821LW each have an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sinking Darlington output drivers.

BiMOS II devices have much higher data-input rates than the original BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS and NMOS logic levels. TTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

The UCN5821A are furnished in a standard 16-pin plastic DIP; the UCN5821LW are in a 16-lead wide-body SOIC for surface-mount applications. The UCN5821A is also available for operation from -40°C to +85°C. To order, change the prefix from 'UCN' to 'UCQ'.

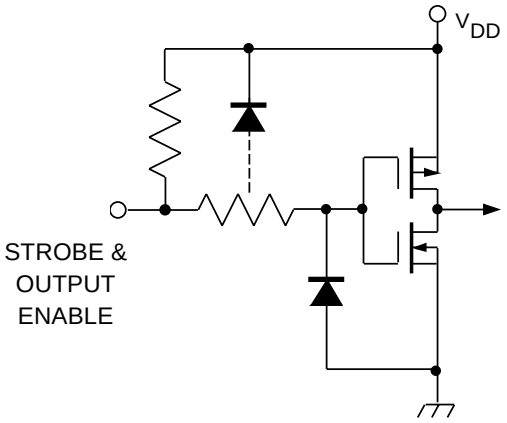
FEATURES

- To 3.3 MHz Data Input Rate
- CMOS, NMOS, TTL Compatible
- Internal Pull-Down Resistors
- Low-Power CMOS Logic & Latches
- High-Voltage Current-Sink Outputs
- Automotive Capable

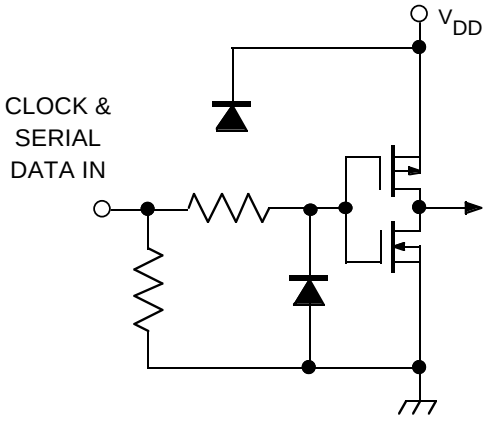
Always order by complete part number, e.g., **UCN5821A**.

5821
8-BIT SERIAL-INPUT, LATCHED DRIVERS

TYPICAL INPUT CIRCUITS

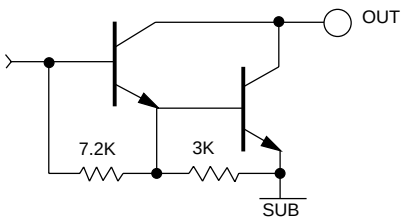


Dwg. EP-010-3



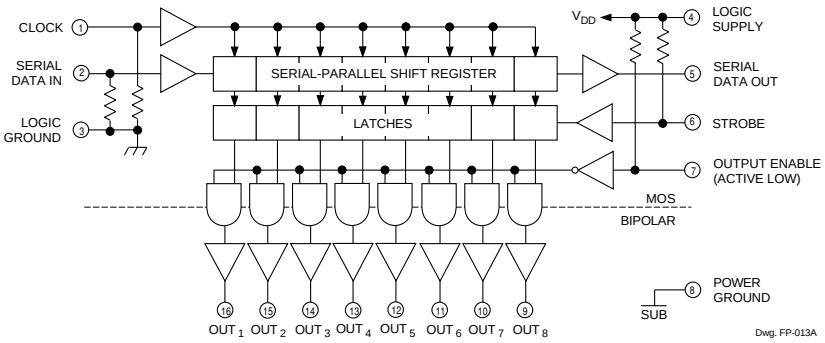
Dwg. EP-010-4A

TYPICAL OUTPUT DRIVER



Dwg. No. A-14,314

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-013A

NOTE — There is an indeterminate resistance between logic ground and power ground. For proper operation, these terminals must be externally connected together.

Number of Outputs ON (I_{OUT} = 200 mA V_{DD} = 12 V)	UCN5821A Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	90%	79%	72%	65%	57%
7	100%	90%	82%	74%	65%
6	100%	100%	96%	86%	76%
5	100%	100%	100%	100%	91%
4	100%	100%	100%	100%	100%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

Number of Outputs ON (I_{OUT} = 200 mA V_{DD} = 12 V)	UCN5821LW Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	67%	59%	54%	49%	43%
7	77%	68%	62%	56%	49%
6	90%	79%	72%	65%	57%
5	100%	95%	86%	78%	68%
4	100%	100%	100%	98%	86%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

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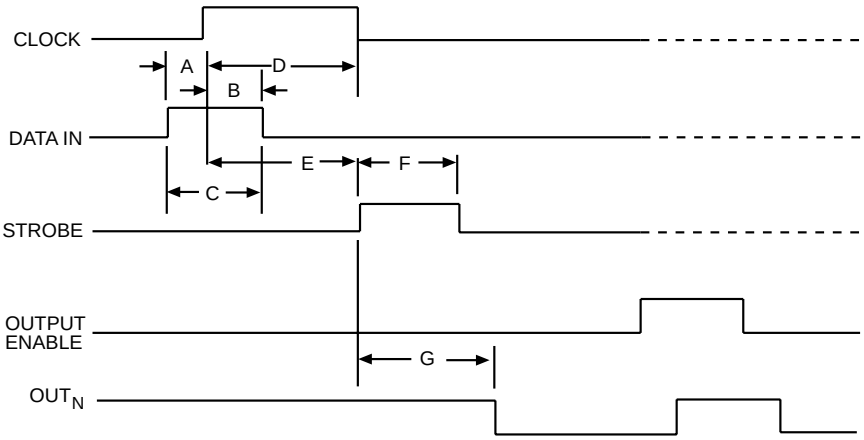
Worcester, Massachusetts 01615-0036 (508) 853-5000

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 50 V	—	50	µA
		V_{OUT} = 50 V, T_A = +70°C	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100 mA	—	1.1	V
		I_{OUT} = 200 mA	—	1.3	V
		I_{OUT} = 350 mA, V_{DD} = 7.0 V	—	1.6	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	V
		V_{DD} = 5.0 V	3.5	—	V
Input Resistance	r_{IN}	V_{DD} = 12 V	50	—	kΩ
		V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$	One Driver ON, V_{DD} = 12 V	—	4.5	mA
		One Driver ON, V_{DD} = 10 V	—	3.9	mA
		One Driver ON, V_{DD} = 5.0 V	—	2.4	mA
	$I_{DD(OFF)}$	V_{DD} = 5.0 V, All Drivers OFF, All Inputs = 0 V	—	1.6	mA
		V_{DD} = 12 V, All Drivers OFF, All Inputs = 0 V	—	2.9	mA

5821
8-BIT SERIAL-INPUT, LATCHED DRIVERS



Dwg. No. A-12,627

TIMING CONDITIONS
(V_{DD} = 5.0 V, T_A = +25°C, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) ..... **75 ns**

B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... **75 ns**

C. Minimum Data Pulse Width ..... **150 ns**

D. Minimum Clock Pulse Width ..... **150 ns**

E. Minimum Time Between Clock Activation and Strobe ..... **30 ns**

F. Minimum Strobe Pulse Width ..... **100 ns**

G. Typical Time Between Strobe Activation and Output Transition ..... **1.0 µs**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ..... I_8	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ..... I_8	Output Enable	Output Contents I_1 I_2 I_3 ..... I_8
H	⌐	H R_1 R_2 ..... R_7	R_7				
L	⌐	L R_1 R_2 ..... R_7	R_7				
X	¬	R_1 R_2 R_3 ..... R_8	R_8				
		X X X X	X	L	R_1 R_2 R_3 ..... R_8		
		P_1 P_2 P_3 ..... P_8	P_8	H	P_1 P_2 P_3 ..... P_8	L	P_1 P_2 P_3 ..... P_8
					X X X X	H	H H H ..... H

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

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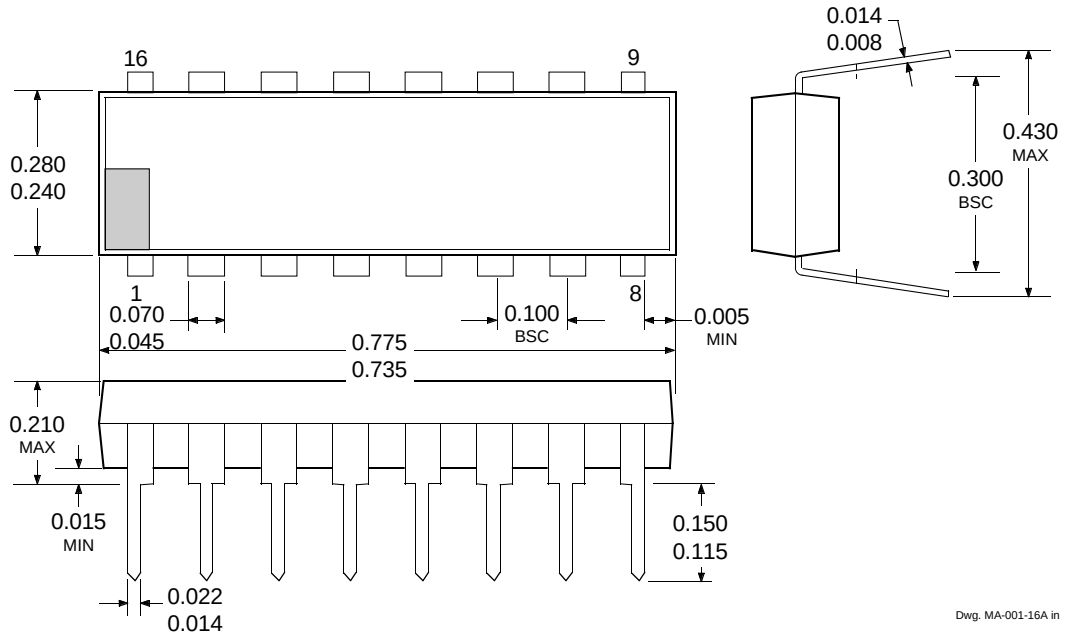
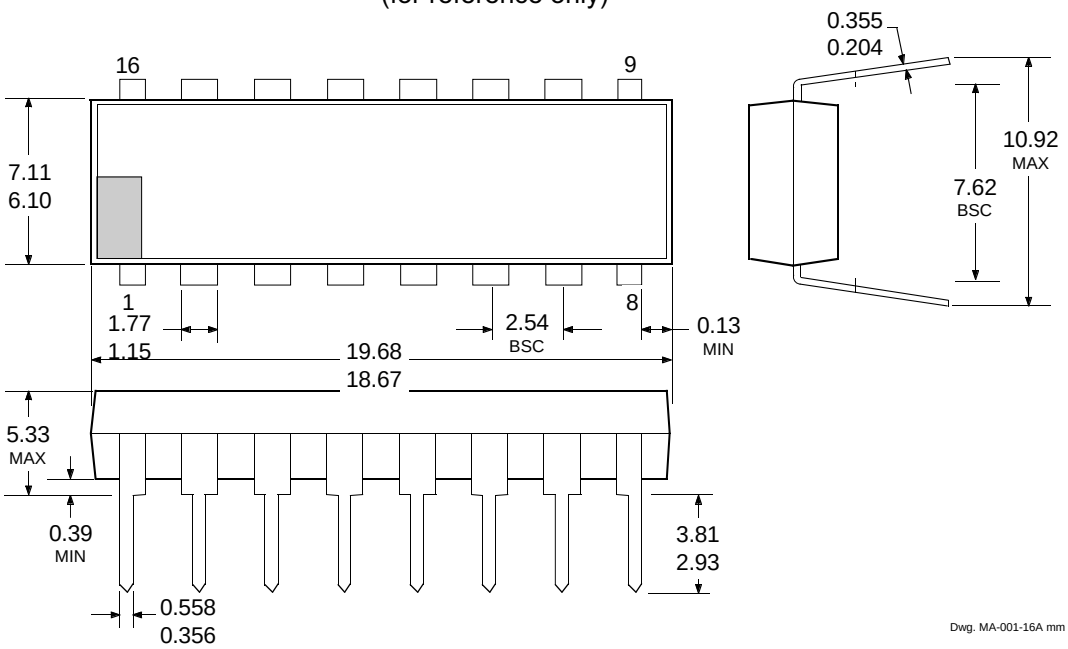
UCN5821A

Dimensions in Inches
(controlling dimensions)



Dwg. MA-001-16A in

Dimensions in Millimeters
(for reference only)

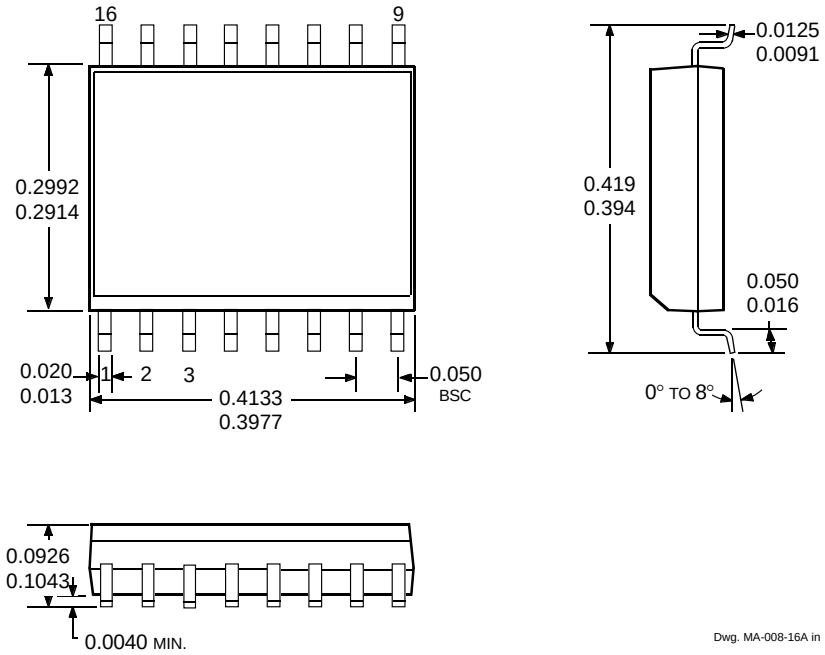


Dwg. MA-001-16A mm

NOTES: 1. Lead thickness is measured at seating plane or below.
2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.

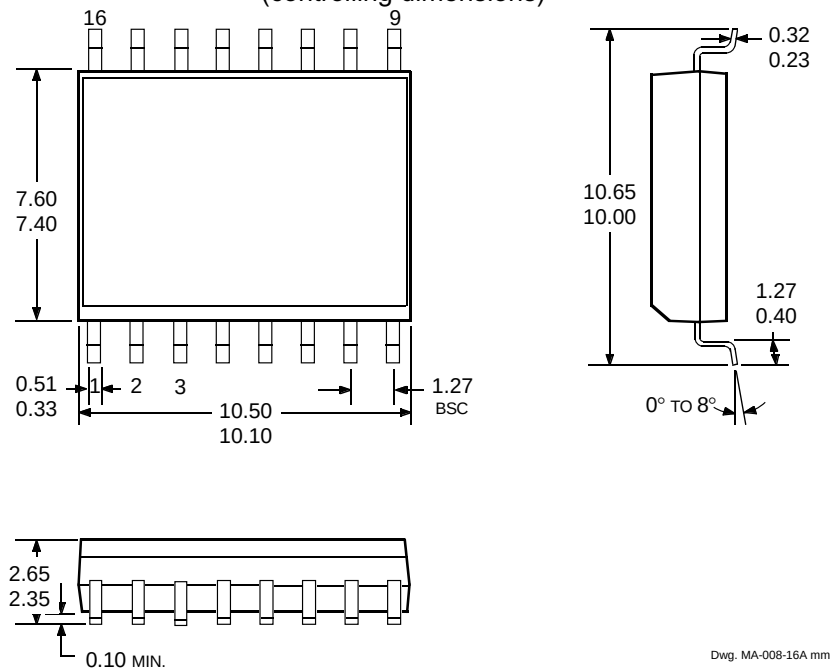
UCN5821LW

Dimensions in Inches
(for reference only)



Dwg. MA-008-16A in

Dimensions in Millimeters
(controlling dimensions)



Dwg. MA-008-16A mm

NOTES: 1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.

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8-BIT SERIAL-INPUT, LATCHED DRIVERS