First Edition
Sep 7, 2005

LCD Module Technical Specification

Final Revision
******

Type No. **DMF-50426NYJ-SLY-AEE-AFN**

Approved by (Quality Assurance Division)

Checked by (ACI Engineering Division)

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Revision History

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1.General Specifications

Operating Temp.	:	min. -20°C ~max. 70°C
Storage Temp.	:	min. -20°C ~max. 70°C
Dot Pixels	:	128 (W) × 32 (H) dots
Dot Size	:	0.40 (W) × 0.48 (H) mm
Dot Pitch	:	0.43 (W) × 0.51 (H) mm
Viewing Area	:	60.0 (W) × 21.3 (H) mm
Outline Dimensions	:	75.0 (W) × 41.5 (H) × 8.5 max. (D) mm
Weight	:	30g max.
LCD Type	:	NSD-13050 (STN / Yellow-mode / Transflective)
Viewing Angle	:	6:00
Data Transfer	:	8-bit parallel data transfer
Backlight	:	LED Backlight / Yellow-green
Drawings	:	Dimensional Outline UE-35371B
RoHS regulation	:	To our best knowledge, this product satisfies material requirement of RoHS regulation. Our company is doing the best efforts to obtain the equivalent certificate from our suppliers.

2.Electrical Specifications

2.1.Absolute Maximum Ratings

V_{SS}=0V

Parameter	Symbol	Conditions	Min.	Max.	Units
Supply Voltage (Logic)	V_{DD}-V_{SS}	-	-0.3	7.0	V
Supply Voltage (LCD Drive)	V_{DD}-V_{LC}	-	-0.3	17.0	V
Input Voltage	V_I	-	-0.3	V_{DD}+0.3	V

2.2.DC Characteristics

Ta=25°C, V_{SS}=0V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage (Logic)	V_{DD}-V_{SS}	-	4.5	-	5.5	V
Supply Voltage (LCD Drive)	V_{DD}-V_{LC}	Shown in 3.1				V
High Level Input Voltage	V_{IH1}	V_{DD}=5.0V±10% Note 1	0.7×V_{DD}	-	V_{DD}	V
	V_{IH2}	V_{DD}=5.0V±10% Note 2	2.0	-	V_{DD}	V
Low Level Input Voltage	V_{IL1}	V_{DD}=5.0V±10% Note 1	0	-	0.3×V_{DD}	V
	V_{IL2}	V_{DD}=5.0V±10% Note 2	0	-	0.8	V
High Level Output Voltage	V_{OH}	I_{OH}=-0.205mA	2.4	-	-	V
Low Level Output Voltage	V_{OL}	I_{OL}=1.2mA	-	-	0.4	V
Supply Current	I_{DD}	V_{DD}-V_{SS}=5.0V	-	2.0	5.0	mA
	I_{LC}	V_{DD}-V_{LC}=13.1V	-	1.8	4.0	mA

Note 1 : Apply to $\overline{RST}$

Note 2 : Apply to DB0~DB7, $\overline{CS1}$, $\overline{CS2}$, R/W, D/I, E

2.3. AC Characteristics

2.3.1. Timing Characteristics

V_{DD}=5.0V±10%

Parameter	Symbol	Conditions	Min.	Max.	Units
Enable Cycle Time	t_{CYC}	Fig.1, 2	1000	-	ns
Enable Pulse Width	PW_{EH}, PW_{EL}	Fig.1, 2	450	-	ns
Enable Rise/Fall Time	t_r, t_f	Fig.1, 2	-	25	ns
Address Setup Time	t_{AS}	Fig.1, 2	140	-	ns
Address Hold Time	t_{AH}	Fig.1, 2	10	-	ns
Write Data Setup Time	t_{DSW}	Fig.1	200	-	ns
Write Data Hold Time	t_{DHW}	Fig.1	10	-	ns
Read Data Delay Time	t_{DDR}	Fig.2	-	320	ns
Read Data Hold Time	t_{DHR}	Fig.2	20	-	ns

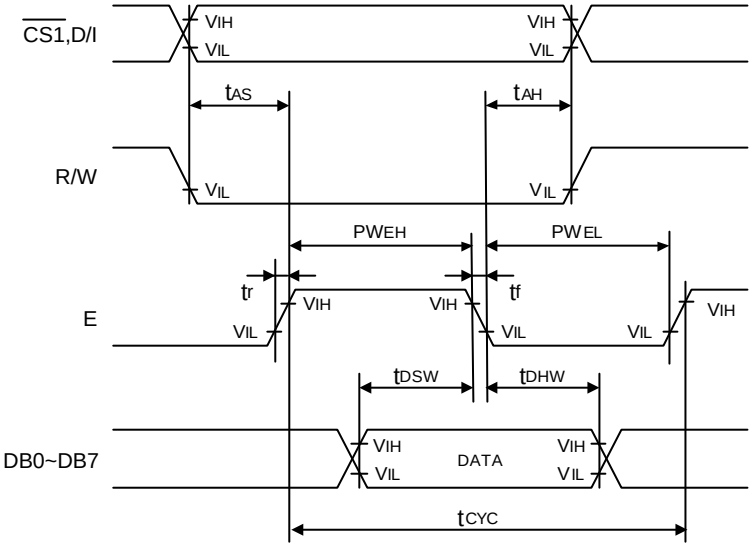


Fig.1 Write Operation Timing

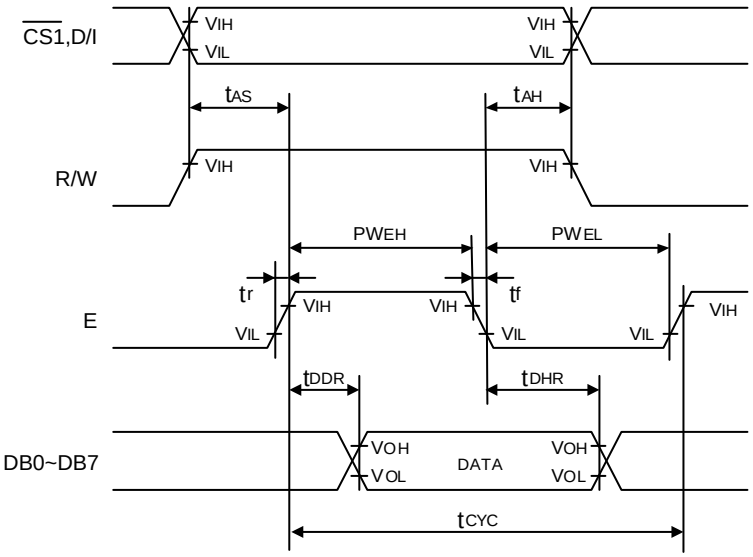
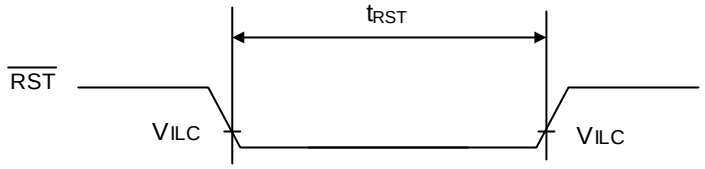


Fig.2 Read Operation Timing

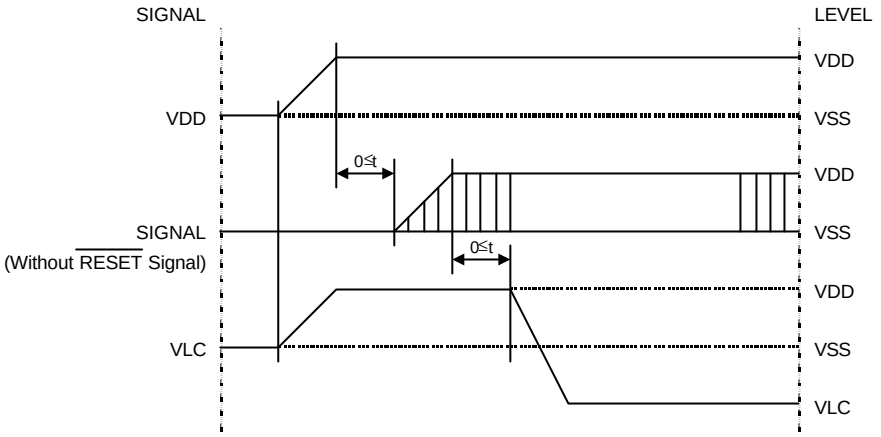
2.3.2. Power Supply Initial Conditions

Parameter	Symbol	Min.	Max.	Units
Reset Low Level Time	t_{RST}	1.0	-	ms

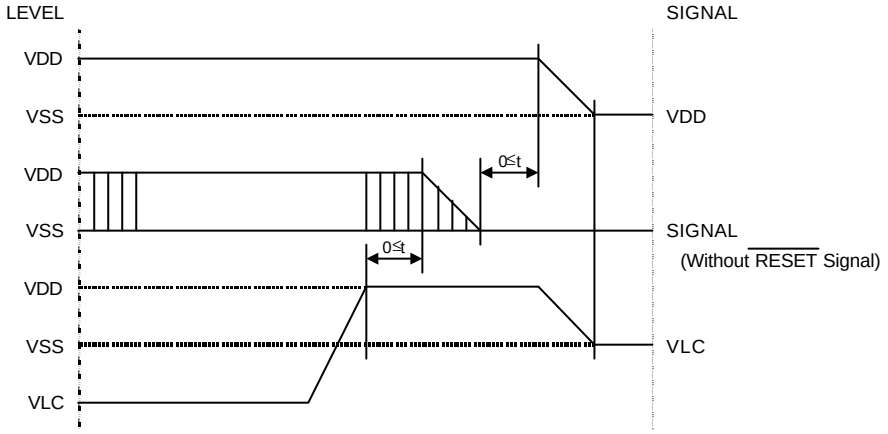


2.4. Power Supply ON/OFF Sequence

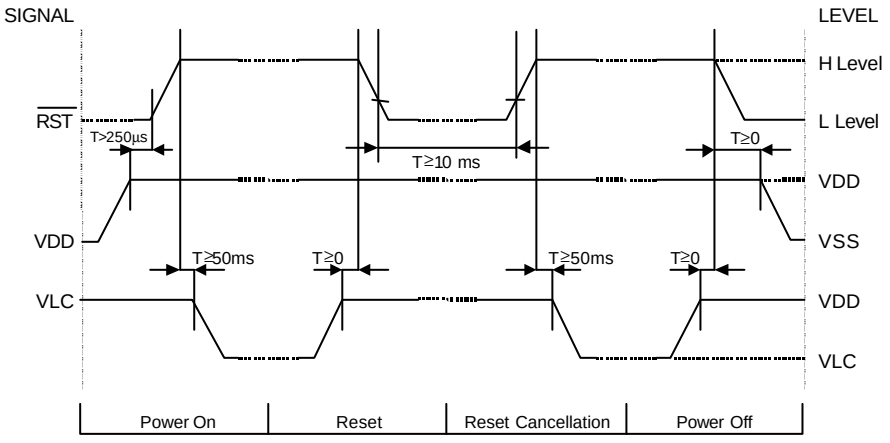
2.4.1. ON Sequence



2.4.2. OFF Sequence



2.4.3. Reset Sequence



Please maintain the above sequence when turning on and off the power supply of the module.

If V_{LC} is supplied to the module while internal alternate signal for LCD driving (M) is unstable or $\overline{RST}$ is active, DC component will be supplied to the LCD panel. This may cause damage to the LCD module.

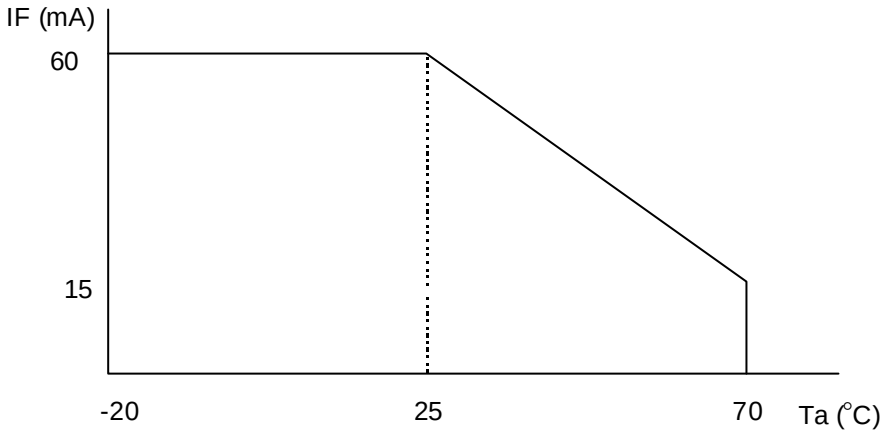
2.5. Lighting Specifications

2.5.1. Absolute Maximum Ratings

Ta=25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Foward Current	I_F	Note 1	-	-	20	mA
Reverse Voltage	V_R	-	-	-	8	V
LED Power Dissipation	P_D	-	-	-	0.3	W

Note 1 : Refer to the foward current derating curve.



2.5.2. Operating Characteristics

Ta=25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Foward Voltage	V_F	I_F=30mA	3.65	4.10	4.45	V
Luminance of Backlight Surface	L	I_F=30mA	6.5	-	-	cd/m^2

3.Optical Specifications

3.1. LCD Driving Voltage

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Recommended	V_{DD}-V_{LC}	Ta= -20°C	-	-	15.2	V
LCD Driving Voltage		Ta=25°C	12.2	13.1	14.0	V
Note 1		Ta=70°C	10.5	-	-	V

Note 1 : Voltage (Applied actual waveform to LCD Module) for the best contrast. The range of minimum and maximum shows tolerance of the operating voltage. The specified contrast ratio and response time are not guaranteed over the entire range.

3.2. Optical Characteristics

Ta=25°C, 1/64 Duty, 1/9 Bias, V_D=13.1V (Note 4), θ= 0°, ϕ= - °

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Units
Contrast Ratio Note 1		CR	θ= 0°, ϕ= - °	-	6	-	
Viewing Angle			Shown in 3.3				
Response	Rise Note 2	T_{ON}	-	-	75	150	ms
Time	Decay Note 3	T_{OFF}	-	-	125	200	ms

Note 1 :Contrast ratio is defined as follows.

$CR = L_{OFF} / L_{ON}$

L_{ON} : Luminance of the ON segments

L_{OFF}: Luminance of the OFF segments

Note 2 :The time that the luminance level reaches 90% of the saturation level from 0% when ON signal is applied.

Note 3 :The time that the luminance level reaches 10% of the saturation level from 100% when OFF signal is applied.

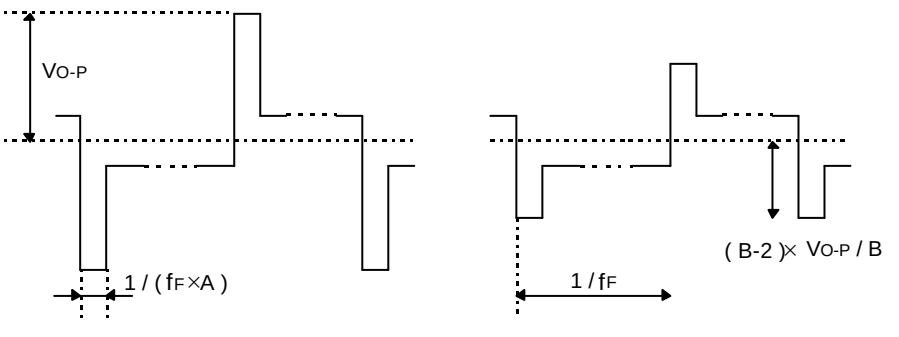
Note 4 :Definition of Driving Voltage V_D

Assuming that the typical driving waveforms shown below are applied to the LCD Panel at 1/A Duty - 1/B Bias (A : Duty Number, B : Bias Number). Driving voltage V_D is defined as follows.

$V_D = (Vth1+Vth2) / 2$

Vth1 : The voltage V_{O-P} that should provide 50% of the saturation level in the luminance at the segment which the ON signal is applied to.

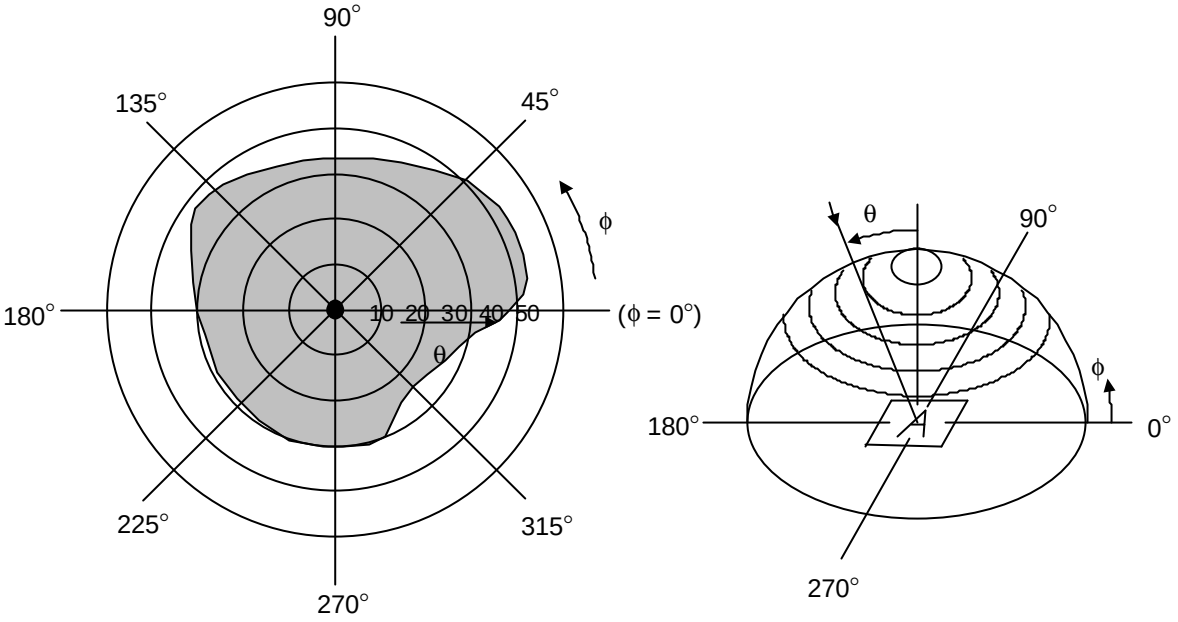
Vth2 : The voltage V_{O-P} that should provide 50% of the saturation level in the luminance at the segment which the OFF signal is applied to.



<ON SIGNAL> <OFF SIGNAL>

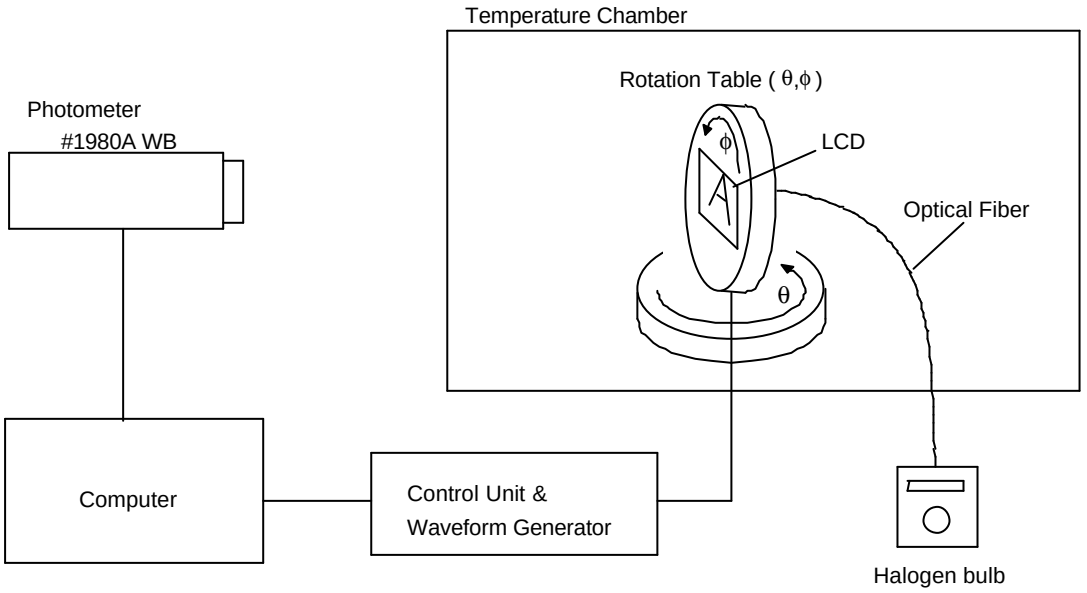
3.3. Definition of Viewing Angle and Optimum Viewing Area

*Point • shows the point where contrast ratio is measured. : θ= 0°, ϕ= -°
*Driving condition : 1/64 Duty, 1/9 Bias, V_D=13.1V, f_F=70Hz



*Area ▭ shows typ. CR≥2

3.4. System Block Diagram



4.I/O Terminal

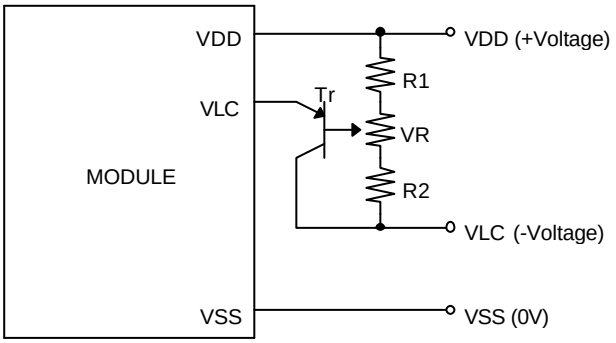
4.1. Pin Assignment

CN1

No.	Symbol	Level	Function
1	V_{DD}	-	Power Supply for Logic
2	V_{SS}	-	Power Supply (0V, GND)
3	V_{LC}	-	Power Supply for LCD Drive
4	DB0	H / L	Data Bus Line
5	DB1	H / L	Data Bus Line
6	DB2	H / L	Data Bus Line
7	DB3	H / L	Data Bus Line
8	DB4	H / L	Data Bus Line
9	DB5	H / L	Data Bus Line
10	DB6	H / L	Data Bus Line
11	DB7	H / L	Data Bus Line
12	$\overline{CS1}$	H / L	Chip Select Signal
13	$\overline{RST}$	H / L	Reset Signal L : Reset
14	R/W	H / L	Write Signal L : Active
15	D/I	H / L	Data / Instruction Signal
16	E	H,H→L	Enable Signal (No pull-up Resister)
17	F GND	-	Frame Ground
18	NC	-	Non-connection
1	LED A	-	LED Anode Terminal
2	LED K	-	LED Cathode Terminal

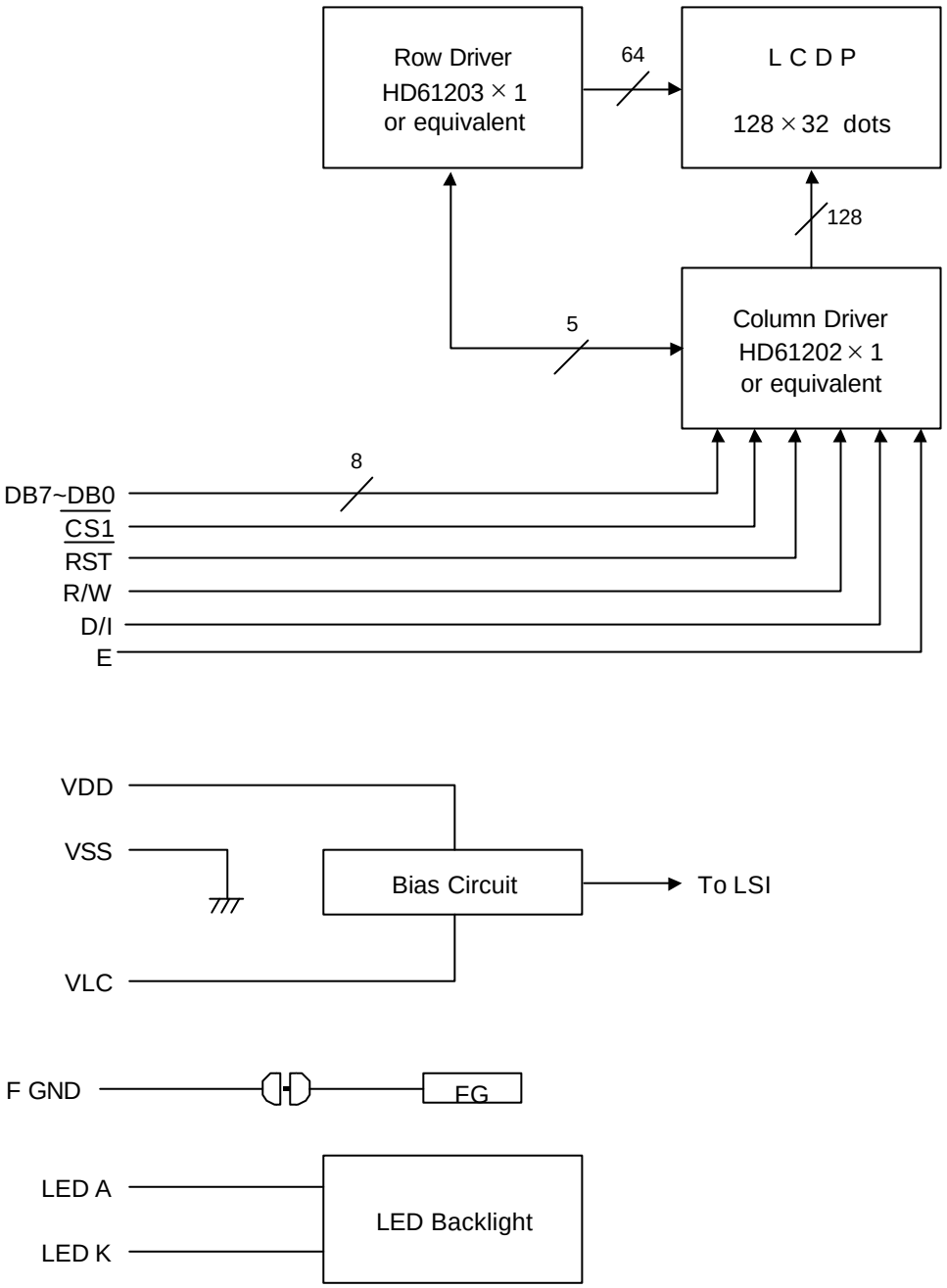
4.2. Example of Power Supply

It is recommended to apply a potentiometer for the contrast adjust due to the tolerance of the driving voltage and its temperature dependence.



R1+R2+VR=10~ 20KΩ
Tr=2SA1202 or equivalent

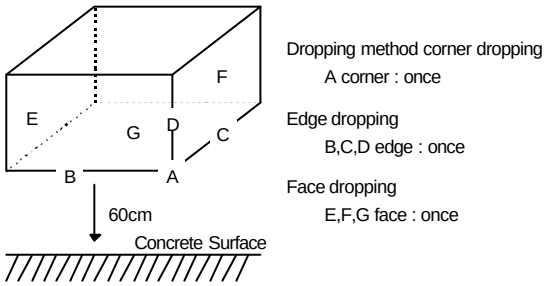
4.3. Block Diagram



5.Test

No change on display and in operation under the following test condition.

Conditions: Unless otherwise specified, tests will be conducted under the following condition.
Temperature: 20±5°C
Humidity : 65±5%RH
tests will be not conducted under functioning state.

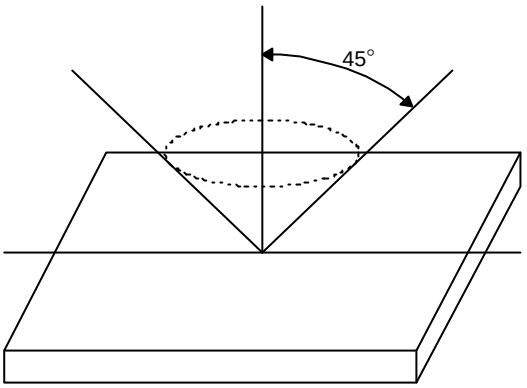
No.	Parameter	Conditions	Notes
1	High Temperature Operating	70°C±2°C, 96hrs (operation state)	
2	Low Temperature Operating	-20°C±2°C, 96hrs (operation state)	1
3	High Temperature Storage	70°C±2°C, 96hrs	2
4	Low Temperature Storage	-20°C±2°C, 96hrs	1,2
5	Damp Proof Test	40°C±2°C,90~95%RH, 96hrs	1,2
6	Vibration Test	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X, Y, Z for each 15 minutes	3
7	Shock Test	To be measured after dropping from 60cm high on the concrete surface in packing state. 	

Note 1 :No dew condensation to be observed.
Note 2 :The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after removed from the test chamber.
Note 3 :Vibration test will be conducted to the product itself without putting it in a container.

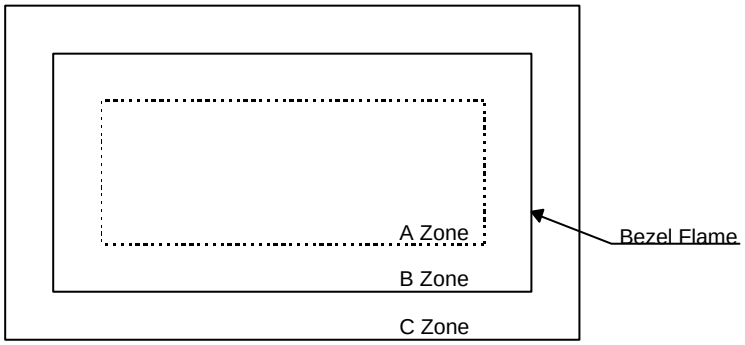
6.Appearance Standards

6.1.Inspection conditions

The LCD shall be inspected under 40W white fluorescent light.
The distance between the eyes and the sample shall be more than 30cm.
All directions for inspecting the sample should be within 45°against perpendicular line.



6.2.Definition of applicable Zones



A Zone : Active display area
B Zone : Area from outside of "A Zone" to validity viewing area
C Zone : Rest parts

A Zone + B Zone = Validity viewing area

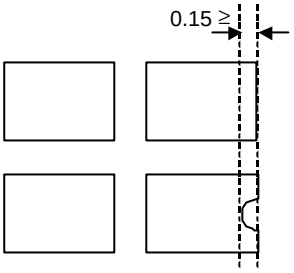
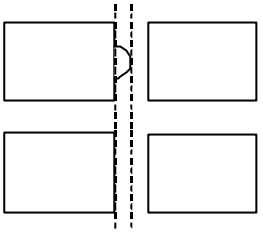
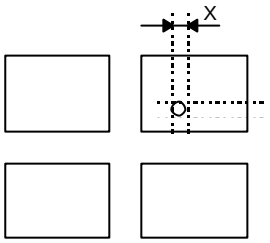
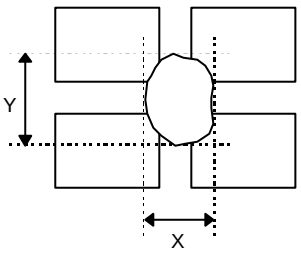
6.3. Standards

<table>
<tr><th>No.</th><th>Parameter</th><th>Criteria</th></tr>
<tr><td>1</td><td>Black and White Spots, Foreign Substances</td><td>
(1) Round Shape
<table>
<tr><th rowspan="2">Zone / Dimension (mm)</th><th colspan="3">Acceptable Number</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>D ≤0.1</td><td>*</td><td>*</td><td>*</td></tr>
<tr><td>0.1 < D ≤0.2</td><td>3</td><td>5</td><td>*</td></tr>
<tr><td>0.2 < D ≤0.25</td><td>2</td><td>3</td><td>*</td></tr>
<tr><td>0.25< D ≤0.3</td><td>0</td><td>1</td><td>*</td></tr>
<tr><td>0.3 < D</td><td>0</td><td>0</td><td>*</td></tr>
</table>
D = (Long + Short) / 2 * : Disregard

(2) Line Shape
<table>
<tr><th rowspan="2">X (mm) \ Y (mm) / Zone</th><th rowspan="2">Y (mm)</th><th colspan="3">Acceptable Number</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>-</td><td>0.03 ≥ W</td><td>*</td><td>*</td><td>*</td></tr>
<tr><td>2.0 ≥ L</td><td>0.05 ≥ W</td><td>3</td><td>3</td><td>*</td></tr>
<tr><td>1.0 ≥ L</td><td>0.1 ≥ W</td><td>3</td><td>3</td><td>*</td></tr>
<tr><td>-</td><td>0.1 < W</td><td colspan="3">In the same way (1)</td></tr>
</table>
X : Length Y : Width * : Disregard

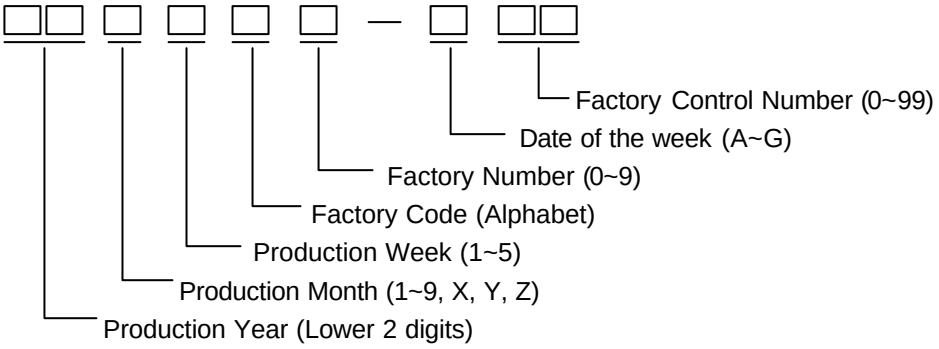
Total defects shall not exceed 5.
</td></tr>
<tr><td>2</td><td>Air Bubbles (between glass & polarizer)</td><td>
<table>
<tr><th rowspan="2">Zone / Dimension (mm)</th><th colspan="3">Acceptable Number</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>D ≤0.3</td><td>*</td><td>*</td><td>*</td></tr>
<tr><td>0.3 < D ≤0.4</td><td>3</td><td>*</td><td>*</td></tr>
<tr><td>0.4 < D ≤0.6</td><td>2</td><td>3</td><td>*</td></tr>
<tr><td>0.6 < D</td><td>0</td><td>0</td><td>*</td></tr>
</table>
* : Disregard

Total defects shall not exceed 3.
</td></tr>
</table>

No.	Parameter	Criteria
3	The Shape of Dot	(1) Dot Shape (with Dent)  As per the sketch of left hand. (2) Dot Shape (with Projection)  Should not be connected to next dot. (3) Pin Hole  (X+Y) / 2 ≤ 0.2mm (Less than 0.1mm is no counted.) (4) Deformation  (X+Y) / 2 ≤ 0.2mm Total acceptable number : 1/dot, 5/cell (Defect number of (4) : 1pc.)
4	Polarizer Scratches	Not to be conspicuous defects.
5	Polarizer Dirts	If the stains are removed easily from LCDP surface, the module is not defective.
6	Complex Foreign Substance Defects	Black spots, line shaped foreign substances or air bubbles between glass & polarizer should be 5pcs maximum in total.
7	Distance between Different Foreign Substance Defects	D ≤ 0.2 : 20mm or more 0.2 < D : 40mm or more

7.Code System of Production Lot

The production lot of module is specified as follows.



8.Type Number

The type number of module is specified as follows.

DMF-50426NYJ-SLY-AEE-AFN

9.Applying Precautions

Please contact us when questions and/or new problems not specified in this Specifications arise.

10.Precautions Relating Product Handling

The Following precautions will guide you in handling our product correctly.

1) Liquid crystal display devices
   1. The liquid crystal display device panel used in the liquid crystal display module is made of plate glass. Avoid any strong mechanical shock. Should the glass break handle it with care.
   2. The polarizer adhering to the surface of the LCD is made of a soft material. Guard against scratching it.

2) Care of the liquid crystal display module against static electricity discharge.
   1. When working with the module, be sure to ground your body and any electrical equipment you may be using. We strongly recommend the use of anti static mats (made of rubber), to protect work tables against the hazards of electrical shock.
   2. Avoid the use of work clothing made of synthetic fibers. We recommend cotton clothing or other conductivity-treated fibers.
   3. Slowly and carefully remove the protective film from the LCD module, since this operation can generate static electricity.

3) When the LCD module alone must be stored for long periods of time:
   1. Protect the modules from high temperature and humidity.
   2. Keep the modules out of direct sunlight or direct exposure to ultraviolet rays.
   3. Protect the modules from excessive external forces.

4) Use the module with a power supply that is equipped with an overcurrent protector circuit,since the module is not provided with this protective feature.

5) Do not ingest the LCD fluid itself should it leak out of a damaged LCD module. Should hands or clothing come in contact with LCD fluid, wash immediately with soap.

6) Conductivity is not guaranteed for models that use metal holders where solder connections between the metal holder and the PCB are not used. Please contact us to discuss appropriate ways to assure conductivity.

7) For models which use CFL:
   1. High voltage of 1000V or greater is applied to the CFL cable connector area. Care should be taken not to touch connection areas to avoid burns.
   2. Protect CFL cables from rubbing against the unit and thus causing the wire jacket to become worn.
   3. The use of CFLs for extended periods of time at low temperatures will significantly shorten their service life.

8) For models which use touch panels:
   1. Do not stack up modules since they can be damaged by components on neighboring modules.
   2. Do not place heavy objects on top of the product. This could cause glass breakage.

9) For models which use COG,TAB,or COF:
   1. The mechanical strength of the product is low since the IC chip faces out unprotected from the rear. Be sure to protect the rear of the IC chip from external forces.
   2. Given the fact that the rear of the IC chip is left exposed, in order to protect the unit from electrical damage, avoid installation configurations in which the rear of the IC chip runs the risk of making any electrical contact.

10) Models which use flexible cable, heat seal, or TAB:
   1. In order to maintain reliability, do not touch or hold by the connector area.
   2. Avoid any bending, pulling, or other excessive force, which can result in broken connections.

11) In case of buffer material such as cushion / gasket is assembled into LCD module, it may have an adverse effect on connecting parts (LCD panel-TCP / HEAT SEAL / FPC / etc., PCB-TCP / HEAT SEAL / FPC etc., TCP-HEAT SEAL, TCP-FPC, HEAT SEAL-FPC, etc.,) depending on its materials.
   Please check and evaluate these materials carefully before use.

12) In case of acrylic plate is attached to front side of LCD panel, cloudiness (very small cracks) can occur on acrylic plate, being influenced by some components generated from polarizer film..
   Please check and evaluate those acrylic materials carefully before use.

11.Warranty

This product has been manufactured to your company's specifications as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

1. We cannot accept responsibility for any defect, which may arise from additional manufacturing of the product (including disassembly and reassembly), after product delivery.

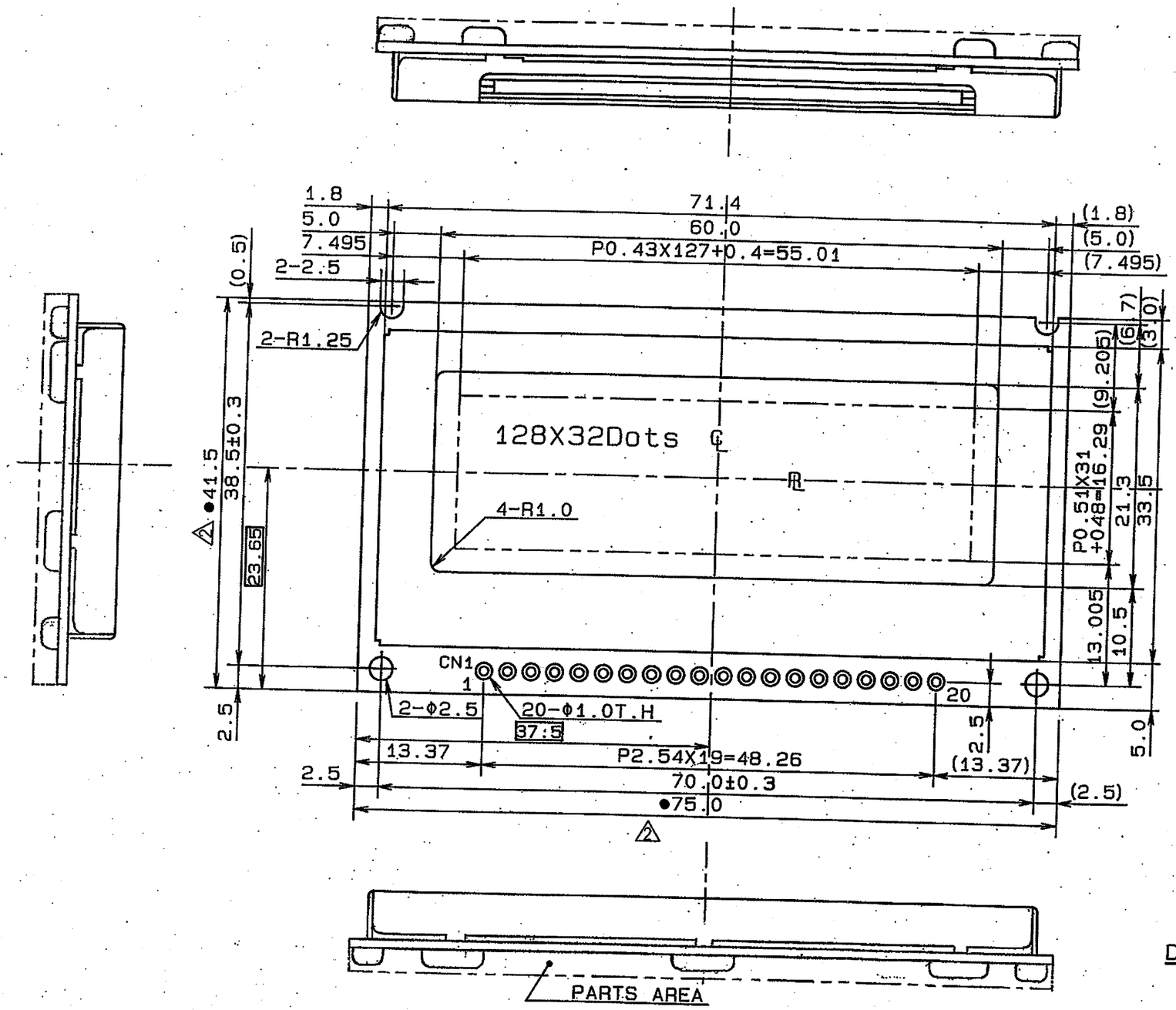
2. We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.

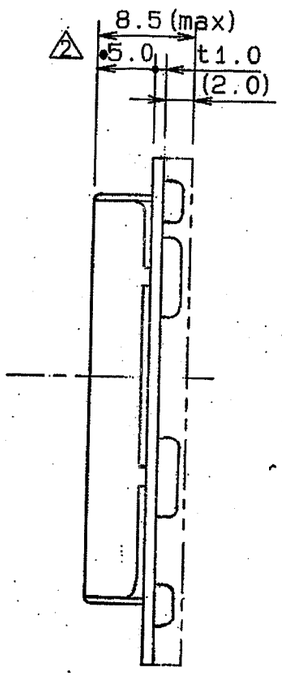
3. We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed your company's acceptance inspection procedures.

4. When the product is in CFL models, CFL service life and brightness will vary According to the performance of the inverter used, leaks, etc. We cannot accept responsibility for product performance, reliability, or defect, which may arise.

5. We cannot accept responsibility for intellectual property of a third party, which may arise through the application of our product to your assembly with exception to those issues relating directly to the structure or method of manufacturing of our product.

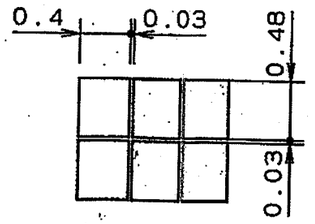
6. Optrex will not be held responsible for any quality guarantee issue for defect products judged as Optrex-origin longer than 2 (two) years from Optrex production or 1(one) year from Optrex, Optrex America, Optrex Europe delivery which ever comes later.





PIN ASSIGNMENT
CN1

NO.	SYMBOL
1	VDD
2	VSS
3	VLC
4	DB0
5	DB1
6	DB2
7	DB3
8	DB4
9	DB5
10	DB6
11	DB7
12	$\overline{CS1}$
13	$\overline{RST}$
14	R/W
15	D/I
16	E
17	FGND
18	NC
19	LED A
20	LED K



DOT DETAIL (SCALE20: 1)

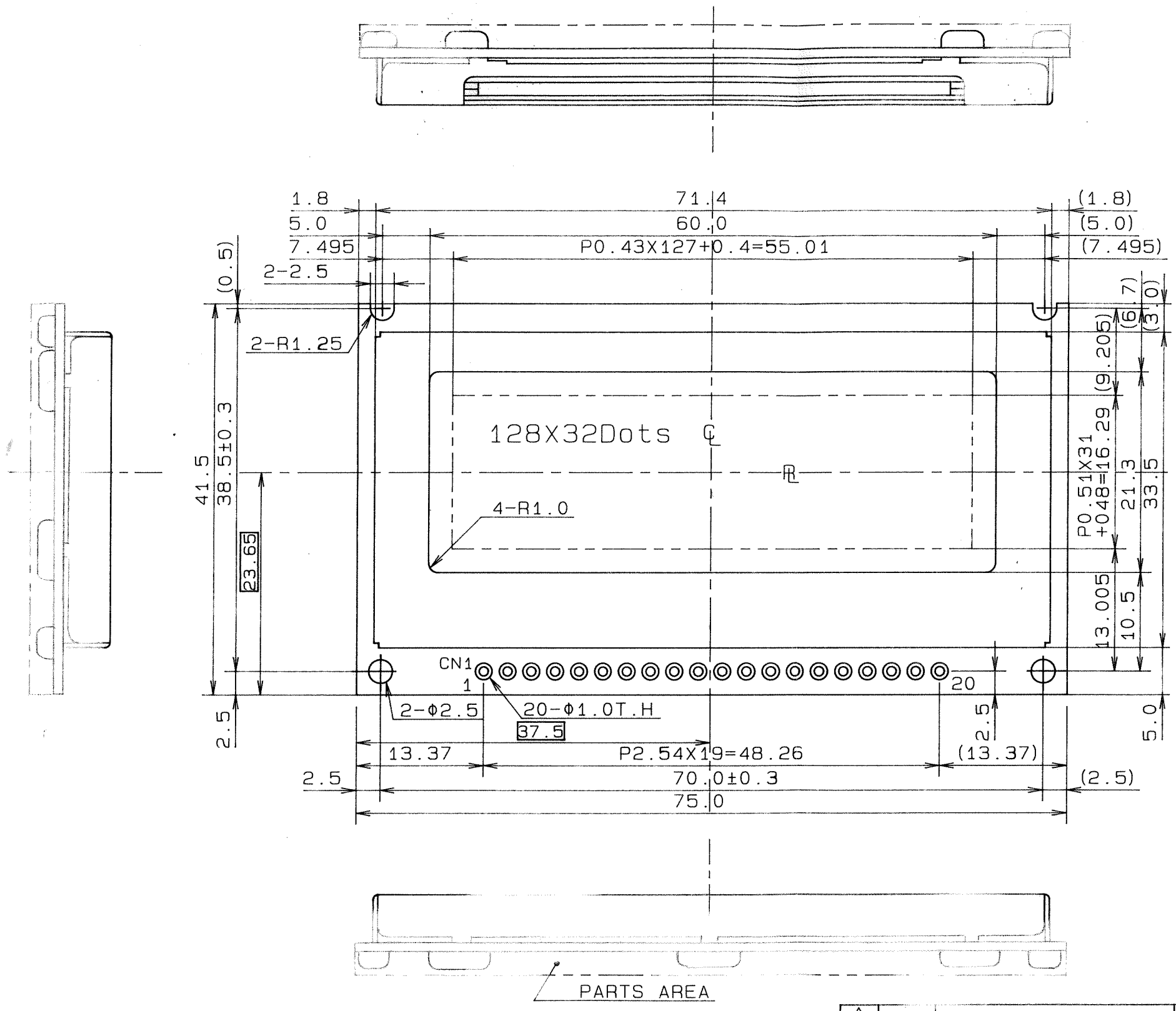
△2 NOTE
1) DON'T USE MATERIAL WHICH ARE PROHIBITED BY RoHS.
2) THE DIMENSIONS WITH THE MARK● ARE CONTROLLED AS A PARTICULAR CHARACTERISTIC.

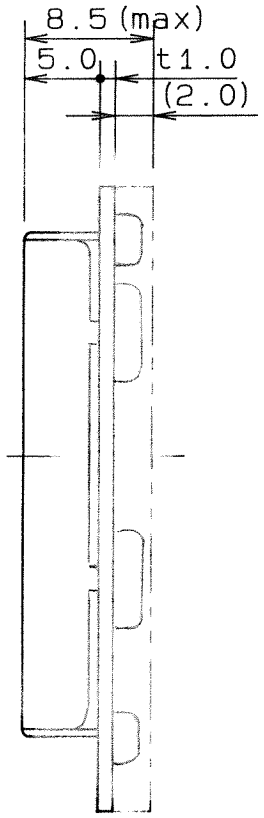
TOLERANCE				
MEASURE	A	B	C	
I≤16	±0.1	±0.3	±1	
16<I≤63	±0.2	±0.5	±1.5	
63<I≤250	±0.3	±0.8	±2	
250<I≤500	±0.5	±1.2	±3	ANGLE
500<I≤1000	±0.8	±2	±4	±30' ±1° ±2°

ISSUE	DATE	REVISIONS	NAME
6			
5			
4			
3			
2	NOV.04'05	ADD RoHS NOTE.	A.Hattanda
1	JUN.19 '01	Change of MODEL name.	

OPTREX CORPORATION

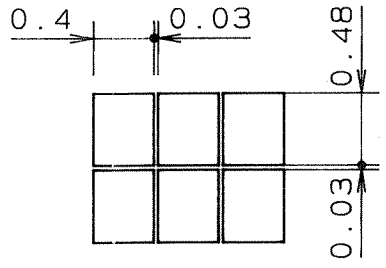
MATERIAL	FINISH	Q'ty	NOTE
3rd ANGLE PROJECTION	TOLERANCE CLASS: B	SCALE: 2: 1	
APPROVED Nov.27'93	MODEL DMF-50426 NJ/NYJ series △1		
CHECKED Nov.27.93	TITLE DIMENSIONAL OUTLINE		
DRAWN Nov.19'93 K.Shimazu	CODE		
DESIGNED Nov.19'93 K.Shimazu	DRAWING No. UE-35371B		





PIN ASSIGNMENT
CN1

NO.	SYMBOL
1	VDD
2	VSS
3	VLC
4	DB0
5	DB1
6	DB2
7	DB3
8	DB4
9	DB5
10	DB6
11	DB7
12	$\overline{CS1}$
13	$\overline{RST}$
14	R/W
15	D/I
16	E
17	FGND
18	NC
19	LED A
20	LED K



DOT DETAIL (SCALE20: 1)

ISSUED
'01. 6. 26
OPTREX Corp.

TOLERANCE				
MEASURE	A	B	C	ANGLE
l≤16	±0.1	±0.3	±1	
16<l≤63	±0.2	±0.5	±1.5	
63<l≤250	±0.3	±0.8	±2	
250<l≤500	±0.5	±1.2	±3	
500<l≤1000	±0.8	±2	±4	±30' ±1° ±2°

ISSUE	DATE	REVISIONS	NAME
6			
5			
4			
3			
2			
1	JUN.19 '01	Change of MODEL name.	

OPTREX CORPORATION

MATERIAL	FINISH	Q'ty	NOTE
3rd ANGLE PROJECTION	TOLERANCE CLASS: B	SCALE: 2: 1	
APPROVED NOV.27'93	MODEL DMF-50426NJ NYJ series △1		
CHECKED NOV.27.93	TITLE DIMENSIONAL OUTLINE		
DRAWN NOV.18'93 K.Shimazu	CODE		
DESIGNED NOV.18'93 K.Shimazu	DRAWING No. UE-35371A		

HD61202U

(Dot Matrix Liquid Crystal GraphicDisplay Column Driver)

HITACHI

ADE-207-273(Z)
'99.9
Rev. 0.0

Description

HD61202U is a column (segment) driver for dot matrix liquid crystal graphic display systems. It stores the display data transferred from a 8-bit micro controller in the internal display RAM and generates dot matrix liquid crystal driving signals.

Each bit data of display RAM corresponds to on/off state of a dot of a liquid crystal display to provide more flexible than character display.

As it is internally equipped with 64 output drivers for display, it is available for liquid crystal graphic displays with many dots.

The HD61202U, which is produced in the CMOS process, can complete portable battery drive equipment in combination with a CMOS micro-controller, utilizing the liquid crystal display's low power dissipation.

Moreover it can facilitate dot matrix liquid crystal graphic display system configuration in combination with the row (common) driver HD61203U.

Features

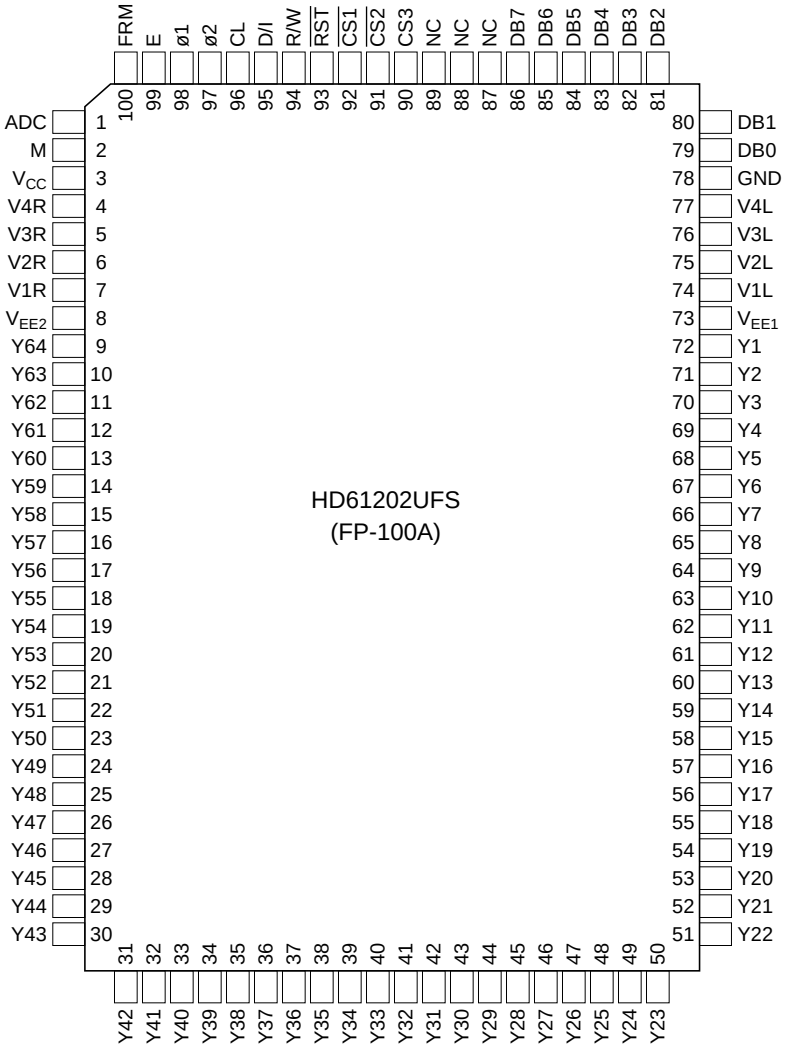
- Dot matrix liquid crystal graphic display column driver incorporating display RAM
- RAM data direct display by internal display RAM
  - RAM bit data 1: On
  - RAM bit data 0: Off
- Display RAM capacity: 512 bytes (4096 bits)
- 8-bit parallel interface
- Internal liquid crystal display driver circuit: 64
- Display duty cycle
  Drives liquid crystal panels with 1/32–1/64 duty cycle multiplexing

- Wide range of instruction function
  Display data read/write, display on/off, set address, set display start line, read status
- Power supply: V_{CC}: 2.7V~5.5V
- Liquid crystal display driving voltage: 8V to 16V

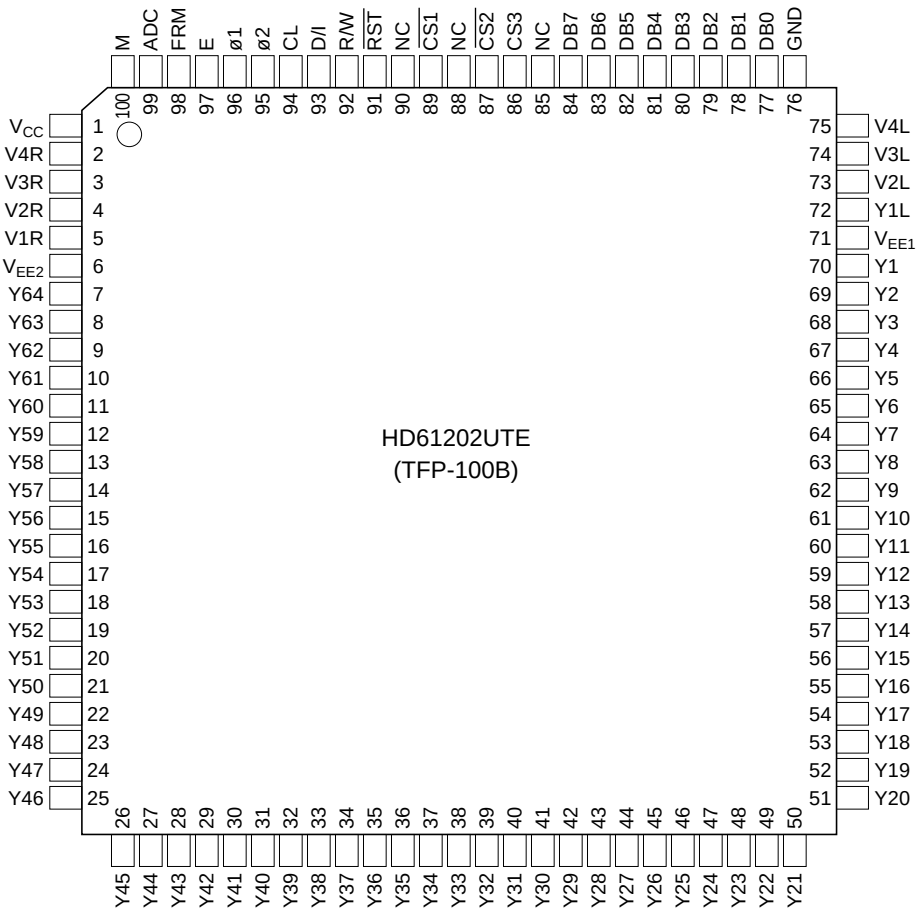
Ordering Information

Type No.	Package
HD61202UFS	100-pin plastic QFP (FP-100A)
HD61202UTE	100-pin thin plastic QFP (TFP-100B)
HCD61202U	Chip

Pin Arrangement

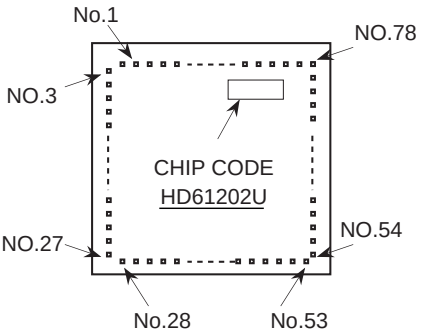


(Top view)


M
ADC
FRM
E
ø1
ø2
CL
D/I
R/W
RST
NC
CS1
NC
CS2
CS3
NC
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
GND
100 99 98 97 96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81 80 79 78 77 76
V_{CC} 1
V4R 2
V3R 3
V2R 4
V1R 5
V_{EE2} 6
Y64 7
Y63 8
Y62 9
Y61 10
Y60 11
Y59 12
Y58 13
Y57 14
Y56 15
Y55 16
Y54 17
Y53 18
Y52 19
Y51 20
Y50 21
Y49 22
Y48 23
Y47 24
Y46 25
75 V4L
74 V3L
73 V2L
72 Y1L
71 V_{EE1}
70 Y1
69 Y2
68 Y3
67 Y4
66 Y5
65 Y6
64 Y7
63 Y8
62 Y9
61 Y10
60 Y11
59 Y12
58 Y13
57 Y14
56 Y15
55 Y16
54 Y17
53 Y18
52 Y19
51 Y20
26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50
Y45 Y44 Y43 Y42 Y41 Y40 Y39 Y38 Y37 Y36 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 Y25 Y24 Y23 Y22 Y21
HD61202UTE
(TFP-100B)

(Top view)

HCD61202U PAD Arrangement

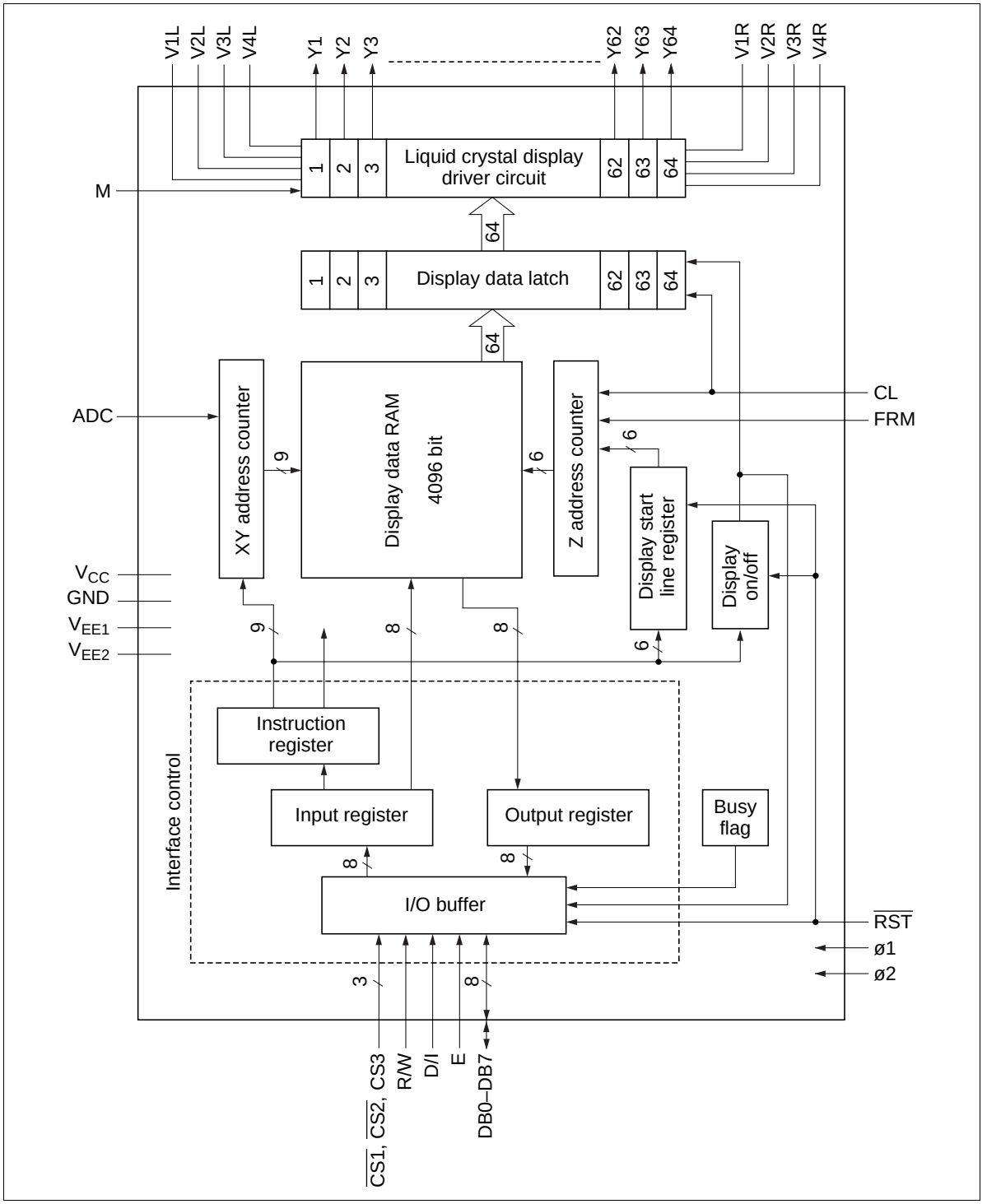


Chip Size : 4.08 × 4.08 mm²
Coordinate : Pad Center
Origin : Chip center
Pad Size : 90 × 90 µm²

HCD61202U Pad Location Coordinates

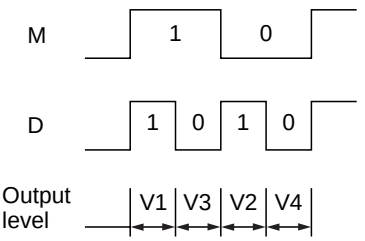
PAD No.	PAD Name	Coordinate X	Coordinate Y	PAD No.	PAD Name	Coordinate X	Coordinate Y	PAD No.	PAD Name	Coordinate X	Coordinate Y	PAD No.	PAD Name	Coordinate X	Coordinate Y
1	ADC	–1493	1756	26	Y47	–1789	–1508	51	Y22	1452	–1789	76	V3L	1789	1442
2	M	–1649	1756	27	Y46	–1789	–1653	52	Y21	1604	–1789	77	V4L	1789	1590
3	V_{CC}	–1789	1689	28	Y45	–1764	–1789	53	Y20	1764	–1789	78	GND	1789	1756
4	V4R	–1789	1445	29	Y44	–1604	–1789	54	Y19	1789	–1654	79	DB0	1495	1756
5	V3R	–1789	1293	30	Y43	–1452	–1789	55	Y18	1789	–1507	80	DB1	1335	1756
6	V2R	–1789	1148	31	Y42	–1312	–1789	56	Y17	1789	–1369	81	DB2	1176	1756
7	V1R	–1789	1011	32	Y41	–1171	–1789	57	Y16	1789	–1230	82	DB3	1016	1756
8	V_{EE2}	–1789	869	33	Y40	–976	–1789	58	Y15	1789	–1100	83	DB4	854	1756
9	Y64	–1789	721	34	Y39	–846	–1789	59	Y14	1789	–970	84	DB5	694	1756
10	Y63	–1789	591	35	Y38	–716	–1789	60	Y13	1789	–840	85	DB6	535	1756
11	Y62	–1789	461	36	Y37	–586	–1789	61	Y12	1789	–710	86	DB7	375	1756
12	Y61	–1789	331	37	Y36	–456	–1789	62	Y11	1789	–580	87	NC		
13	Y60	–1789	201	38	Y35	–326	–1789	63	Y10	1789	–450	88	NC		
14	Y59	–1789	71	39	Y34	–196	–1789	64	Y9	1789	–320	89	NC		
15	Y58	–1789	–60	40	Y33	–65	–1789	65	Y8	1789	–190	90	CS3	218	1756
16	Y57	–1789	–190	41	Y32	65	–1789	66	Y7	1789	–60	91	CS2	62	1756
17	Y56	–1789	–320	42	Y31	195	–1789	67	Y6	1789	71	92	CS1	–94	1756
18	Y55	–1789	–450	43	Y30	325	–1789	68	Y5	1789	201	93	RST	–249	1756
19	Y54	–1789	–580	44	Y29	455	–1789	69	Y4	1789	331	94	R/W	–405	1756
20	Y53	–1789	–710	45	Y28	585	–1789	70	Y3	1789	461	95	D/I	–560	1756
21	Y52	–1789	–840	46	Y27	715	–1789	71	Y2	1789	591	96	CL	–716	1756
22	Y51	–1789	–970	47	Y26	845	–1789	72	Y1	1789	721	97	ø2	–871	1756
23	Y50	–1789	–1100	48	Y25	975	–1789	73	V_{EE1}	1789	1024	98	ø1	–1027	1756
24	Y49	–1789	–1230	49	Y24	1170	–1789	74	V1L	1789	1153	99	E	–1182	1756
25	Y48	–1789	–1369	50	Y23	1311	–1789	75	V2L	1789	1293	100	FRM	–1338	1756

Block Diagram



Terminal Functions

Terminal Name	Number of Terminals	I/O	Connected to	Functions
V_{CC} GND	2		Power supply	Power supply for internal logic. Recommended voltage is: GND = 0V V_{CC} = 2.7 to 5.5V
V_{EE1} V_{EE2}	2		Power supply	Power supply for liquid crystal display drive circuit. Recommended power supply voltage is V_{CC}–V_{EE} = 8 to 16V. Connect the same power supply to V_{EE1} and V_{EE2}. V_{EE1} and V_{EE2} are not connected each other in the LSI.
V1L, V1R V2L, V2R V3L, V3R V4L, V4R	8		Power supply	Power supply for liquid crystal display drive. Apply the voltage specified depending on liquid crystals within the limit of V_{EE} through V_{CC}. V1L (V1R), V2L (V2R): Selection level V3L (V3R), V4L (V4R): Non-selection level Power supplies connected with V1L and V1R (V2L & V2R, V3L & V3R, V4L & V4R) should have the same voltages.
$\overline{CS1}$ $\overline{CS2}$ CS3	3	I	MPU	Chip selection. Data can be input or output when the terminals are in the following conditions: Terminal name: $\overline{CS1}$ / $\overline{CS2}$ / CS3 Condition: L / L / H
E	1	I	MPU	Enable. At write (R/W = low): Data of DB0 to DB7 is latched at the fall of E. At read (R/W = high): Data appears at DB0 to DB7 while E is at high level.
R/W	1	I	MPU	Read/write. R/W = High: Data appears at DB0 to DB7 and can be read by the MPU. When E = high, $\overline{CS1}$, $\overline{CS2}$ = low and CS3 = high. R/W = Low: DB0 to DB7 can accept at fall of E when $\overline{CS1}$, $\overline{CS2}$ = low and CS3 = high.
D/I	1	I	MPU	Data/instruction. D/I = High: Indicates that the data of DB0 to DB7 is display data. D/I = Low: Indicates that the data of DB0 to DB7 is display control data.

Terminal Name	Number of Terminals	I/O	Connected to	Functions
ADC	1	I	V_{CC}/GND	Address control signal to determine the relation between Y address of display RAM and terminals from which the data is output. ADC = High: Y1: H'0, Y64: H'63 ACD = Low: Y64: H'0, Y1: H'63
DB0–DB7	8	I/O	MPU	Data bus, three-state I/O common terminal.
M	1	I	HD61203U	Switch signal to convert liquid crystal drive waveform into AC.
FRM	1	I	HD61203U	Display synchronous signal (frame signal). Presets the 6-bit display line counter and synchronizes the common signal with the frame timing when the FRM signal becomes high.
CL	1	I	HD61203U	Synchronous signal to latch display data. The rising CL signal increments the display output address counter and latches the display data.
ø1, ø2	2	I	HD61203U	2-phase clock signal for internal operation. The ø1 and ø2 clocks are used to perform operations (I/O of display data and execution of instructions) other than display.
Y1–Y64	64	O	Liquid crystal display	Liquid crystal display column (segment) drive output. The outputs at these pins are at the light-on level when the display RAM data is 1, and at the light-off level when the display RAM data is 0. Relation among output level, M, and display data (D) is as follows: 
$\overline{RST}$	1	I	MPU or external CR	The following registers can be initialized by setting the $\overline{RST}$ signal to low level. 1. On/off register 0 set (display off) 2. Display start line register line 0 set (displays from line 0) After releasing reset, this condition can be changed only by instruction.
NC	3		Open	Unused terminals. Don't connect any lines to these terminals.

Note: 1 corresponds to high level in positive logic.

Function of Each Block

Interface Control

I/O Buffer: Data is transferred through 8 data bus lines (DB0–DB7).

DB7: MSB (most significant bit)
DB0: LSB (least significant bit)

Data can neither be input nor output unless $\overline{CS1}$ to CS3 are in the active mode. Therefore, when $\overline{CS1}$ to CS3 are not in active mode it is useless to switch the signals of input terminals except $\overline{RST}$ and ADC; that is namely, the internal state is maintained and no instruction excutes. Besides, pay attention to $\overline{RST}$ and ADC which operate irrespectively of $\overline{CS1}$ to CS3.

Register: Both input register and output register are provided to interface to an MPU whose speed is different from that of internal operation. The selection of these registers depend on the combination of R/W and D/I signals (Table 1).

1. Input register

   The input register is used to store data temporarily before writing it into display data RAM.

   The data from MPU is written into input register, then into display data RAM automatically by internal operation. When $\overline{CS1}$ to CS3 are in the active mode and D/I and R/W select the input register as shown in Table 1, data is latched at the fall of the E signal.

2. Output register

   The output register is used to store data temporarily that is read from display data RAM. To read out the data from the output register, $\overline{CS1}$ to CS3 should be in the active mode and both D/I and R/W should be 1. With the read display data instruction, data stored in the output register is output while E is high level. Then, at the fall of E, the display data at the indicated address is latched into the output register and the address is increased by 1.

   The contents in the output register are rewritten by the read display data instruction, but are held by address set instruction, etc.

   Therefore, the data of the specified address cannot be output with the read display data instruction right after the address is set, but can be output at the second read of data. That is to say, one dummy read is necessary. Figure 1 shows the MPU read timing.

Table 1 Register Selection

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation (display data RAM → output register)
1	0	Writes data into input register as internal operation (input register → display data RAM)
0	1	Busy check. Read of status data.
0	0	Instruction

Busy Flag

Busy flag = 1 indicates that HD61202U is operating and no instructions except status read instruction can be accepted. The value of the busy flag is read out on DB7 by the status read instruction. Make sure that the busy flag is reset (0) before issuing instructions.

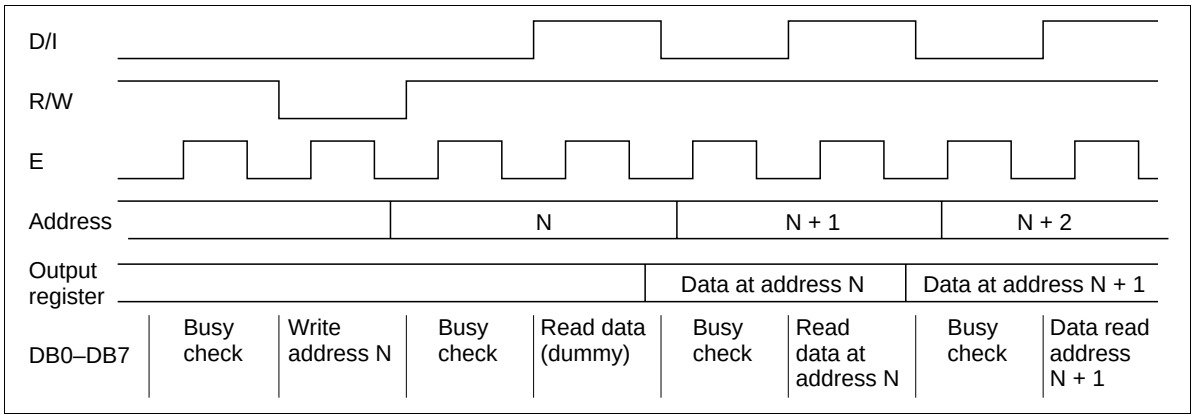


Figure 1 MPU Read Timing

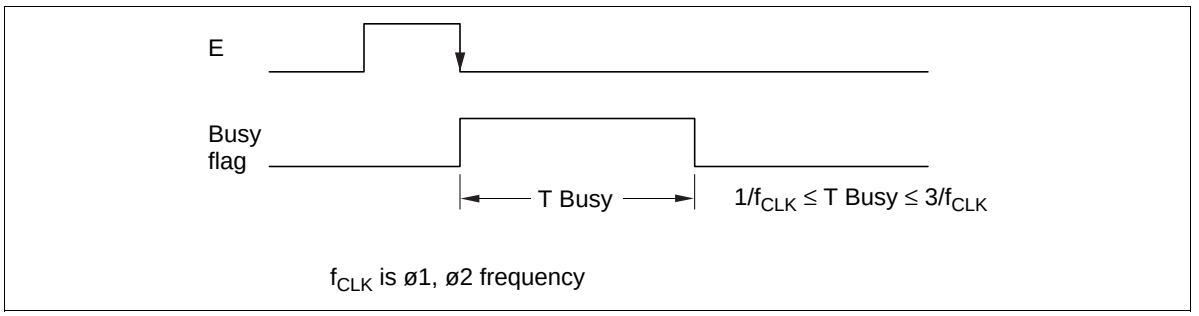


Figure 2 Busy Flag

Display On/Off Flip/Flop

The display on/off flip/flop selects one of two states, on state and off state of segments Y1 to Y64. In on state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments disappear in off state independent of the data in RAM. It is controlled by display on/off instruction. $\overline{RST}$ signal = 0 sets the segments in off state. The status of the flip/flop is output to DB5 by status read instruction. Display on/off instruction does not influence data in RAM. To control display data latch by this flip/flop, CL signal (display synchronous signal) should be input correctly.

Display Start Line Register

The display start line register specifies the line in RAM which corresponds to the top line of LCD panel, when displaying contents in display data RAM on the LCD panel. It is used for scrolling of the screen.

6-bit display start line information is written into this register by the display start line set instruction. When high level of the FRM signal starts the display, the information in this register is transferred to the Z address counter, which controls the display address, presetting the Z address counter.

X, Y Address Counter

A 9-bit counter which designates addresses of the internal display data RAM. X address counter (upper 3 bits) and Y address counter (lower 6 bits) should be set to each address by the respective instructions.

1. X address counter
   Ordinary register with no count functions. An address is set by instruction.
2. Y address counter
   An Address is set by instruction and is increased by 1 automatically by R/W operations of display data. The Y address counter loops the values of 0 to 63 to count.

Display Data RAM

Stores dot data for display. 1-bit data of this RAM corresponds to light on (data = 1) and light off (data = 0) of 1 dot in the display panel. The correspondence between Y addresses of RAM and segment pins can be reversed by ADC signal.

As the ADC signal controls the Y address counter, reversing of the signal during the operation causes malfunction and destruction of the contents of register and data of RAM. Therefore, never fail to connect ADC pin to V_{CC} or GND when using.

Figure 3 shows the relations between Y address of RAM and segment pins in the cases of ADC = 1 and ADC = 0 (display start line = 0, 1/64 duty cycle).

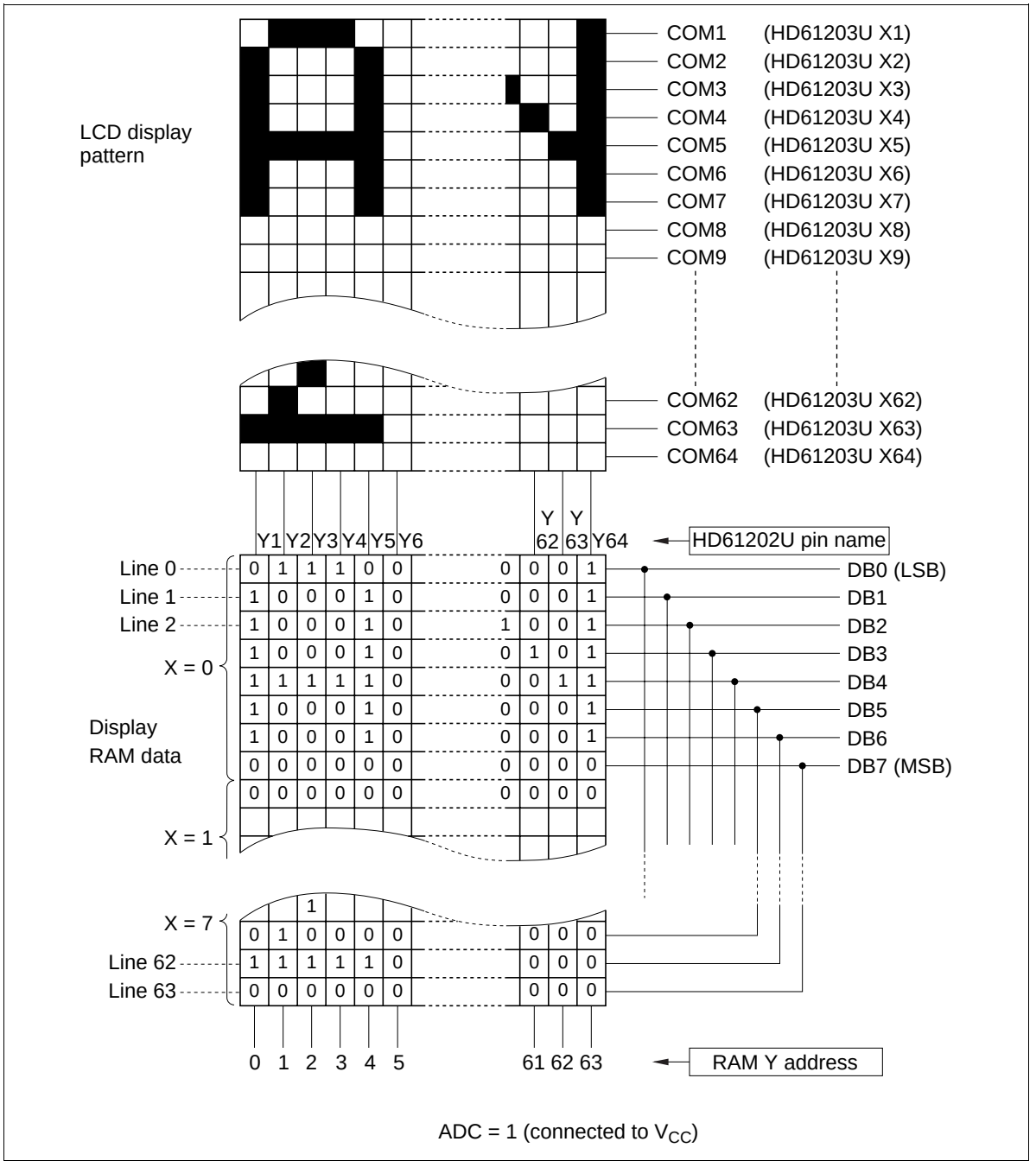


Figure 3 Relation between RAM Data and Display

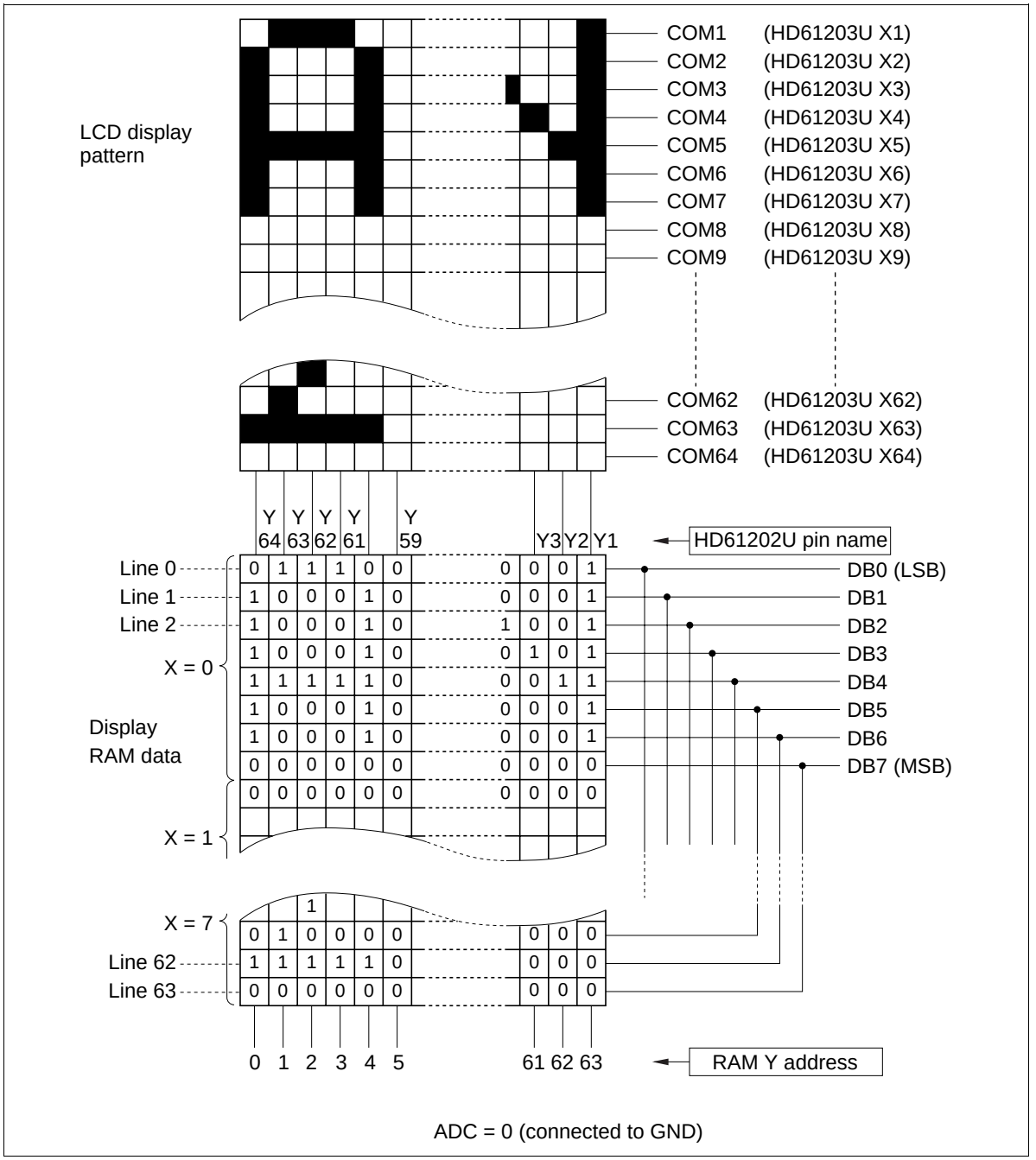


Figure 3 Relation between RAM Data and Display (cont)

Z Address Counter

The Z address counter generates addresses for outputting the display data synchronized with the common signal. This counter consists of 6 bits and counts up at the fall of the CL signal. At the high level of FRM, the contents of the display start line register is present at the Z counter.

Display Data Latch

The display data latch stores the display data temporarily that is output from display data RAM to the liquid crystal driving circuit. Data is latched at the rise of the CL signal. The display on/off instruction controls the data in this latch and does not influence data in dicsplay data RAM.

Liquid Crystal Display Driver Circuit

The combination of latched display data and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3, and V4 to be output.

Reset

The system can be initialized by setting $\overline{\text{RST}}$ terminal at low level when turning power on.

1. Display off
2. Set display start line register line 0.

While $\overline{\text{RST}}$ is low level, no instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4 = 0 (clear RESET) and DB7 = 0 (ready) by status read instruction.

Display Control Instructions

Outline

Table 2 shows the instructions. Read/write (R/W) signal, data/instruction (D/I) signal, and data bus signals (DB0 to DB7) are also called instructions because the internal operation depends on the signals from the MPU.

These explanations are detailed in the following pages. Generally, there are following three kinds of instructions:

1. Instruction to set addresses in the internal RAM
2. Instruction to transfer data from/to the internal RAM
3. Other instructions

In general use, the second type of instruction is used most frequently. Since Y address of the internal RAM is increased by 1 automatically after writing (reading) data, the program can be shortened. During the execution of an instruction, the system cannot accept instructions other than status read instruction. Send instructions from MPU after making sure that the busy flag is 0, which is proof that an instruction is not being executed.

Table 2 Instructions

Instructions	Code R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Functions	
Display on/off	0	0	0	0	1	1	1	1	1	1/0	Controls display on/off. RAM data and internal status are not affected. 1: on, 0: off.	
Display start line	0	0	1	1	Display start line (0–63)						Specifies the RAM line displayed at the top of the screen.	
Set page (X address)	0	0	1	0	1	1	1	Page (0–7)			Sets the page (X address) of RAM at the page (X address) register.	
Set Y address	0	0	0	1	Y address (0–63)						Sets the Y address in the Y address counter.	
Status read	1	0	Busy	0	ON/ OFF	Reset	0	0	0	0	Reads the status. RESET 1: Reset 0: Normal ON/OFF 1: Display off 0: Display on Busy 1: Internal operation 0: Ready	
Write display data	0	1	Write data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM.	Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
Read display data	1	1	Read data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.	

Note: Busy time varies with the frequency (f_{CLK}) of ø1, and ø2.
($1/f_{CLK} \leq T_{BUSY} \leq 3/f_{CLK}$)

Detailed Explanation

Display On/Off

	R/W	D/I	DB7	·····	DB0
Code	0	0	0	0	1	1	1	1	1	D
			MSB							LSB

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D = 0, it remains in the display data RAM. Therefore, you can make it appear by changing D = 0 into D = 1.

Display Start Line

	R/W	D/I	DB7	·····	DB0
Code	0	0	1	1	A	A	A	A	A	A
			MSB							LSB

Z address AAAAAA (binary) of the display data RAM is set in the display start line register and displayed at the top of the screen. Figure 4 shows examples of display (1/64 duty cycle) when the start line = 0–3. When the display duty cycle is 1/64 or more (ex. 1/32, 1/24 etc.), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

Set Page (X Address)

	R/W	D/I	DB7	·····	DB0
Code	0	0	1	0	1	1	1	A	A	A
			MSB							LSB

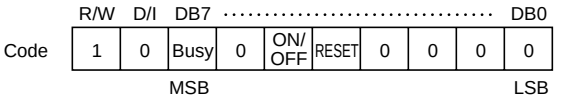
X address AAA (binary) of the display data RAM is set in the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set. See Figure 5.

Set Y Address

	R/W	D/I	DB7	·····	DB0
Code	0	0	0	1	A	A	A	A	A	A
			MSB							LSB

Y address AAAAAA (binary) of the display data RAM is set in the Y address counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

Status Read



- Busy

  When busy is 1, the LSI is executing internal operations. No instructions are accepted while busy is 1, so you should make sure that busy is 0 before writing the next instruction.

- ON/OFF

  Shows the liquid crystal display conditions: on condition or off condition.

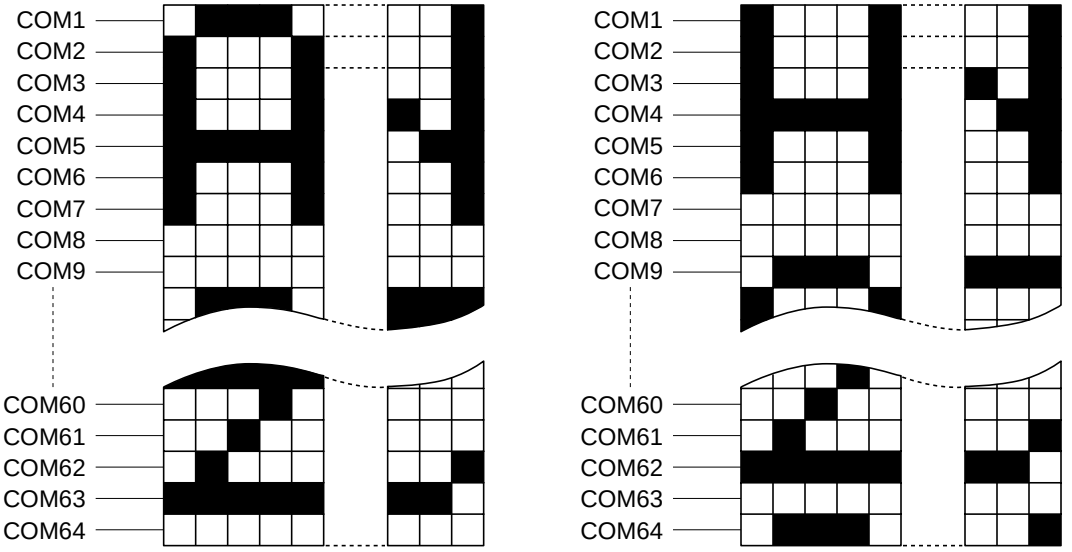
  When on/off is 1, the display is in off condition.

  When on/off is 0, the display is in on condition.

- RESET

  RESET = 1 shows that the system is being initialized. In this condition, no instructions except status read can be accepted.

  RESET = 0 shows that initializing has finished and the system is in the usual operation condition.



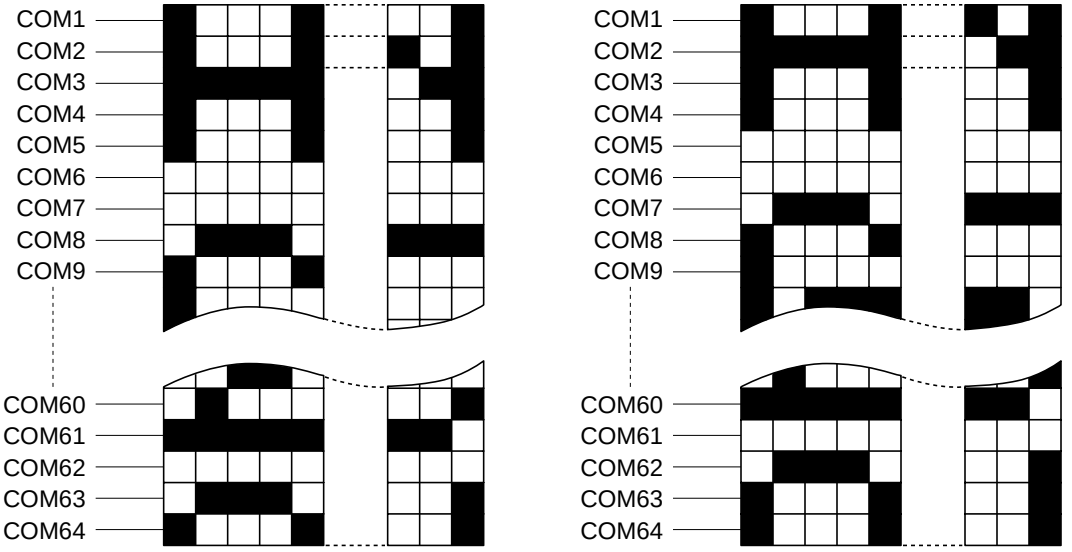


Figure 4 Relation between Start Line and Display

Write Display Data

	R/W	D/I	DB7	·····	DB0
Code	0	1	D		D
			MSB		LSB

Writes 8-bit data DDDDDDDD (binary) into the display data RAM. Then Y address is increased by 1 automatically.

Read Display Data

	R/W	D/I	DB7	·····	DB0
Code	1	1	D		D
			MSB		LSB

Reads out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.

One dummy read is necessary right after the address setting. For details, refer to the explanation of output register in “Function of Each Block”.

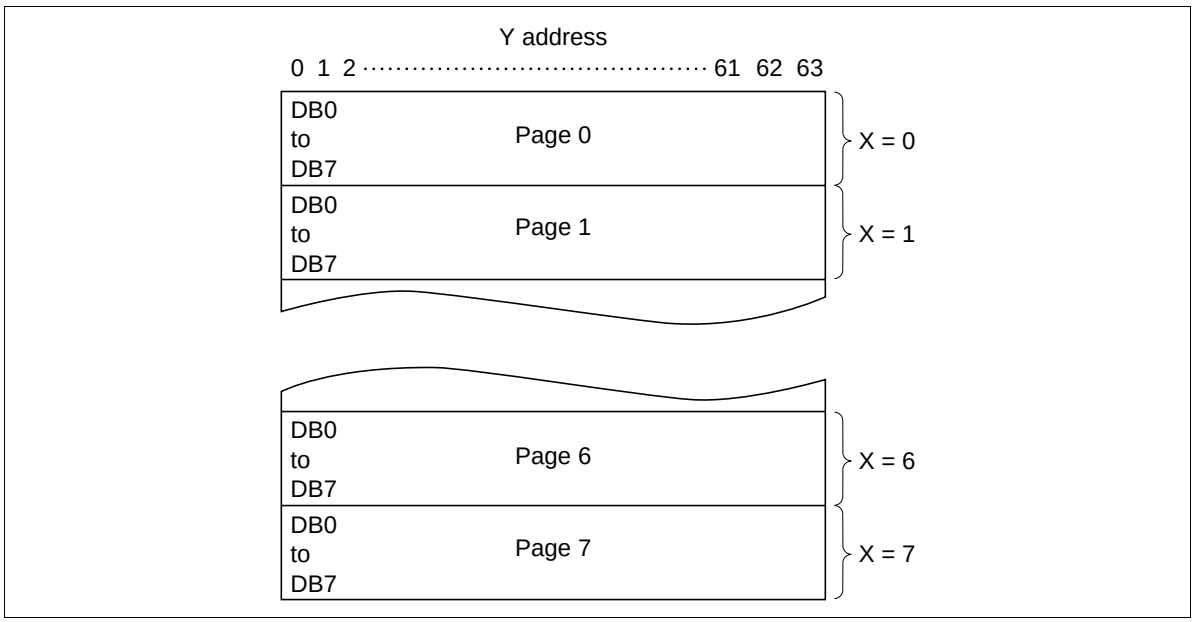
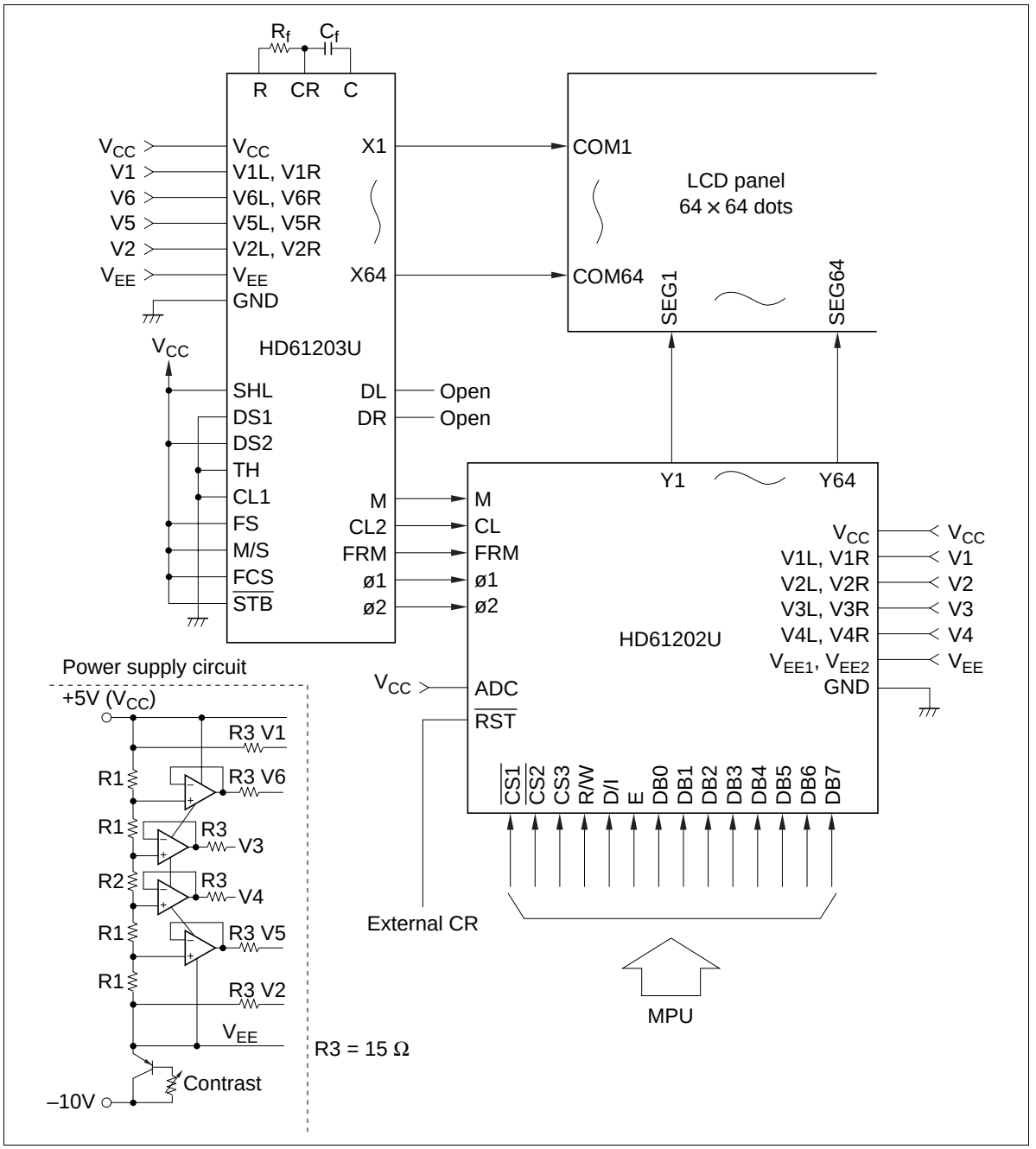
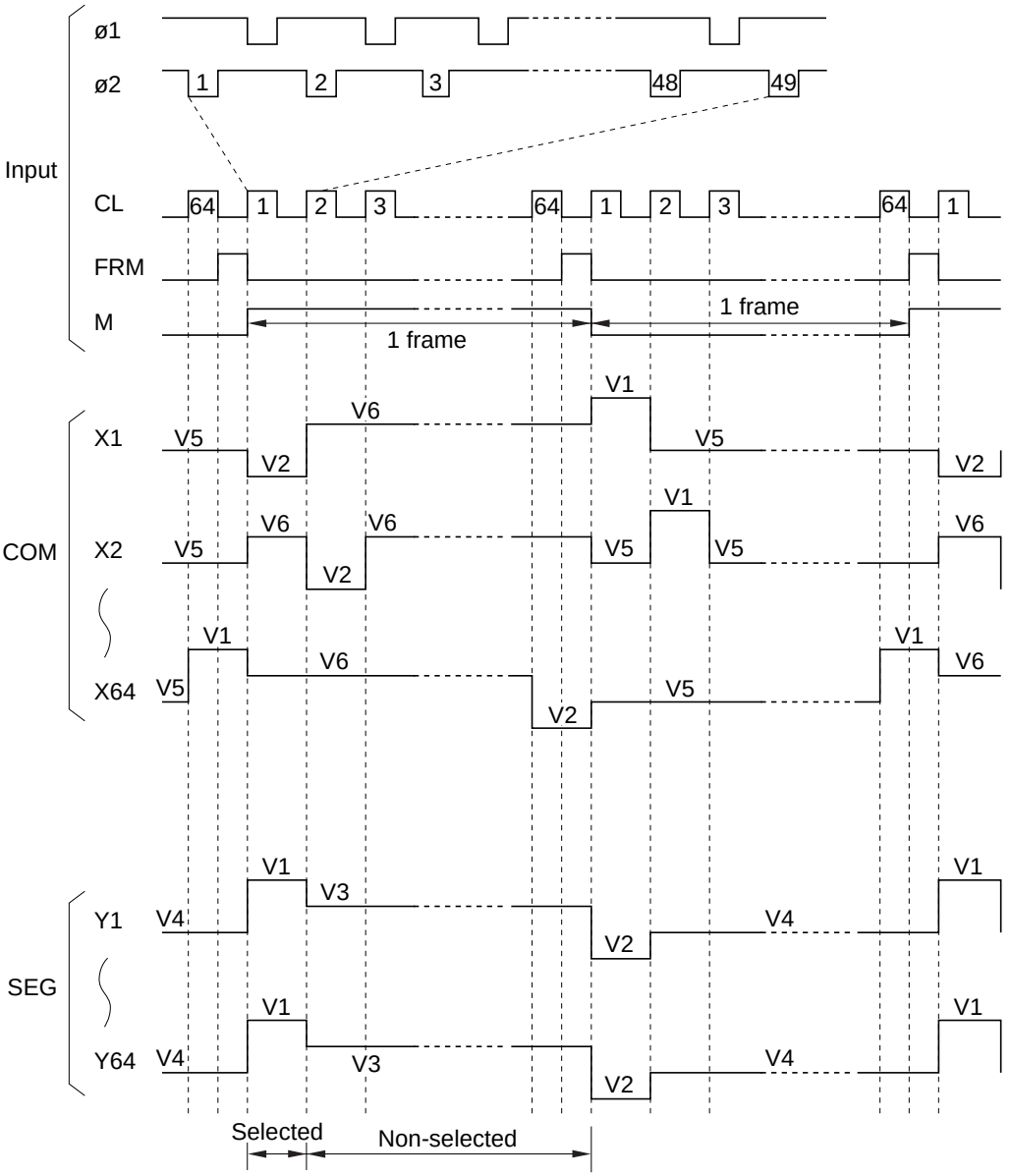


Figure 5 Address Configuration of Display Data RAM

Use of HD61202U

Interface with HD61203 (1/64 Duty Cycle)





The waveforms of Y1 to Y64 outputs vary with the display data. In this example, the top line of the panel lights up and other dots do not.

Figure 6 LCD Driver Timing Chart (1/64 Duty Cycle)

Interface with CPU

1. Example of Connection with H8/536S

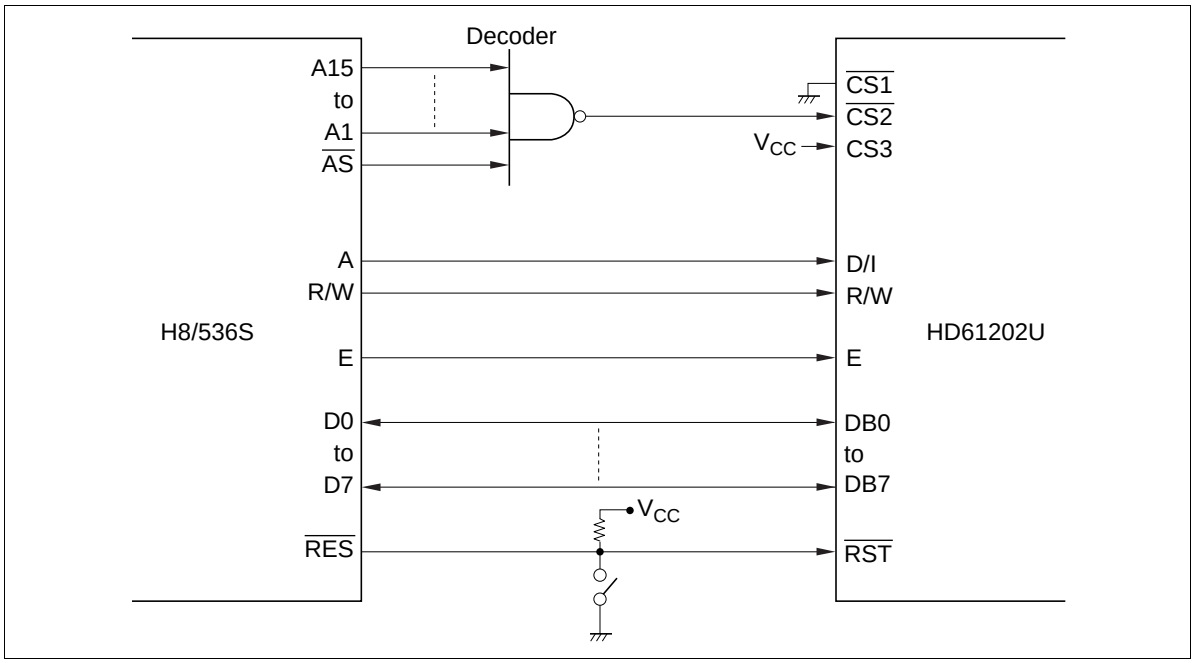


Figure 7 Example of Connection with H8/536S

Example of Application

In this example, two HD61203s output the equivalent waveforms. So, stand-alone operation is possible. In this case, connect COM1 and COM65 to X1, COM2 and COM66 to X2, ..., and COM64 and COM128 to X64. However, for the large screen display, it is better to drive in 2 rows as in this example to guarantee the display quality.

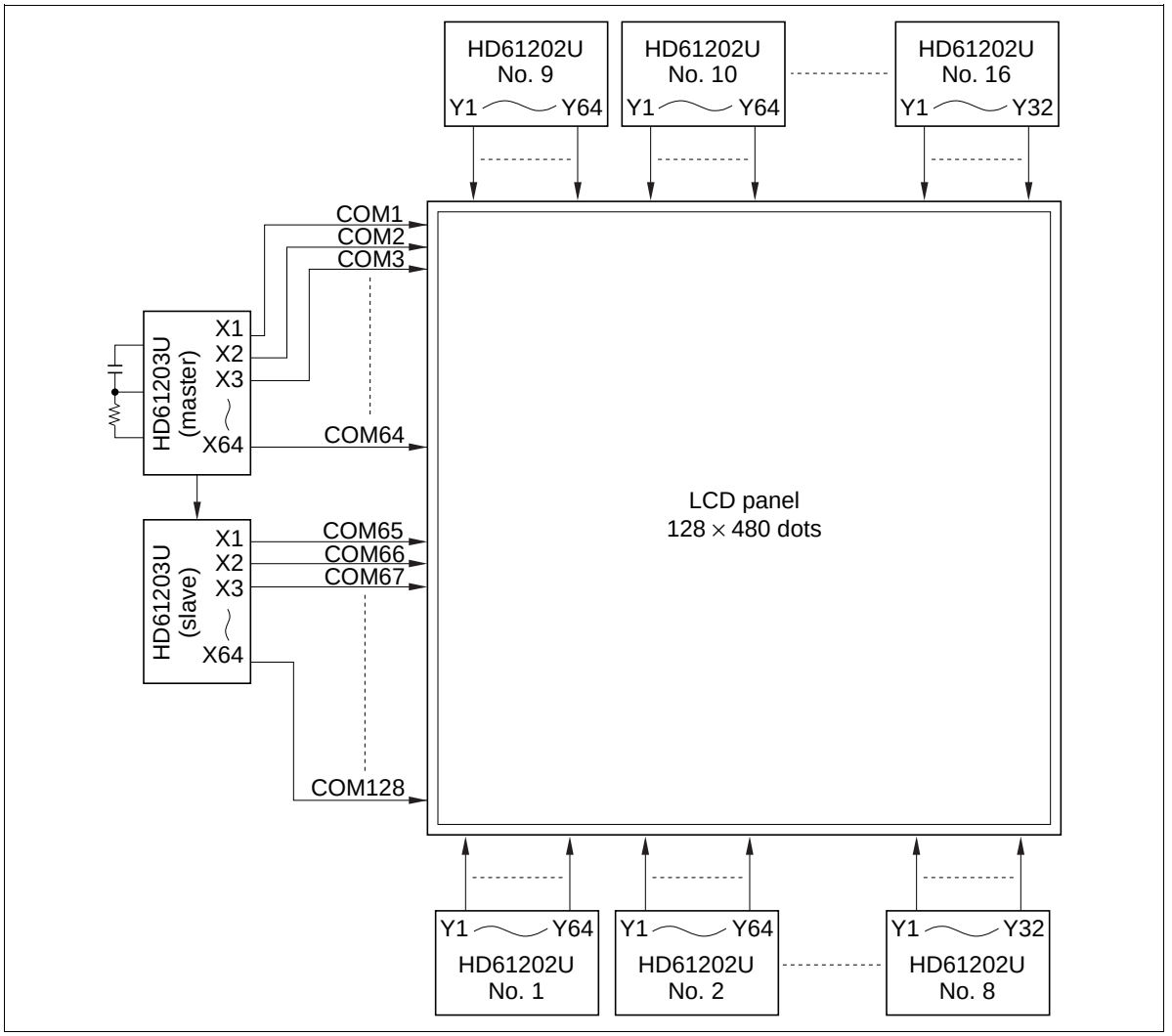


Figure 8 Application Example

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	–0.3 to +7.0	V	2
	V_{EE1} V_{EE2}	V_{CC} – 17.0 to V_{CC} + 0.3	V	3
Terminal voltage (1)	VT1	V_{EE} – 0.3 to V_{CC} + 0.3	V	4
Terminal voltage (2)	VT2	–0.3 to V_{CC} + 0.3	V	2, 5
Operating temperature	T_{opr}	–30 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: 1. LSIs may be destroyed if they are used beyond the absolute maximum ratings.
In ordinary operation, it is desirable to use them within the recommended operation conditions.
Useing them beyond these conditions may cause malfunction and poor reliability.

2. All voltage values are referenced to GND = 0V.
3. Apply the same supply voltage to V_{EE1} and V_{EE2}.
4. Applies to V1L, V2L, V3L, V4L, V1R, V2R, V3R, and V4R.
Maintain
$V_{CC} \geq V1L = V1R \geq V3L = V3R \geq V4L = V4R \geq V2L = V2R \geq V_{EE}$
5. Applies to M, FRM, CL, $\overline{RST}$, ADC, ø1, ø2, $\overline{CS1}$, $\overline{CS2}$, CS3, E, R/W, D/I, and DB0–DB7.

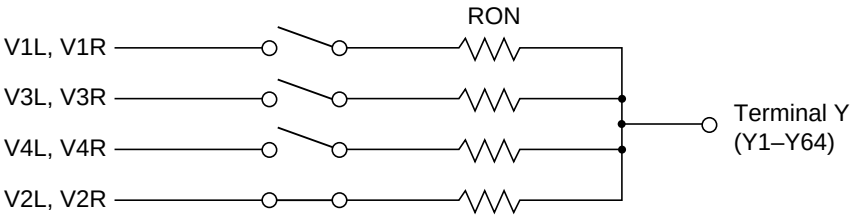
Electrical Characteristics (GND = 0V, V_{CC} = 2.7 ~ 5.5V, V_{CC} – V_{EE} = 8.0 to 16.0V, Ta = –30 ~ +75°C)[*8]

Item	Symbol	Limit Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	VIHC	0.7V_{CC}	—	V_{CC}	V	V_{CC} = 2.7V~5.5V	1
	VIHT	0.7V_{CC}	—	V_{CC}	V	V_{CC} = 2.7V~4.5V	2
		2.0	—	V_{CC}	V	V_{CC} = 4.5V~5.5V	2
Input low voltage	VILC	0.0		0.3V_{CC}	V	V_{CC} = 2.7V~5.5V	1
	VILT	0.0	—	0.5	V	V_{CC} = 2.7V~4.5V	2
		0.0		0.8	V	V_{CC} = 4.5V~5.5V	2
Output high voltage	VOH	0.75V_{CC}	—	—	V	I_{OH} = –100 µA, V_{CC} = 2.7V~4.5V	3
		2.4	—	—	V	I_{OH} = –205 µA V_{CC} = 4.5V~5.5V	3
Output low voltage	VOL	—		0.2V_{CC}	V	I_{OL} = 100 uA, V_{CC} = 2.7V~4.5V	3
		—	—	0.4	V	I_{OL} = 1.2mA, V_{CC} = 4.5V~5.5V	3
Input leakage current	I_{IL}	–1	—	1	µA	Vin = GND ~ V_{CC}	4
Three-state (off) input current	I_{TSL}	–5	—	5	µA	Vin = GND ~ V_{CC}	5
Liquid crystal supply leakage current	I_{LSL}	–2	—	2	µA	Vin = V_{EE}–V_{CC}	6
Driver on resistance	R_{ON}	—	—	7.5	kΩ	±I_{LOAD} = 0.1 mA, V_{CC}–V_{EE} = 15V	8
Dissipation current	I_{CC} (1)	—	—	100	µA	During display	7
	I_{CC} (2)	—	—	500	µA	During access, Cycle = 1MHz	7

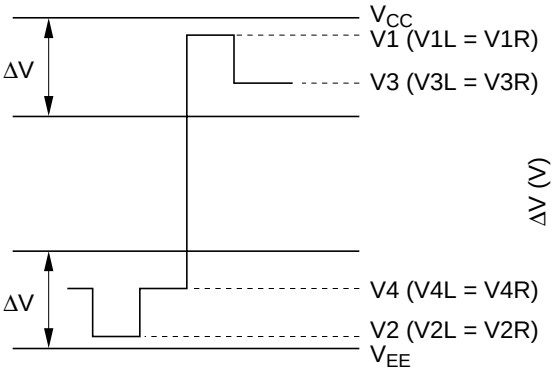
Notes:
1. Applies to M, FRM, CL, RST, ø1, and ø2.
2. Applies to CS1, CS2, CS3, E, R/W, D/I, and DB0–DB7.
3. Applies to DB0–DB7.
4. Applies to terminals except for DB0–DB7.
5. Applies to DB0–DB7 at high impedance.
6. Applies to V1L–V4L and V1R–V4R.
7. Specified when LCD is in 1/64 duty cycle mode.
   Operation frequency: f_{CLK} = 250 kHz (ø1 and ø2 frequency)
   Frame frequency: f_M = 70 Hz (FRM frequency)
   Specified in the state of
   Output terminal: Not loaded
   Input level: VIH = V_{CC} (V)
   VIL = GND (V)
   Measured at V_{CC} terminal
8. Specified at +75°C for die products.

9. Resistance between terminal Y and terminal V (one of V1L, V1R, V2L, V2R, V3L, V3R, V4L, and V4R) when load current flows through one of the terminals Y1 to Y64. This value is specified under the following condition:

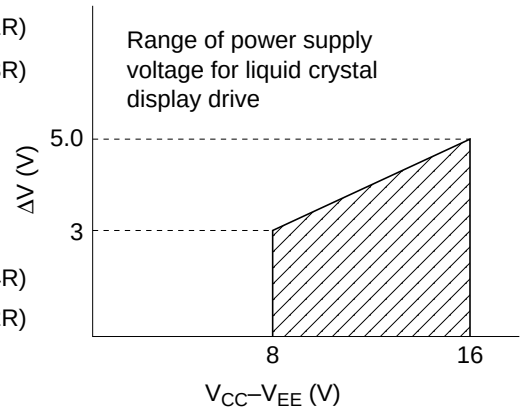
$V_{CC}–V_{EE}$ = 15.0V
V1L = V1R, V3L = V3R = V_{CC}–2/7 ($V_{CC}–V_{EE}$)
V2L = V2R, V4L = V4R = V_{CC}+2/7 ($V_{CC}–V_{EE}$)



The following is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to V1L = V1R and V3L = V3R and negative voltage to V2L = V2R and V4L = V4R within the ΔV range. This range allows stable impedance on driver output (RON). Notice that ΔV depends on power supply voltage $V_{CC}–V_{EE}$.



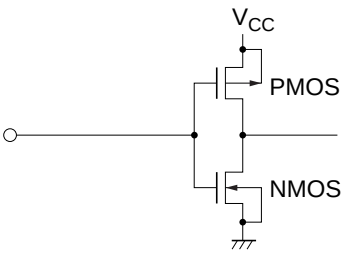
Correlation between driver output waveform and power supply voltages for liquid crystal display drive



Correlation between power supply voltage $V_{CC}–V_{EE}$ and ΔV

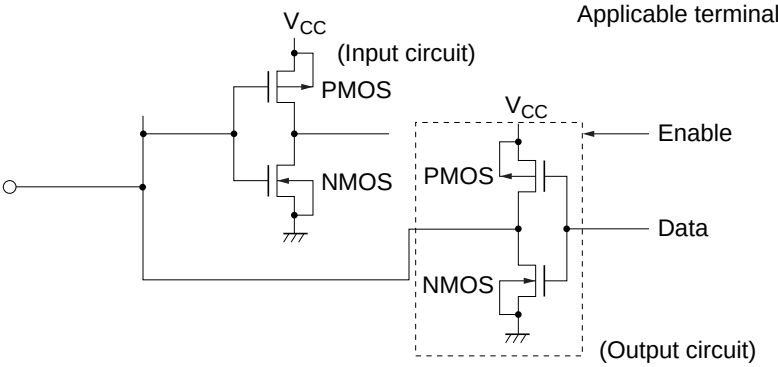
Terminal Configuration

Input Terminal



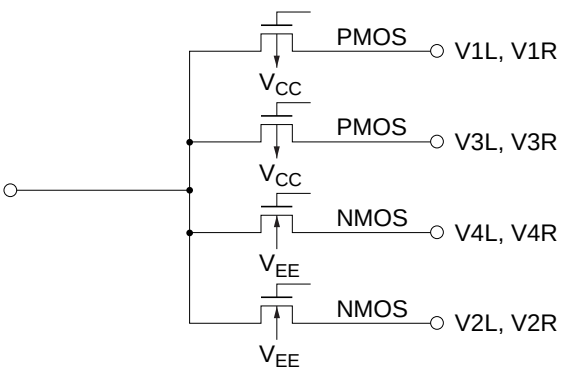
Applicable terminals:
M, FRM, CL, $\overline{RST}$, ø1, ø2, $\overline{CS1}$, $\overline{CS2}$, CS3,
E, R/W, D/I, ADC

Input/Output Terminal



Applicable terminals: DB0–DB7

Output Terminal



Applicable terminals:
Y1–Y64

Interface AC Characteristics

MPU Interface (GND = 0V, V_{CC} = 2.7 to 5.5V, Ta = –30 to +75°C)*

Item	Symbol	Min	Typ	Max	Unit	Note
E cycle time	t_{CYC}	1000	—	—	ns	Fig. 10, Fig. 11
E high level width	P_{WEH}	450	—	—	ns	
E low level width	P_{WEL}	450	—	—	ns	
E rise time	t_r	—	—	25	ns	
E fall time	t_f	—	—	25	ns	
Address setup time	t_{AS}	140	—	—	ns	
Address hold time	t_{AH}	10	—	—	ns	
Data setup time	t_{DSW}	200	—	—	ns	Fig. 10
Data delay time	t_{DDR}	—	—	320	ns	Fig. 11, Fig. 12
Data hold time (write)	t_{DHW}	10	—	—	ns	Fig. 10
Data hold time (read)	t_{DHR}	20	—	—	ns	Fig. 11

Note: Specified at +75°C for die products.

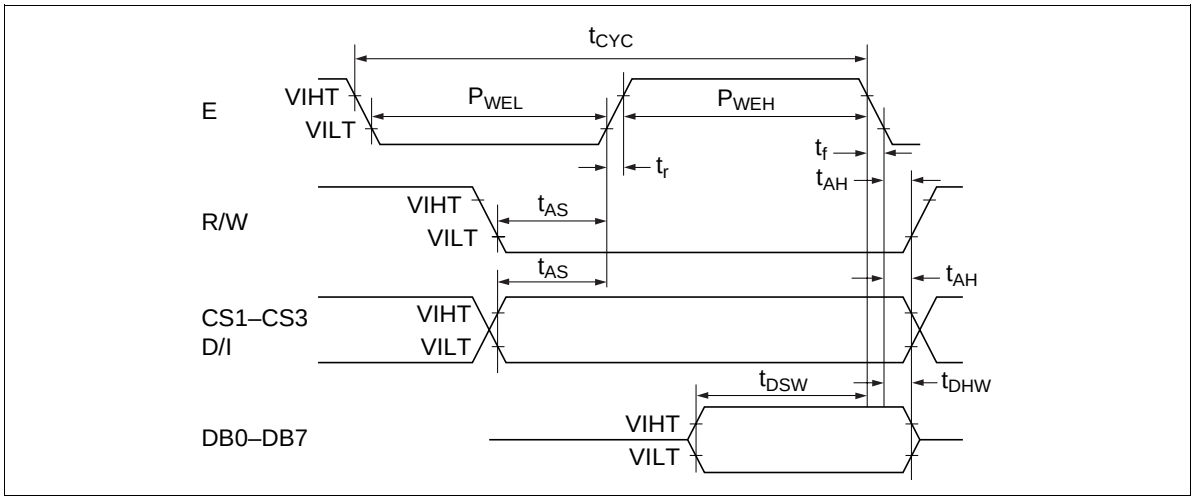


Figure 9 MPU Write Timing

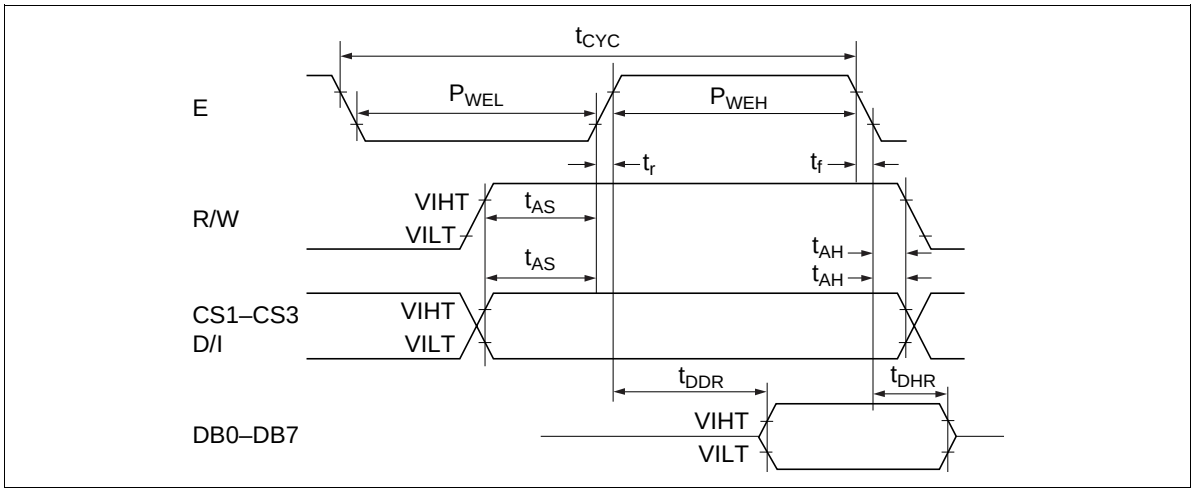


Figure 10 MPU Read Timing

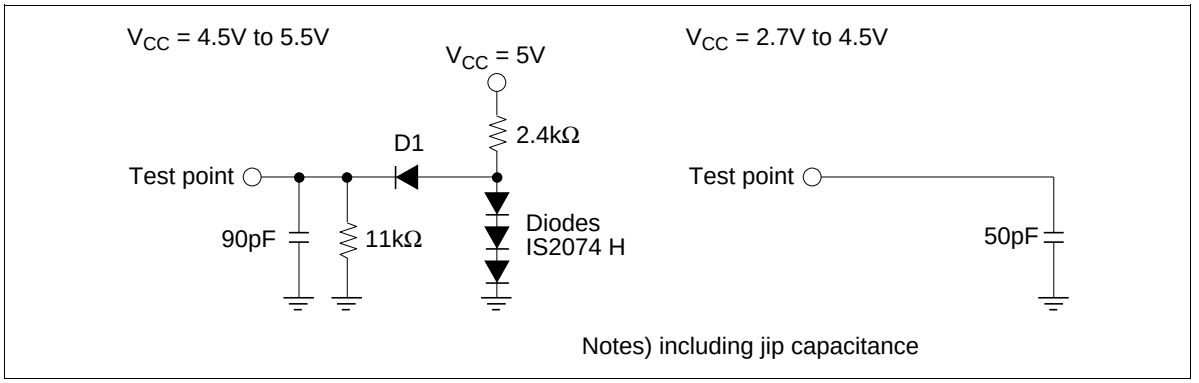


Figure 11 DB0–DB7: Load Circuit

Clock Timing (GND = 0V, V_{CC} = 2.7 to 5.5V, Ta = –30 to +75°C)*

Item	Symbol	Limit			Unit	Test Condition
		Min	Typ	Max		
ø1, ø2 cycle time	t_{cyc}	2.5	—	20	µs	Fig. 13
ø1 low level width	$t_{WLø1}$	625	—	—	ns	
ø2 low level width	$t_{WLø2}$	625	—	—	ns	
ø1 high level width	$t_{WHø1}$	1875	—	—	ns	
ø2 high level width	$t_{WHø2}$	1875	—	—	ns	
ø1–ø2 phase difference	t_{D12}	625	—	—	ns	
ø2–ø1 phase difference	t_{D21}	625	—	—	ns	
ø1, ø2 rise time	t_r	—	—	150	ns	
ø1, ø2 fall time	t_f	—	—	150	ns	

Note: Specified at +75°C for die products.

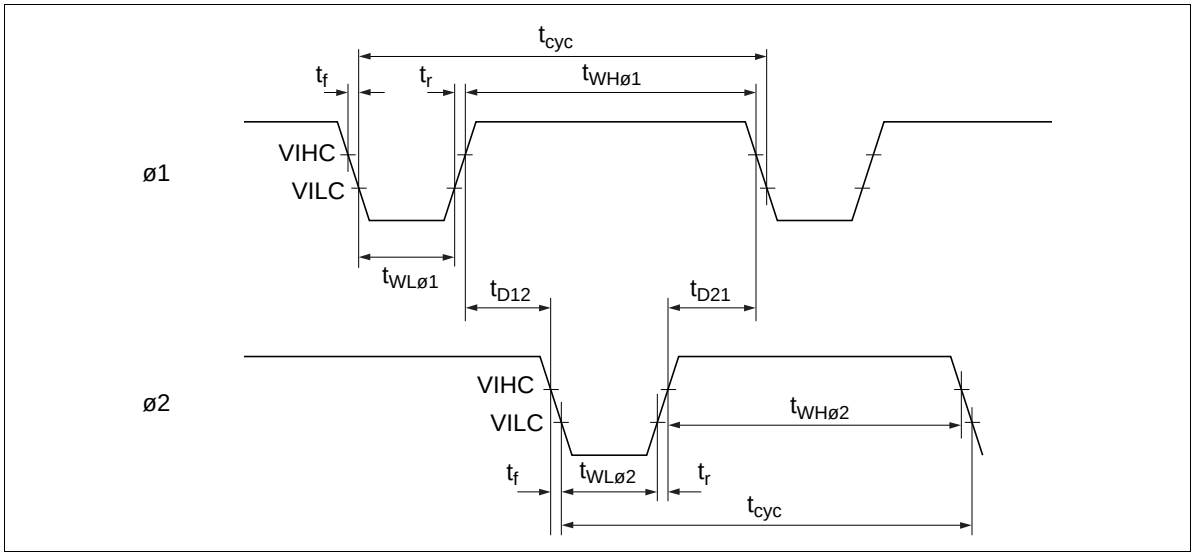


Figure 12 External Clock Waveform

Display Control Timing (GND = 0V, V_{CC} = 2.7 to 5.5V, Ta = –30 to +75°C)*

Item	Symbol	Limit			Unit	Test Condition
		Min	Typ	Max		
FRM delay time	t_{DFRM}	–2	—	+2	µs	Fig. 14
M delay time	t_{DM}	–2	—	+2	µs	
CL low level width	t_{WLCL}	35	—	—	µs	
CL high level width	t_{WHCL}	35	—	—	µs	

Note: Specified at +75°C for die products.

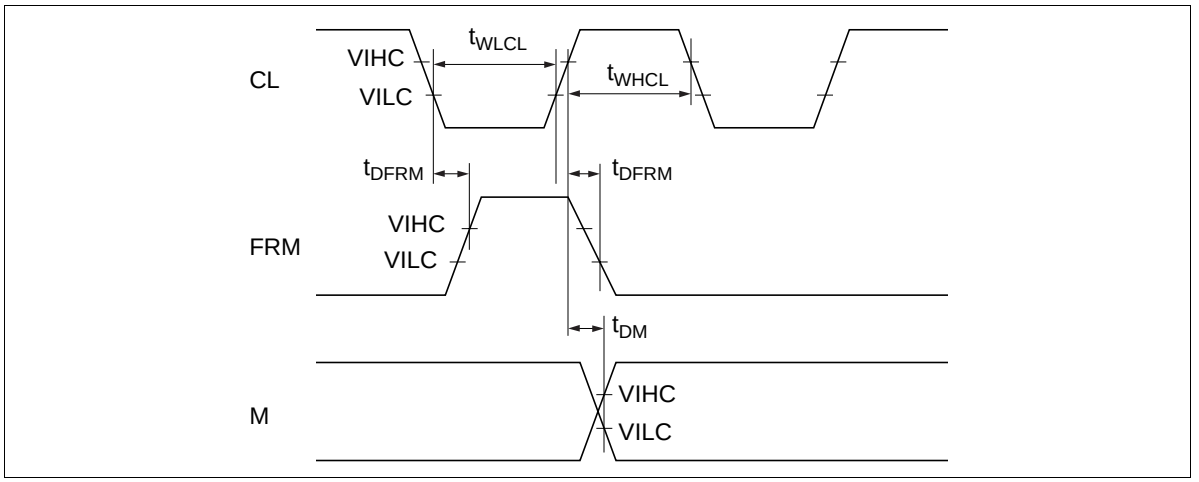


Figure 13 Display Control Signal Waveform

Reset Timing (GND = 0V, V_{CC} = 2.7 to 5.5V, Ta = –30 to +75°C)*

Item	Symbol	Min	Typ	Max	Unit
Reset time	t_{RST}	1.0	—	—	µs

Do not fail to set the system again because RESET during operation may destroy the data in all the registers except on/off register and in RAM.

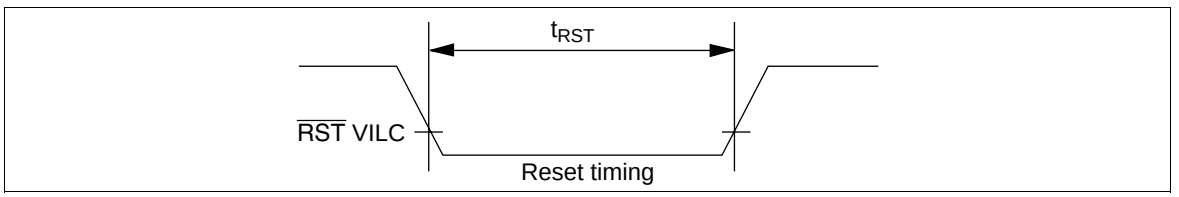


Figure 14 Reset Timing

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