2114A
1024 x 4 BIT STATIC RAM

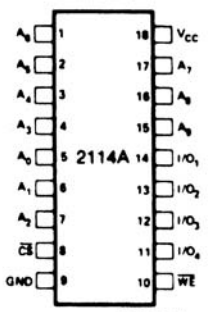
	2114AL-1	2114AL-2	2114AL-3	2114AL-4	2114A-4	2114A-5
Max. Access Time (ns)	100	120	150	200	200	250
Max. Current (mA)	40	40	40	40	70	70

- **HMOS II Technology**
- **Low Power, High Speed**
- **Identical Cycle and Access Times**
- **Single +5V Supply ±10%**
- **High Density 18 Pin Package**
- **Completely Static Memory—No Clock or Timing Strobe Required**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **High Reliability Plastic or Cerdip**
- **Available in EXPRESS**
  - **Standard Temperature Range**
  - **Extended Temperature Range**

The Intel 2114A is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using HMOS II, a high performance MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding, therefore it requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2114A is designed for memory applications where the high performance and high reliability of HMOS II, low cost, large bit storage, and simple interfacing are important design objectives. The 2114A is assembled in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.



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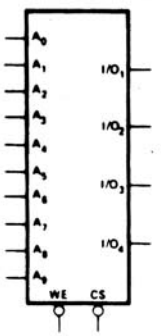
Pin Configuration



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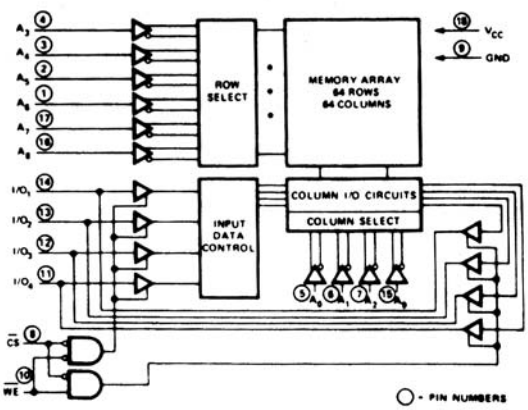
Logic Symbol

Pin Names

A_0–A_9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
I/O_1–I/O_4	DATA INPUT/OUTPUT	



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Block Diagram

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin
With Respect to Ground ..... −3.5V to +7V
Power Dissipation 1.0W
D.C. Output Current ..... 5 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±10%, unless otherwise noted

Symbol	Parameter	2114AL-1/L-2/L-3/L-4			2114A-4/-5			Unit	Conditions
		Min	Typ(1)	Max	Min	Typ(1)	Max		
$\|I_{LI}\|$	Input Load Current (All Input Pins)		0.01	1			1	µA	V_{IN} = 0V to 5.5V
$\|I_{LO}\|$	I/O Leakage Current		0.1	10			10	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = 0V to 5.5V
I_{CC}	Power Supply Current		25	40		50	70	mA	V_{CC} = max, $I_{I/O}$ = 0 mA, T_A = 0°C
V_{IL}	Input Low Voltage	−3.0		0.8	−3.0		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
I_{OL}	Output Low Current	4.0	9.0		4.0	9.0		mA	V_{OL} = 0.4V
I_{OH}	Output High Current	−2.0	−2.5		−2.0	−2.5		mA	V_{OH} = 2.4V
I_{OS}(2)	Output Short Circuit Current			40			40	mA	V_{OUT} = GND

NOTES:
1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. Duration not to exceed 1 second.

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Max	Unit	Conditions
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V

NOTE:
This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels ..... 0.8V to 2.0V
Input Rise and Fall Times ..... 10 ns
Input and Output Timing Levels ..... 0.8V to 2.0V
Output Load ..... 1 TTL Gate and C_L = 100 pF

LOAD FOR T_{OTD} AND T_{OTW}

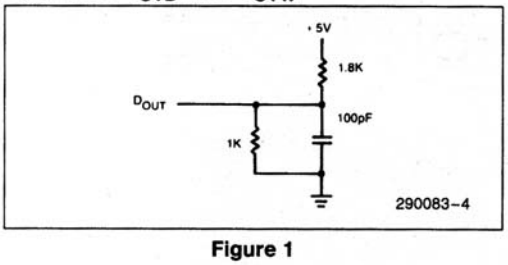


Figure 1

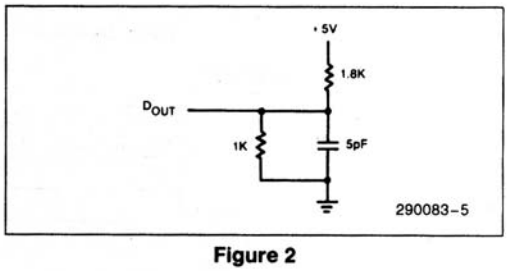


Figure 2

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%, unless otherwise noted.

READ CYCLE[1]

Symbol	Parameter	2114AL-1		2114AL-2		2114AL-3		2114A-4/L-4		2114A-5		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	100		120		150		200		250		ns
t_A	Access Time		100		120		150		200		250	ns
t_{CO}	Chip Selection to Output Valid		70		70		70		70		85	ns
t_{CX}[3]	Chip Selection to Output Active	10		10		10		10		10		ns
t_{OTD}[3]	Output 3-state from Deselection		30		35		40		50		60	ns
t_{OHA}	Output Hold from Address Change	15		15		15		15		15		ns

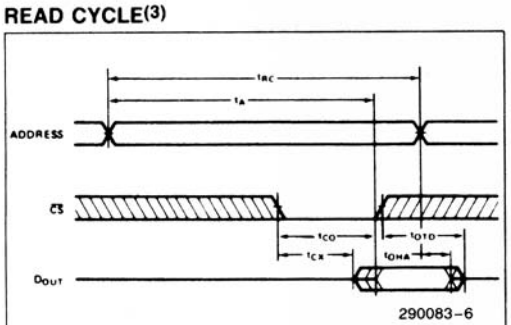
WRITE CYCLE[2]

Symbol	Parameter	2114AL-1		2114AL-2		2114AL-3		2114A-4/L-4		2114A-5		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	100		120		150		200		250		ns
t_W	Write Time	75		75		90		120		135		ns
t_{WR}	Write Release Time	0		0		0		0		0		ns
t_{OTW}[3]	Output 3-state from Write		30		35		40		50		60	ns
t_{DW}	Data to Write Time Overlap	70		70		90		120		135		ns
t_{DH}	Data Hold from Write Time	0		0		0		0		0		ns

NOTES:
1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.
3. Measured at ±500 mV with 1 TTL Gate and C_L = 5.00 pF.

WAVEFORMS

READ CYCLE[3]



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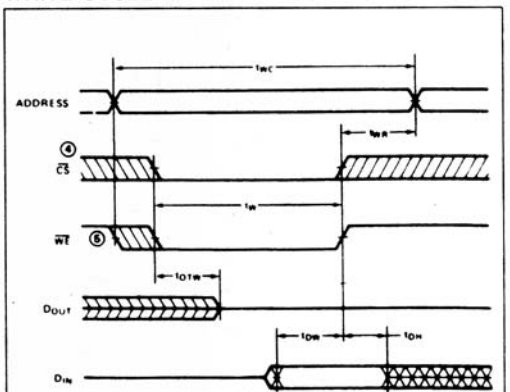
NOTES:
3. $\overline{WE}$ is high for a Read Cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
5. $\overline{WE}$ must be high during all address transitions.

WRITE CYCLE



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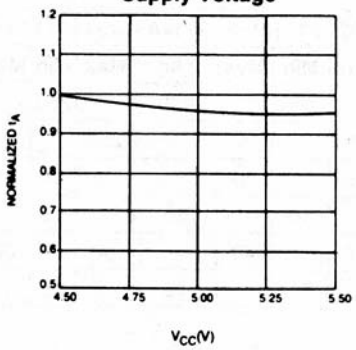
TYPICAL D.C. AND A.C. CHARACTERISTICS

Normalized Access Time vs Supply Voltage



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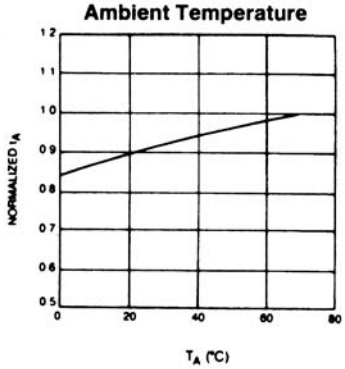
Normalized Access Time vs Ambient Temperature



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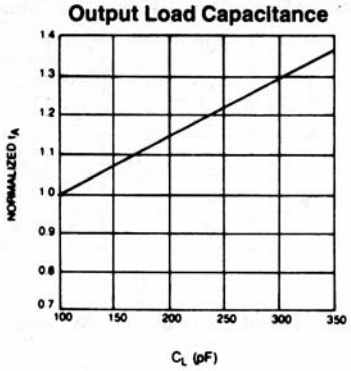
Normalized Access Time vs Output Load Capacitance



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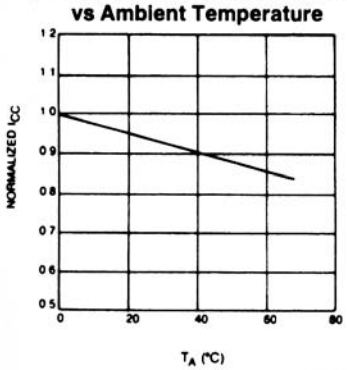
Normalized Power Supply Current vs Ambient Temperature



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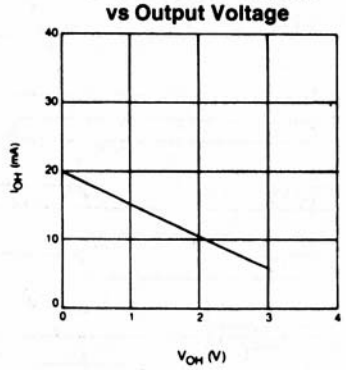
Output Source Current vs Output Voltage



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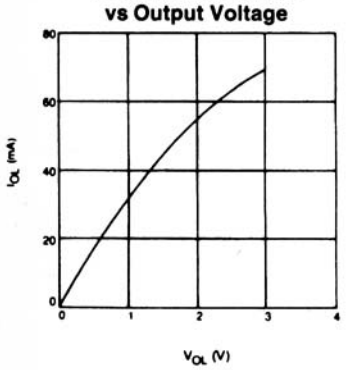
Output Sink Current vs Output Voltage



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