

**Document Title****512Kx8 bit Low Power full CMOS Static RAM****Revision History**

<b><u>Revision No.</u></b>	<b><u>History</u></b>	<b><u>Draft Date</u></b>	<b><u>Remark</u></b>
0.0	Initial draft	July 30, 2002	Preliminary
0.1	Revised - Added Commercial Product.	November 30, 2002	Preliminary
1.0	Finalized - Added Lead Free 32-SOP-525 Product - Changed Icc from 10mA to 5mA - Changed Icc1 from 8mA to 7mA - Changed Icc2 from 40mA to 30mA - Changed Isb from 3mA to 0.4mA - Changed Idr(Commercial) from 15 $\mu$ A to 12 $\mu$ A - Changed Idr(industrial) from 20 $\mu$ A to 12 $\mu$ A - Changed Idr(Automotive) from 30 $\mu$ A to 25 $\mu$ A	September 16, 2003	Final
2.0	Revised - Changed Isb1 of Automotive product from 30 $\mu$ A to 60 $\mu$ A - Changed Idr of Automotive product from 25 $\mu$ A to 30 $\mu$ A - Added Lead Free Products	March 27, 2005	Final

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## 512Kx8 bit Low Power full CMOS Static RAM

### FEATURES

- Process Technology: Full CMOS
- Organization: 512Kx8
- Power Supply Voltage: 4.5~5.5V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL compatible
- Package Type: 32-DIP-600, 32-SOP-525, 32-TSOP2-400F/R

### GENERAL DESCRIPTION

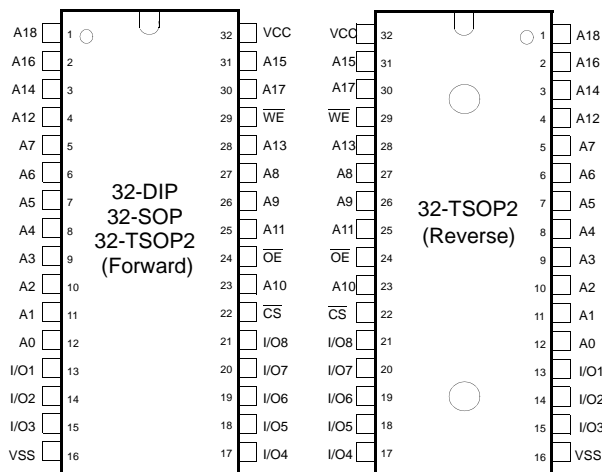
The K6X4008C1F families are fabricated by SAMSUNG's advanced full CMOS process technology. The families supports various operating temperature range and various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I <sub>SB1</sub> , Max)	Operating (I <sub>CC2</sub> , Max)	
K6X4008C1F-B	Commercial (0~70°C)	4.5~5.5V	55 <sup>1)</sup> /70ns	20μA	30mA	32-DIP-600, 32-SOP-525, 32-TSOP2-400F/R
K6X4008C1F-F	Industrial (-40~85°C)					
K6X4008C1F-Q	Automotive (-40~125°C)			60μA		32-SOP-525, 32-TSOP2-400F

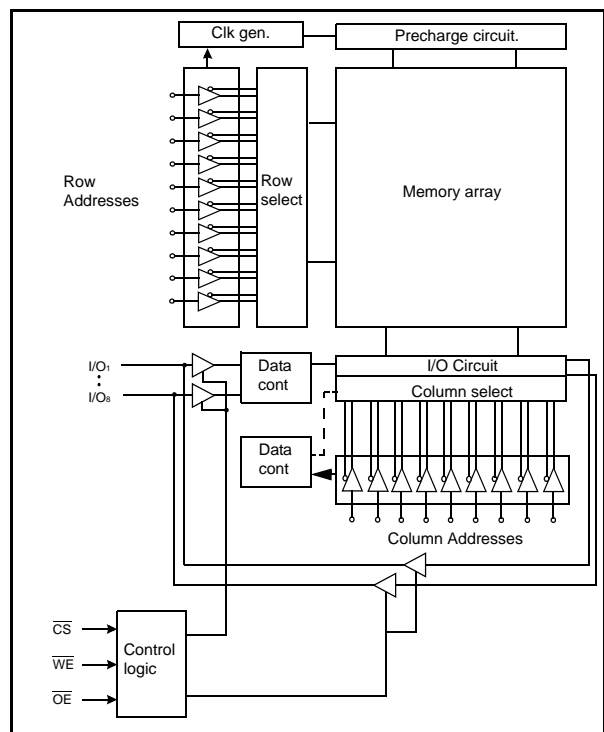
1. The parameter is measured with 50pF test load.

### PIN DESCRIPTION



Pin Name	Function
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
A0~A18	Address Inputs
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground

### FUNCTIONAL BLOCK DIAGRAM



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## PRODUCT LIST

Commercial Products(0~70°C)		Industrial Products(-40~85°C)		Automotive Products(-40~125°C)	
Part Name	Function	Part Name	Function	Part Name	Function
K6X4008C1F-DB55	32-DIP, 55ns, LL	K6X4008C1F-DF55	32-DIP, 55ns, LL	K6X4008C1F-GQ55	32-SOP, 55ns, L
K6X4008C1F-DB70	32-DIP, 70ns, LL	K6X4008C1F-DF70	32-DIP, 70ns, LL	K6X4008C1F-GQ70	32-SOP, 70ns, L
K6X4008C1F-GB55	32-SOP, 55ns, LL	K6X4008C1F-GF55	32-SOP, 55ns, LL	K6X4008C1F-BQ55	32-SOP, 55ns, L, LF
K6X4008C1F-GB70	32-SOP, 70ns, LL	K6X4008C1F-GF70	32-SOP, 70ns, LL	K6X4008C1F-BQ70	32-SOP, 70ns, L, LF
K6X4008C1F-BB55 <sup>1)</sup>	32-SOP, 55ns, LL, LF	K6X4008C1F-BF55 <sup>1)</sup>	32-SOP, 55ns, LL, LF	K6X4008C1F-VQ55	32-TSOP2-F, 55ns, L
K6X4008C1F-BB70 <sup>1)</sup>	32-SOP, 70ns, LL, LF	K6X4008C1F-BF70 <sup>1)</sup>	32-SOP, 70ns, LL, LF	K6X4008C1F-VQ70	32-TSOP2-F, 70ns, L
K6X4008C1F-VB55	32-TSOP2-F, 55ns, LL	K6X4008C1F-VF55	32-TSOP2-F, 55ns, LL	K6X4008C1F-UQ55	32-TSOP2-F, 55ns, L, LF
K6X4008C1F-VB70	32-TSOP2-F, 70ns, LL	K6X4008C1F-VF70	32-TSOP2-F, 70ns, LL	K6X4008C1F-UQ70	32-TSOP2-F, 70ns, L, LF
K6X4008C1F-UB55 <sup>1)</sup>	32-TSOP2-F, 55ns, LL, LF	K6X4008C1F-UF55 <sup>1)</sup>	32-TSOP2-F, 55ns, LL, LF		
K6X4008C1F-UB70 <sup>1)</sup>	32-TSOP2-F, 70ns, LL, LF	K6X4008C1F-UF70 <sup>1)</sup>	32-TSOP2-F, 70ns, LL, LF		
K6X4008C1F-MB55	32-TSOP2-R, 55ns, LL	K6X4008C1F-MF55	32-TSOP2-R, 55ns, LL		
K6X4008C1F-MB70	32-TSOP2-R, 70ns, LL	K6X4008C1F-MF70	32-TSOP2-R, 70ns, LL		

1. Lead Free Product

## FUNCTIONAL DESCRIPTION

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O Pin	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
L	H	H	High-Z	Output disbaled	Active
L	L	H	Dout	Read	Active
L	X <sup>1)</sup>	L	Din	Write	Active

1. X means don't care.( Must be in low or high state.)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> ,V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5V(max. 7.0V)	V	-
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.3 to 7.0	V	-
Power Dissipation	P <sub>D</sub>	1.0	W	-
Storage temperature	T <sub>STG</sub>	-65 to 150	°C	-
Operating Temperature	T <sub>A</sub>	0 to 70	°C	K6X4008C1F-B
		-40 to 85		K6X4008C1F-F
		-40 to 125		K6X4008C1F-Q

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.5 <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	-0.5 <sup>3)</sup>	-	0.8	V

Note:

- Commercial Product: T<sub>A</sub>=0 to 70°C, otherwise specified  
Industrial Product: T<sub>A</sub>=-40 to 85°C, otherwise specified  
Automotive Product: T<sub>A</sub>=-40 to 125°C, otherwise specified
- Overshoot: V<sub>CC</sub>+3.0V in case of pulse width ≤ 30ns
- Undershoot: -3.0V in case of pulse width ≤ 30ns
- Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	10	pF

- Capacitance is sampled, not 100% tested

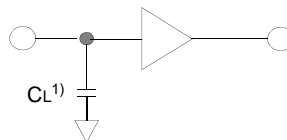
## DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CS}$ =V <sub>IH</sub> or $\overline{OE}$ =V <sub>IH</sub> or $\overline{WE}$ =V <sub>IL</sub> , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Operating power supply current	I <sub>CC</sub>	I <sub>IO</sub> =0mA, $\overline{CS}$ =V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> , Read	-	-	5	mA	
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100% duty, I <sub>IO</sub> =0mA $\overline{CS}$ ≤0.2V, V <sub>IN</sub> ≥0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	-	-	7	mA	
	I <sub>CC2</sub>	Cycle time=Min, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}$ =V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	-	-	30	mA	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4	V	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4	-	-	V	
Standby Current(TTL)	I <sub>SB</sub>	$\overline{CS}$ =V <sub>IH</sub> , Other inputs = V <sub>IL</sub> or V <sub>IH</sub>	-	-	0.4	mA	
Standby Current(CMOS)	I <sub>SB1</sub>	$\overline{CS}$ ≥V <sub>CC</sub> -0.2V, Other inputs=0~V <sub>CC</sub>	K6X4008C1F-B	-	-	20	μA
			K6X4008C1F-F	-	-		
			K6X4008C1F-Q	-	-	60	μA

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level: 0.8 to 2.4V  
 Input rising and falling time: 5ns  
 Input and output reference voltage: 1.5V  
 Output load (See right):  $C_L=100\text{pF}+1\text{TTL}$   
 $C_L=50\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

## AC CHARACTERISTICS

( $V_{CC}=4.5\sim 5.5\text{V}$ , Commercial product:  $T_A=0$  to  $70^\circ\text{C}$ , Industrial product:  $T_A=-40$  to  $85^\circ\text{C}$ , Automotive product:  $T_A=-40$  to  $125^\circ\text{C}$ )

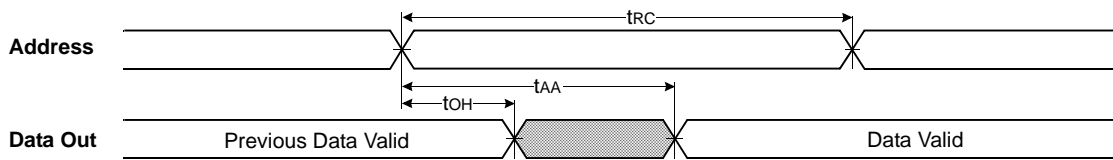
Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	t <sub>RC</sub>	55	-	70	-	ns
	Address access time	t <sub>AA</sub>	-	55	-	70	ns
	Chip select to output	t <sub>CO</sub>	-	55	-	70	ns
	Output enable to valid output	t <sub>OE</sub>	-	25	-	35	ns
	Chip select to low-Z output	t <sub>LZ</sub>	10	-	10	-	ns
	Output enable to low-Z output	t <sub>OLZ</sub>	5	-	5	-	ns
	Chip disable to high-Z output	t <sub>HZ</sub>	0	20	0	25	ns
	Output disable to high-Z output	t <sub>OHZ</sub>	0	20	0	25	ns
	Output hold from address change	t <sub>OH</sub>	10	-	10	-	ns
Write	Write cycle time	t <sub>WC</sub>	55	-	70	-	ns
	Chip select to end of write	t <sub>CW</sub>	45	-	60	-	ns
	Address set-up time	t <sub>AS</sub>	0	-	0	-	ns
	Address valid to end of write	t <sub>AW</sub>	45	-	60	-	ns
	Write pulse width	t <sub>WP</sub>	40	-	50	-	ns
	Write recovery time	t <sub>WR</sub>	0	-	0	-	ns
	Write to output high-Z	t <sub>WHZ</sub>	0	20	0	25	ns
	Data to write time overlap	t <sub>DW</sub>	25	-	30	-	ns
	Data hold from write time	t <sub>DH</sub>	0	-	0	-	ns
	End write to output low-Z	t <sub>OW</sub>	5	-	5	-	ns

## DATA RETENTION CHARACTERISTICS

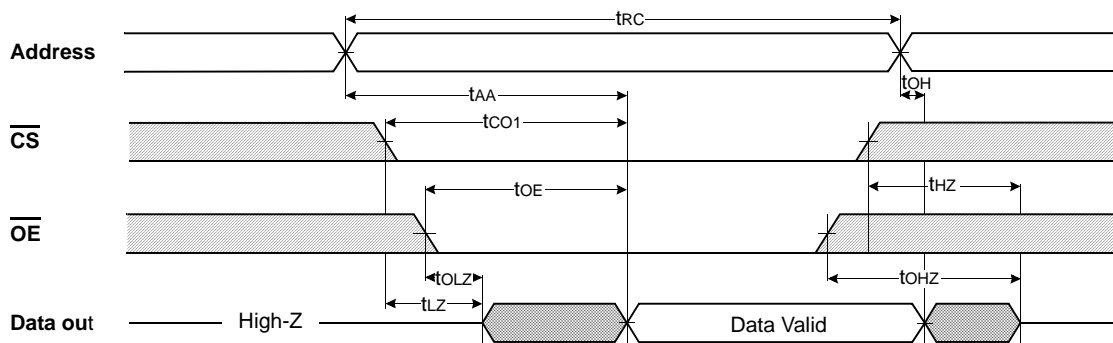
Item	Symbol	Test Condition	Min	Typ	Max	Unit
V <sub>CC</sub> for data retention	V <sub>DR</sub>	$\overline{CS} \geq V_{CC}-0.2\text{V}$	2.0	-	5.5	V
Data retention current	I <sub>DR</sub>	$V_{CC}=3.0\text{V}, \overline{CS} \geq V_{CC}-0.2\text{V}$	-	-	12	$\mu\text{A}$
					12	
					30	
Data retention set-up time	t <sub>SDR</sub>	See data retention waveform	0	-	-	ms
Recovery time	t <sub>RDR</sub>		5	-	-	

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ )



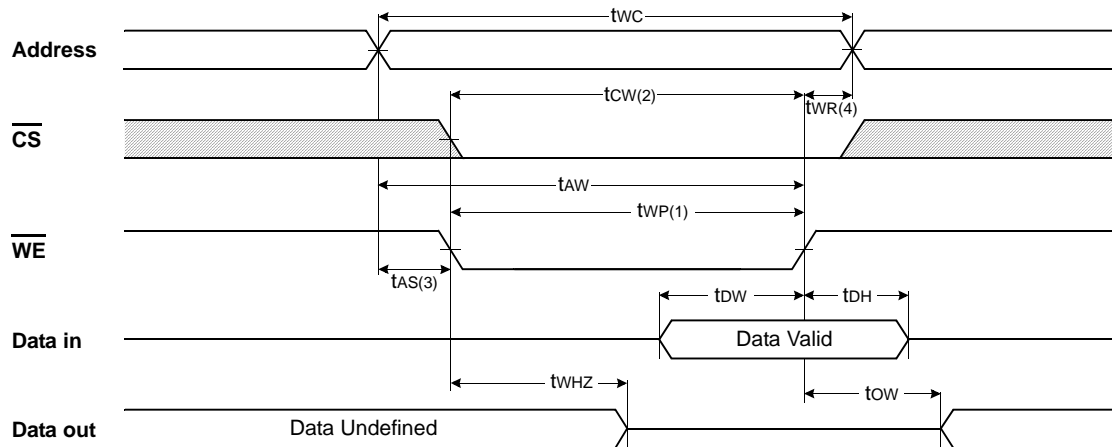
TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE}=V_{IH}$ )



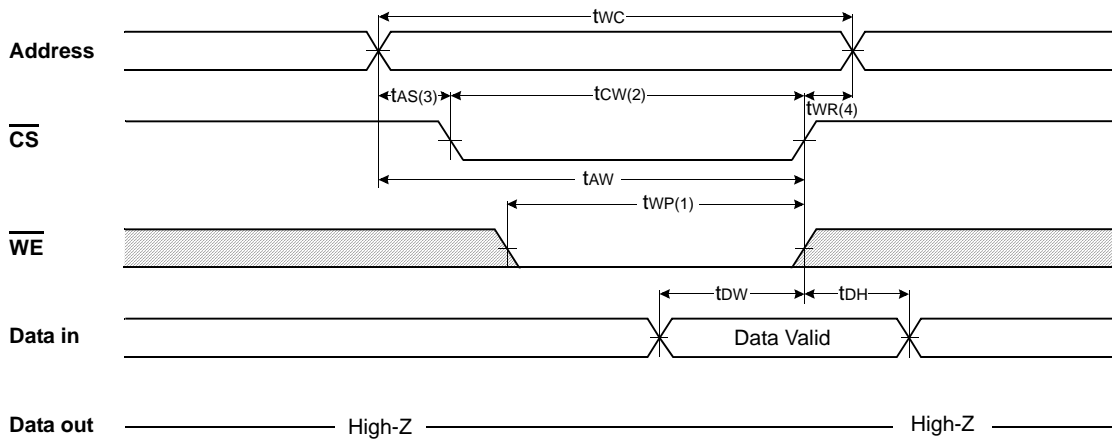
NOTES (READ CYCLE)

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

## TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$ Controlled)



## TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS}$ Controlled)

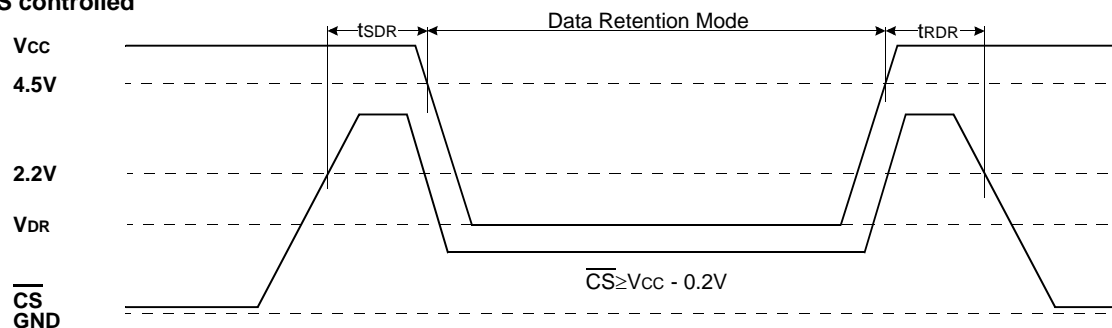


### NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}$  going Low and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CS}$  going high and  $\overline{WE}$  going high,  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}$  going low to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  is applied in case a write ends with  $\overline{CS}$  or  $\overline{WE}$  going high.

## DATA RETENTION WAVE FORM

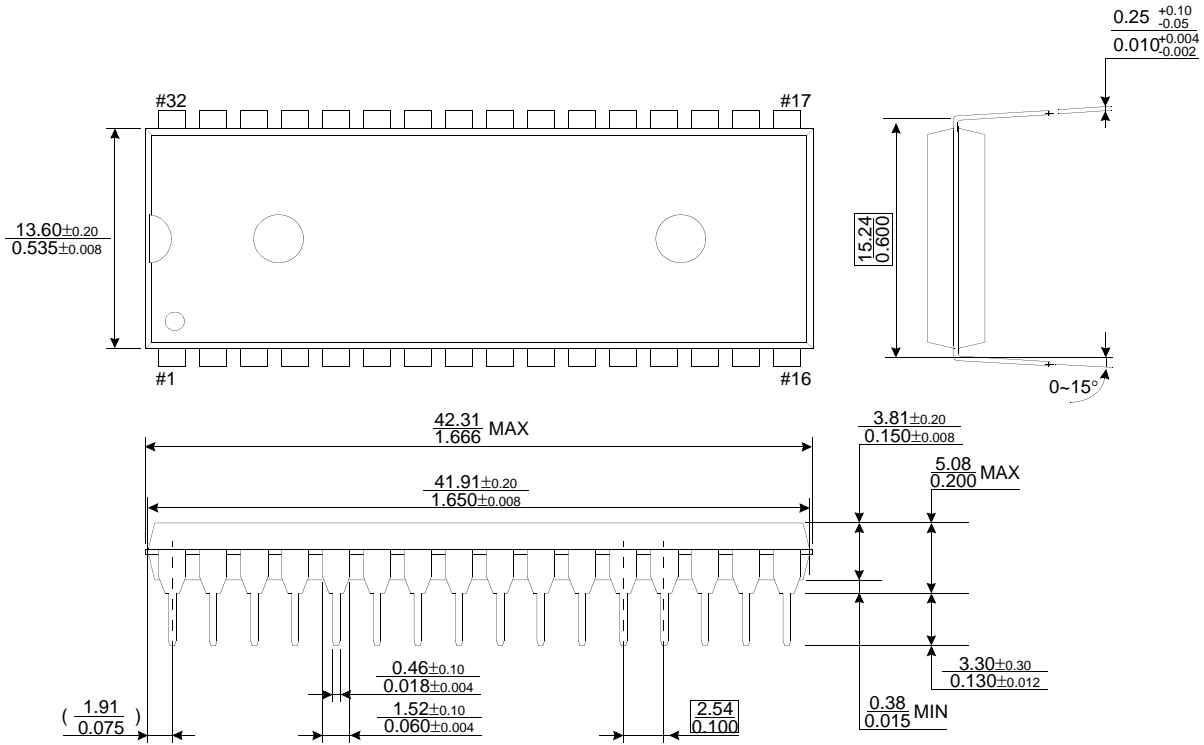
### $\overline{CS}$ controlled



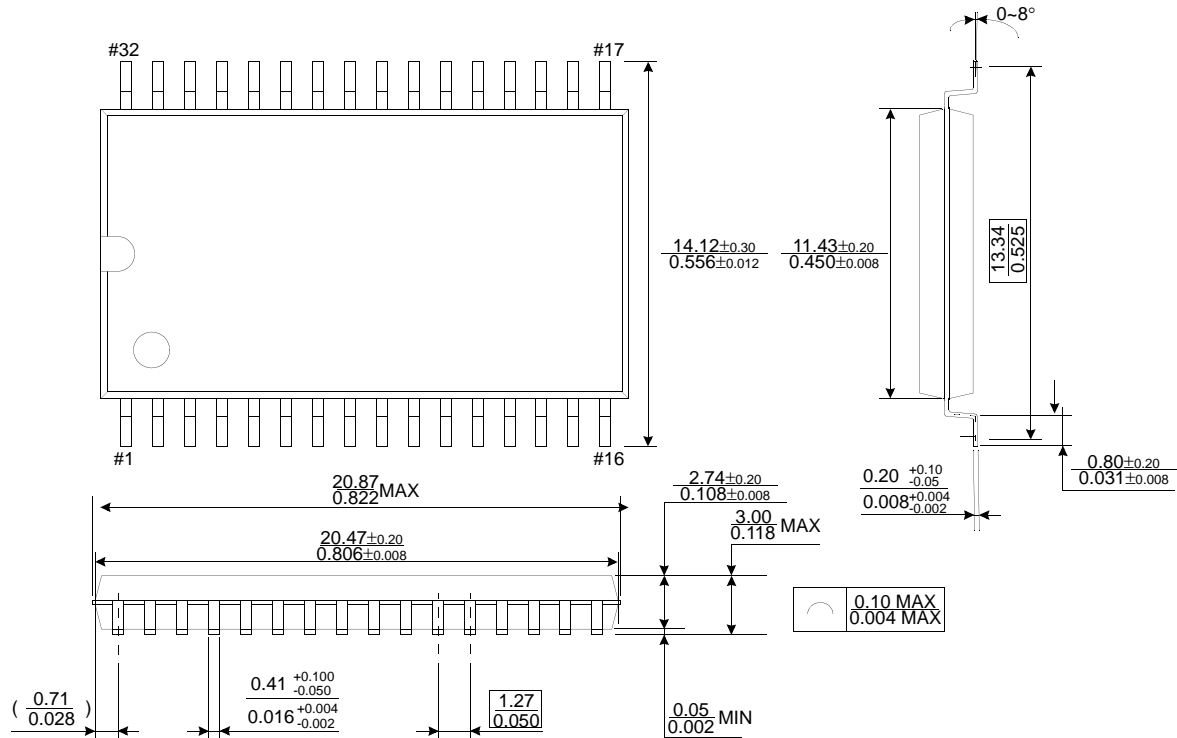
## PACKAGE DIMENSIONS

Units : millimeter(Inch)

### 32 PIN DUAL INLINE PACKAGE (600mil)



### 32 PIN PLASTIC SMALL OUTLINE PACKAGE (525mil)

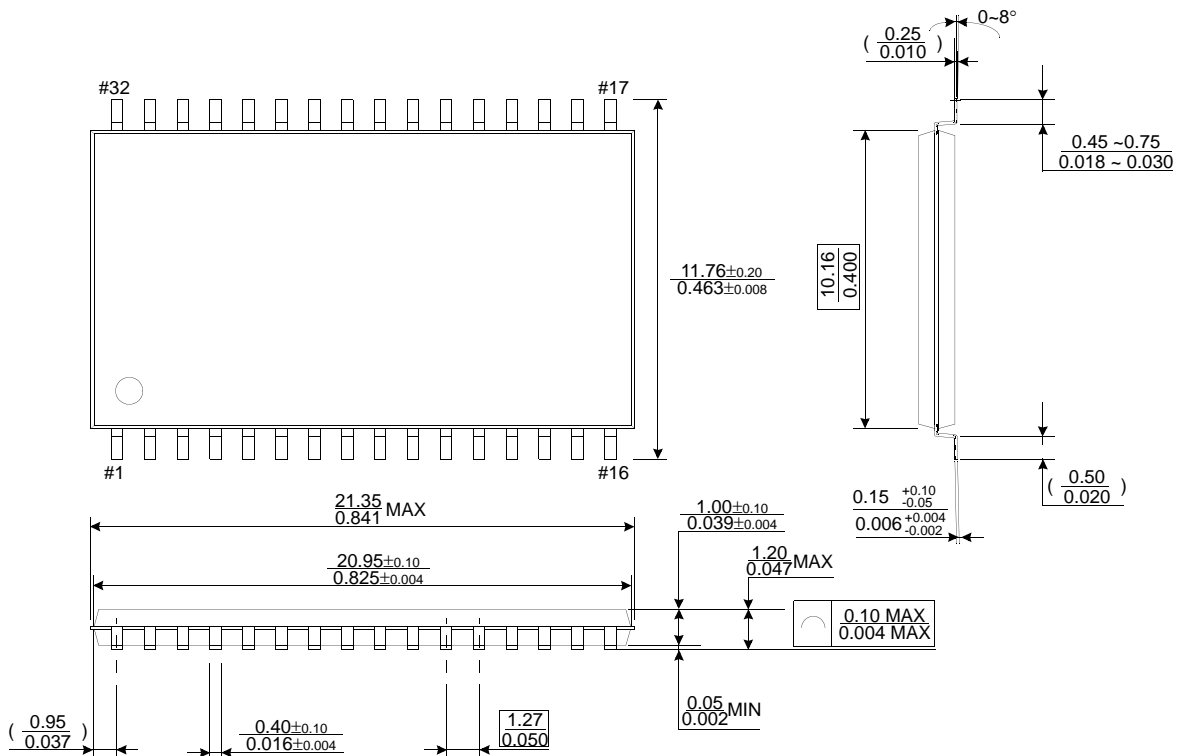




## PACKAGE DIMENSIONS

Units : millimeter(Inch)

### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)



### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400R)

