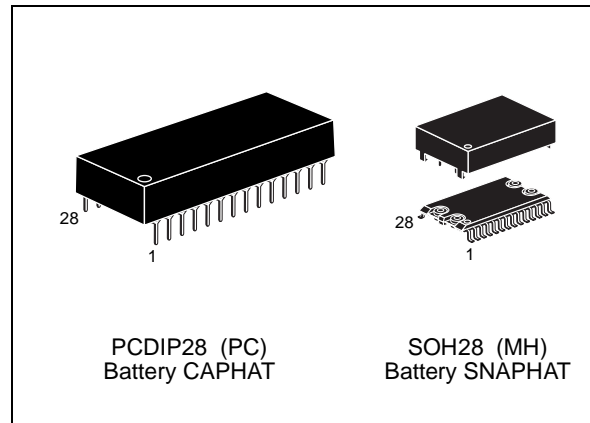


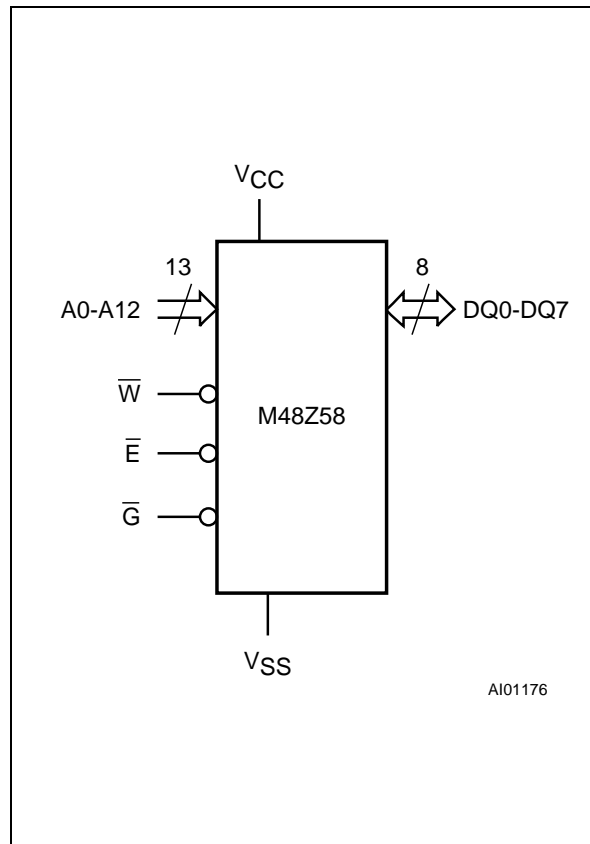
CMOS 8K x 8 ZEROPOWER SRAM

DATA BRIEFING

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
 - M48Z58: $4.5V \leq V_{PFD} \leq 4.75V$
 - M48Z58Y: $4.2V \leq V_{PFD} \leq 4.5V$
- SELF CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY
- SNAPHAT HOUSING (BATTERY) REPLACEABLE
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 8K x 8 SRAMs



Logic Diagram

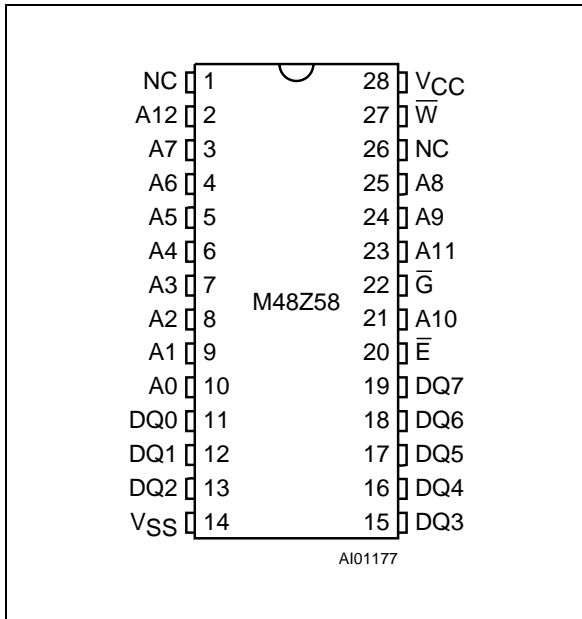


DESCRIPTION

The M48Z58 ZEROPOWER[®] RAM is an 8K x 8 non-volatile static RAM that integrates power-fail deselect circuitry and battery control logic on a single die. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory solution.

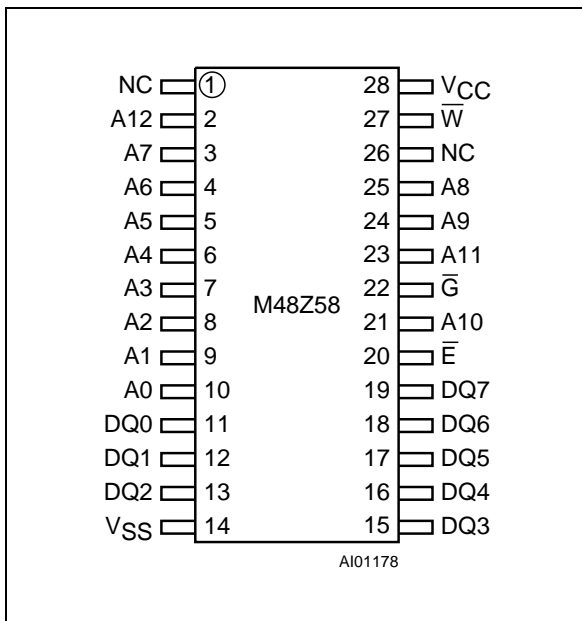
The M48Z58 is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

DIP Pin Connections



Warning: NC = Not Connected

SO Pin Connections



Warning: NC = Not Connected

Signal Names

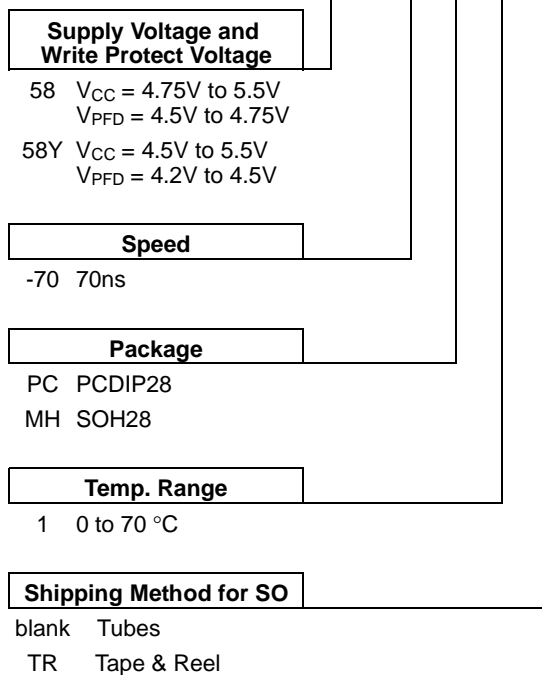
A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
\bar{E}	Chip Enable
\bar{G}	Output Enable
\bar{W}	Write Enable
V _{CC}	Supply Voltage
V _{SS}	Ground

Ordering Information Scheme

For a list of available options refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

Example: M48Z58Y -70 MH 1 TR



Note: The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4Z28-BR00SH1".