Fast Infrared Transceiver Module Family (FIR, 4 Mbit/s) for 2.6 V to 5.5 V Operation

Description

The TFDU6102E, TFDS6402, TFDS6502E, TFDT6502E are a family of low–power infrared transceiver modules compliant to the IrDA physical layer standard for fast infrared data communication, supporting IrDA speeds up to 4.0 Mbit/s (FIR), HP-SIR, Sharp ASK and carrier based remote control modes up to 2 MHz. Integrated within the transceiver modules are a photo PIN diode, an infrared emitter (IRED), and a low–power CMOS control IC to provide a total front–end solution in a single package.

Vishay Telefunken's FIR transceivers are available in four package options, including our Baby Face package (TFDU610xE), the standard setting, once smallest FIR transceiver available on the market. This wide selection provides flexibility for a variety of applications and space constraints. The transceivers are capable of directly interfacing with a wide variety of I/O devices which perform the modulation/ demodulation function, including National Semiconductor's PC87338, PC87108 and PC87109, SMC's FDC37C669, FDC37N769 and CAM35C44, and Hitachi's SH3. At a minimum, a current–limiting resistor in series with the infrared emitter and a V_{CC} bypass capacitor are the only external components required implementing a complete solution.

Features

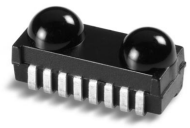
- Compliant to the IrDA physical layer specification (Up to 4 Mbit/s), HP–SIR®, Sharp ASK® and TV Remote Control
- For 3.0 V and 5.0 V Applications
- Operates from 2.6 V to 5.5 V within specification, operational down to 2.4 V
- Low Power Consumption (3 mA Supply Current)
- Power Shutdown Mode (1 μA Shutdown Current)
- Four Surface Mount Package Options
  - Universal ($9.7 \times 4.7 \times 4.0$ mm)
  - Side View ($13.0 \times 5.95 \times 5.3$ mm)
  - Top View ($13.0 \times 7.6 \times 5.95$ mm)
  - Dracula ($11.2 \times 5.6 \times 2.2$ mm)
- Push-Pull-Receiver Output, grounded in shutdown mode
- High Efficiency Emitter
- Baby Face (Universal) Package Capable of Surface Mount Soldering to Side and Top View Orientation
- Directly Interfaces with Various Super I/O and Controller Devices
- Built–In EMI Protection – No External Shielding Necessary
- Few External Components Required
- Backward Pin to Pin Compatible to all Vishay Telefunken SIR and FIR Infrared Transceivers
- Split power supply, transmitter and receiver can be operated from two power supplies with relaxed requirements, thus saving costs

Applications

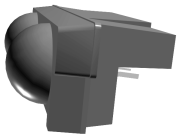
- Notebook Computers, Desktop PCs, Palmtop Computers (Win CE, Palm PC), PDAs
- Digital Still and Video Cameras
- Printers, Fax Machines, Photocopiers, Screen Projectors
- Telecommunication Products (Cellular Phones, Pagers)
- Internet TV Boxes, Video Conferencing Systems
- External Infrared Adapters (Dongles)
- Medical and Industrial Data Collection Devices

Package Options

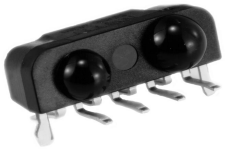
TFDU6102E
Baby Face (Universal)
weight 0.20 g



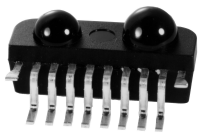
TFDS6402
Dracula Side View
weight 0.30 g



TFDS6502E
Side View
weight 0.39 g



TFDT6502E
Top View
weight 0.39 g



Ordering Information

Part Number	Qty / Reel	Description
TFDU6102E–TR3	1000 pcs	Oriented in carrier tape for side view surface mounting
TFDU6102E–TT3	1000 pcs	Oriented in carrier tape for top view surface mounting
TFDS6402–TR3	1000 pcs	Side View
TFDS6502E–TR3	750 pcs	Side View
TFDT6502E–TR3	750 pcs	Top View

Functional Block Diagram

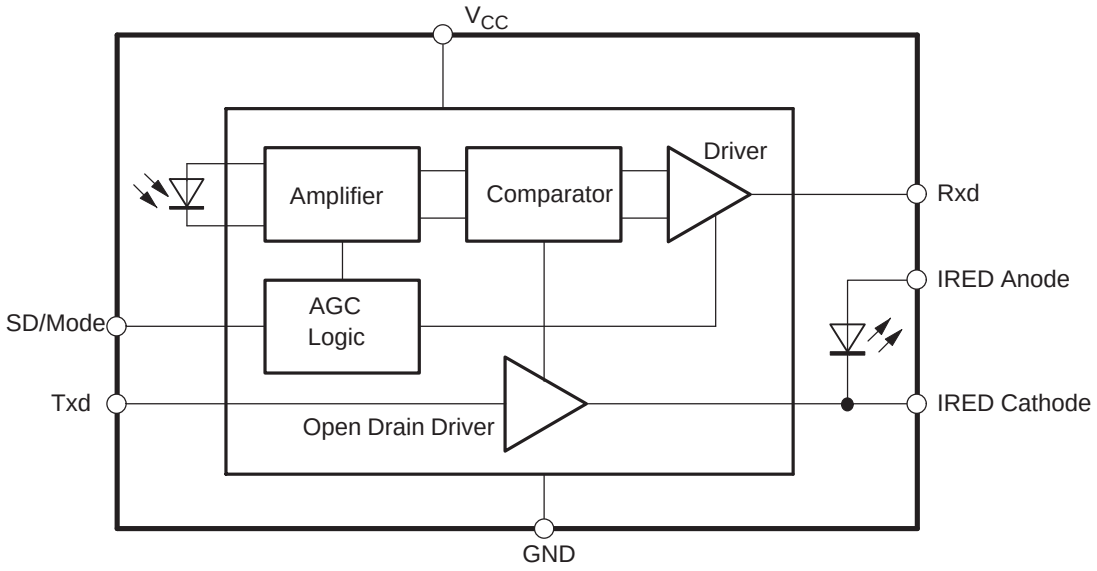
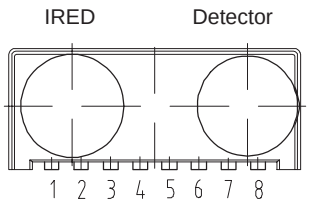


Figure 1. Functional Block Diagram

Pin Description

Pin Number		Function	Description	I/O	Active
"U" and "T" Option	"S" Option				
1	8	IRED Anode	IRED anode, to be externally connected to V_{CC} through a current control resistor. This pin is allowed to be supplied from an uncontrolled power supply separated from the controlled V_{CC} supply		
2	1	IRED Cathode	IRED cathode, internally connected to driver transistor		
3	7	Txd	Transmit Data Input	I	HIGH
4	2	Rxd	Received Data Output, push-pull CMOS driver output capable of driving a standard CMOS or TTL load. No external pull-up or pull-down resistor is required. **Pin is floating when device is in shutdown mode**	O	LOW
5	6	SD/Mode	Shutdown/ Mode	I	HIGH
6	3	V_{CC}	Supply Voltage		
7	5	Mode	HIGH: High speed mode; LOW: Low speed mode, SIR only (see chapter "Mode Switching")	I	
8	4	GND	Ground		

"U" Option Baby Face (Universal) and Dracula



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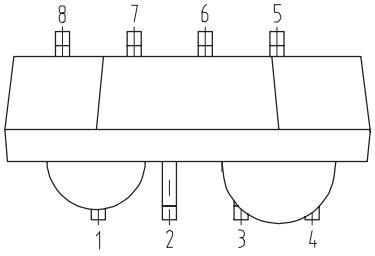
"S" Option Side View



"T" Option Top View

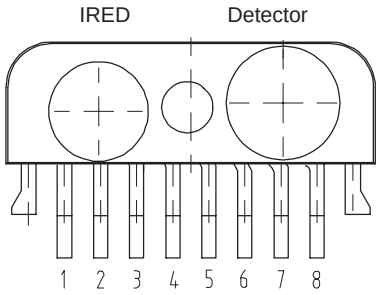


Figure 2. Pinnings

Absolute Maximum Ratings

Reference point Pin: GND unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage Range, Transceiver	0 V <V_{CC2} <6 V	V_{CC1}	– 0.5		6	V
Supply Voltage Range, Transmitter	0 V <V_{CC1} <6 V	V_{CC2}	– 0.5		6	V
Input Currents	For all Pins, Except IRED Anode Pin				10	mA
Output Sinking Current					25	mA
Power Dissipation	See Derating Curve	P_D			350	mW
Junction Temperature		T_J			125	°C
Ambient Temperature Range (Operating)		T_{amb}	–25		+85	°C
Storage Temperature Range		T_{stg}	–25		+85	°C
Soldering Temperature	See Recommended Solder Profile (see Figure 11)				240	°C
Average Output Current		I_{IRED} (DC)			130	mA
Repetitive Pulsed Output Current	<90 µs, t_{on} <20%	I_{IRED} (RP)			600	mA
IRED Anode Voltage		V_{IREDA}	– 0.5		6	V
Transmitter Data Input Voltage		V_{Txd}	– 0.5		V_{CC1} +0.5	V
Receiver Data Output Voltage		V_{Rxd}	– 0.5		V_{CC1} +0.5	V
Virtual Source Size	Method: (1–1/e) encircled energy	d	2.5	2.8		mm
Maximum Intensity for Class 1 Operation of IEC825–1 or EN60825–1 (worst case IrDA FIR pulse pattern)	EN60825, 1997, unidirectional operation, worst case test mode				320	mW/sr

Electrical Characteristics

T_{amb} = 25°C, V_{CC} = 2.6V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Transceiver						
Supply Voltage		V_{CC}	2.6		5.5	V
Dynamic Supply Current	Receive mode only. In transmit mode, add additional 85 mA (typ) for IRED current					
	SD = Low, E_e = 0 klx	I_{CC}		3	4.5	mA
	SD = Low, E_e = 1 klx *)	I_{CC}		3	4.5	mA
Standby Supply Current	SD = High, Mode = Floating, T = 25°C, E_e = 0 klx T = 25°C, E_e = 1 klx *)	I_{SD}			 1 1.5	 µA µA
	SD = High, T = 85°C, Mode = Floating, Not Ambient Light Sensitive	I_{SD}			5	µA
Operating Temperature Range		T_A	–25		+85	°C
Output Voltage Low	R_{load} = 2.2 kΩ, C_{load} = 15 pF	V_{OL}		0.5	0.8	V
Output Voltage High	R_{load} = 2.2 kΩ, C_{load} = 15 pF	V_{OH}	V_{CC}–0.5			V
Input Voltage Low (Txd, SD/ Mode, Mode)		V_{IL}	0		0.8	V
Input Voltage High (Txd, SD/ Mode, Mode)	CMOS level **)	V_{IH}	0.9 x V_{CC}			V
	TTL level, $V_{CC} \geq$ 4.5 V	V_{IH}	2.4			V
Input Leakage Current (Txd, SD/ Mode)		I_L	–10		+10	µA
Input Leakage Current, Mode		I_L	–80		+80	µA
Input Capacitance		C_I			5	pF

*) Standard Illuminant A
**) The typical threshold level is between 0.5 x $V_{CC/2}$ (V_{CC} = 3 V) and 0.4 x V_{CC} (V_{CC} = 5.5 V) .
It is recommended to use the specified min/ max values to avoid increased operating current.

Optoelectronic Characteristics

T_{amb} = 25°C, V_{CC} = 2.6 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Receiver						
Minimum Detection Threshold Irradiance, SIR Mode	TFDS6502E/ TFDT6502E 9.6 kbit/s to 115.2 kbit/s λ = 850 nm to 900 nm	E_e		20	35	mW/m^2
	TFDU6102E, TFDS6402 9.6 kbit/s to 115.2 kbit/s λ = 850 nm to 900 nm	E_e		25	40	mW/m^2
Minimum Detection Threshold Irradiance, MIR Mode	TFDS6502E/ TFDT6502E 1.152 Mbit/s λ = 850 nm to 900 nm	E_e		50		mW/m^2
	TFDU6102E, TFDS6402 1.152 Mbit/s λ = 850 nm to 900 nm	E_e		65		mW/m^2
Minimum Detection Threshold Irradiance, FIR Mode	TFDS6502E/ TFDT6502E 4.0 Mbit/s λ = 850 nm to 900 nm	E_e		65	100	mW/m^2
	TFDU6102E, TFDS6402 4.0 Mbit/s λ = 850 nm to 900 nm	E_e		85	100	mW/m^2
Maximum Detection Threshold Irradiance	λ = 850 nm to 900 nm	E_e	5	10		kW/m^2
Logic LOW Receiver Input Irradiance		E_e	4			mW/m^2
Rise Time of Output Signal—,,,,klll	10% to 90%, @2.2 kΩ, 15 pF	$t_{r\ (Rxd)}$	10		40	ns
Fall Time of Output Signal	90% to 10%, @2.2 kΩ, 15 pF	$t_{f\ (Rxd)}$	10		40	ns
Rxd Pulse Width of Output Signal, 50% SIR Mode	Input pulse length 20 µs, 9.6 kbit/s	t_{PW}	1.2	10	20	µs
	Input pulse length 1.41 µs, 115.2 kbit/s	t_{PW}	1.2		1/2 bit length	µs
Rxd Pulse Width of Output Signal, 50% MIR Mode	Input pulse length 217 ns, 1.152 Mbit/s	t_{PW}	110		260	ns
Rxd Pulse Width of Output Signal, 50% FIR Mode	Input pulse length 125 ns, 4.0 Mbit/s	t_{PW}	100		160	ns
	Input pulse length 250 ns, 4.0 Mbit/s	t_{PW}	200		290	ns
Stochastic Jitter, Leading Edge, FIR Mode	Input Irradiance = 100 mW/m^2, 4.0 Mbit/s			±10		ns
Latency		t_L		120	300	µs

Optoelectronic Characteristics (continued)

T_{amb} = 25°C, V_{CC} = 2.6 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Transmitter						
IRED Operating Current	R1*) = 7.2 Ω, V_{CC} = 5.0 V	I_D		0.4	0.55	A
Output Radiant Intensity (see Figure 3)	V_{CC} = 5.0 V, α = 0°, 15° Txd = High, SD = Low, R1 = 7.2 Ω	I_e	120	170	350	mW/sr
Output Radiant Intensity	V_{CC} = 5.0 V, α = 0°, 15° Txd = Low, SD = High, (Receiver is inactive as long as SD = High) R1 = 7.2 Ω	I_e			0.04	mW/sr
Output Radiant Intensity, Angle of Half Intensity		α		±24		°
Peak – Emission Wavelength		λ_P	880		900	nm
Optical Output Pulse Duration	Input pulse width 217 ns, 1.152 Mbit/s	t_{opt}	207	217	227	ns
	Input pulse width 125 ns, 4 Mbit/s	t_{opt}	117	125	133	ns
	Input pulse width 250 ns, 4 Mbit/s	t_{opt}	242	250	258	ns
	Input pulse width t < 80 µs Input pulse width t ≥ 80 µs	t_{opt}		t 	 80	µs
Optical Rise Time, Fall Time		t_{ropt}, t_{fopt}	10		40	ns
Optical Overshoot					10	%

*) R1: control series resistor for current limitation

Recommended Circuit Diagram

The only required component for designing an IrDA 1.3 solution using Vishay Telefunken transceivers is a current limiting resistor, R1, to the IRED. However, depending on the entire system design and board layout, additional components may be required (see figure 3).

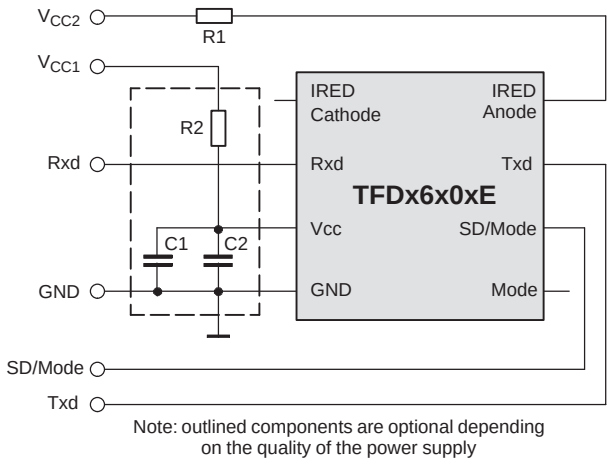


Figure 3. Recommended Application Circuit

Vishay Telefunken transceivers integrate a sensitive receiver and a built-in power driver. The combination of both needs a careful circuit board layout. The use of thin, long, resistive and inductive wiring should be avoided. The inputs (Txd, SD/ Mode) and the output Rxd should be directly (DC) coupled to the I/O circuit.

R1 is used for controlling the current through the IR emitter. For increasing the output power of the IRED, the value of the resistor should be reduced. Similarly, to reduce the output power of the IRED, the value of the resistor should be increased. For typical values of R1 see figure 4. For IrDA compliant operation, a current control resistor of 7.2 Ω is recommended. For compensating losses of the cosmetic window, reducing that value to 5.6 Ω is acceptable. The upper drive current limitation is dependent on the duty cycle and is given by the absolute maximum ratings on the data sheet.

R2, C1 and C2 are optional and dependent on the quality of the supply voltage V_{CC} and injected noise. An unstable power supply with dropping voltage during transmission may reduce sensitivity (and transmission range) of the transceiver.

The placement of these parts is critical. It is strongly recommended to position C2 as near as possible to the transceiver power supply pins. An electrolytic capacitor should be used for C1 while a ceramic capacitor is used for C2.

Table 1. Recommended Application Circuit Components

Component	Recommended Value	Vishay Part Number
C1	4.7 µF, Tantalum	293D 475X9 016B 2T
C2	0.1 µF, Ceramic	VJ 1206 Y 104 J XXMT
R1	5 V supply voltage: 7.2 Ω , 0.25 W (recommend using two 3.6 Ω, 0.125 W resistors in series) 3.3 V supply voltage: 3.6 Ω , 0.25 W (recommend using two 1.8 Ω, 0.125 W resistors in series)	CRCW–1206–3R60–F–RT1 CRCW–1206–1R80–F–RT1
R2	47 Ω , 0.125 W	CRCW–1206–47R0–F–RT1

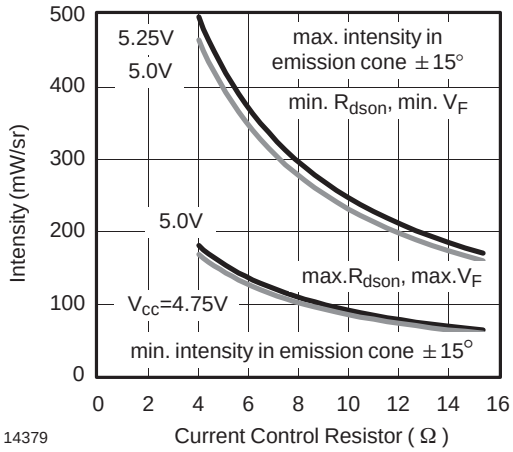


Figure 4. Intensity I_e vs. Current Control Resistor R1, 5 V Applications

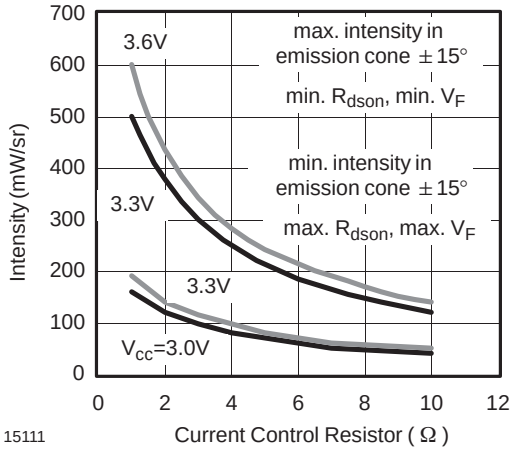


Figure 5. Intensity I_e vs. Current Control Resistor R1, 3 V Applications

In addition, when connecting the described circuit to the power supply, low impedance wiring should be used.

I/O and Software

In the description, already different I/Os are mentioned. Differnt combinations are tested and the function verified with the special drivers available from the I/O suppliers. In special cases refer to the I/O manual, the Vishay application notes, or contact directly Vishay Sales, Marketing or Application.

Control: Differences to TFDx6000 Series

For applications using I/Os from NSC, Winbond and TI no software upgrade is necessary. In combination with the latest SMSC controllers for Microsoft Windows 98® a software upgrade is necessary, drivers are available from SMSC and Vishay Semiconductor GmbH. This software is intended to work with Windows 95®, too. Alternatively the HP/ Sharp settings can be selected. The Microsoft Operating Systems NT 5.0® Beta 2 and Windows 2000® provide Miniport device drivers.

Mode Switching

The TFDU6102E, TFDS6402, TFDS6502E and TFDT6502E do not power on with a default mode, therefore the data transfer rate has to be set by a programming sequence using the Txd and SD/ Mode inputs as described below or selected by setting the Mode Pin. The Mode Pin can be used to statically set the mode (Mode Pin: LOW: SIR, HIGH: 0.576 Mbit/s to 4.0 Mbit/s). When using the Mode Pin, the standby current may increase to about 50 to 60 µA when high or low. If not used or in standby mode, the mode input should float to minimize standby current. The low frequency mode covers speeds up to 115.2 kbit/s. Signals with higher data rates should be detected in the high frequency mode. Lower frequency data can also be received in the high frequency mode but with reduced sensitivity. To switch the transceivers from low frequency mode to the high frequency mode and vice versa, the programming sequences described below are required.

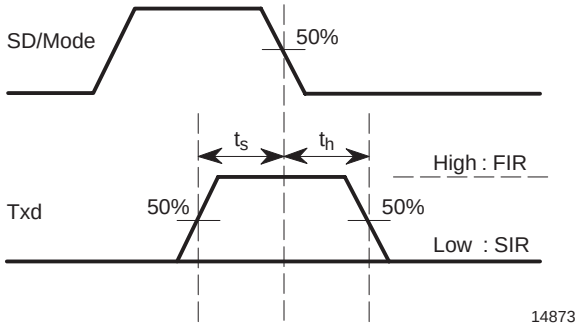


Figure 6. Mode Switching Timing Diagram

Setting to the High Bandwidth Mode (0.576 Mbit/s to 4.0 Mbit/s)

1. Set SD/MODE input to logic “HIGH”.
2. Set Txd input to logic “HIGH”. Wait $t_s \geq 200$ ns.
3. Set SD/MODE to logic “LOW” (this negative edge latches state of Txd, which determines speed setting).
4. After waiting $t_h \geq 200$ ns Txd can be set to logic “LOW”. The hold time of Txd is limited by the maximum allowed pulse length.

Txd is now enabled as normal Txd input for the high bandwidth mode.

Setting to the Lower Bandwidth Mode (2.4 kbit/s to 115.2 kbit/s)

1. Set SD/MODE input to logic “HIGH”.
2. Set Txd input to logic “LOW”. Wait $t_s \geq 200$ ns.
3. Set SD/MODE to logic “LOW” (this negative edge latches state of Txd, which determines speed setting).
4. Txd must be held for $t_h \geq 200$ ns.

Txd is now enabled as normal Txd input for the lower bandwidth mode.

Recommended SMD Pad Layout

The leads of the device should be soldered in the center position of the pads.

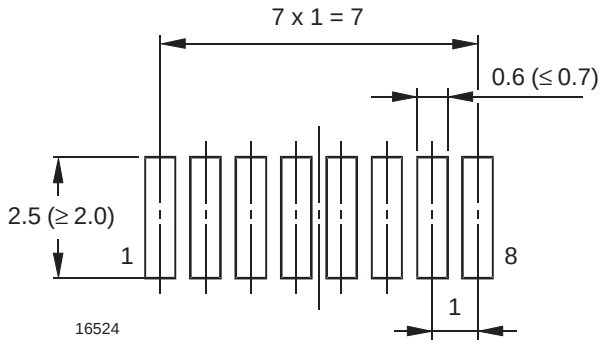


Figure 7. TFDU6102E BabyFace (Universal)

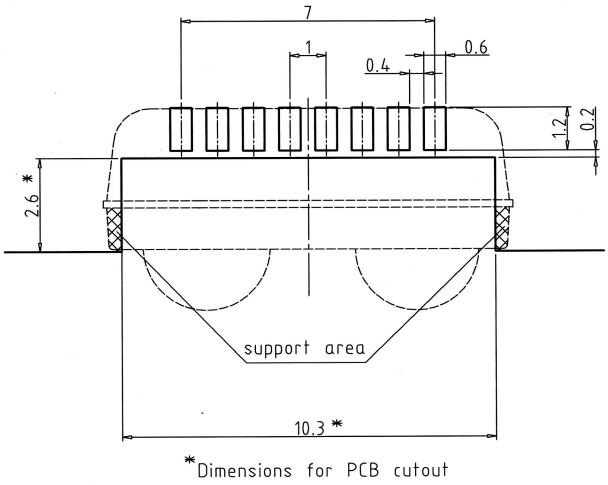


Figure 8. TFDS6402 (Dracula)

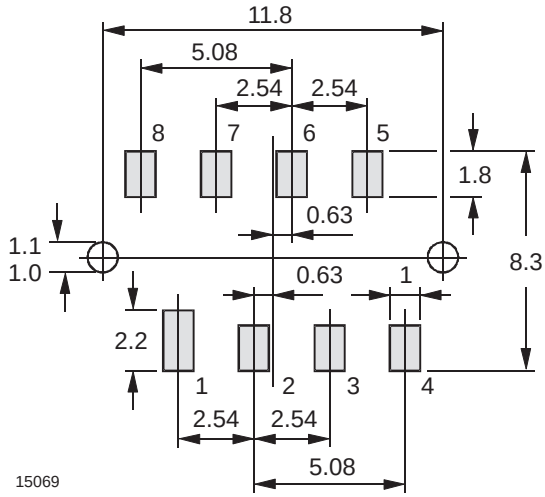


Figure 9. TFDS6502E Side View Package
Pad 1 is longer to designate Pin 1 connection to transceiver.

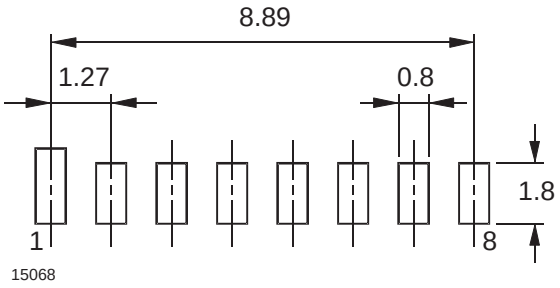


Figure 10. TFDT6502E Top View Package
Pad 1 is longer to designate Pin 1 connection to transceiver.

Note: Leads of the device should be at least 0.3 mm within the ends of the pads.

Recommended Solder Profile

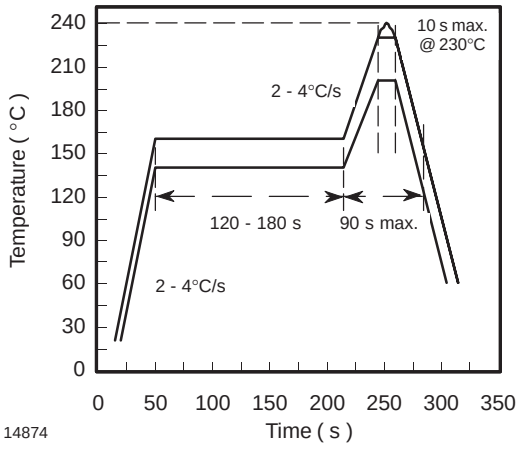


Figure 11. Recommended Solder Profile

Current Derating Diagram

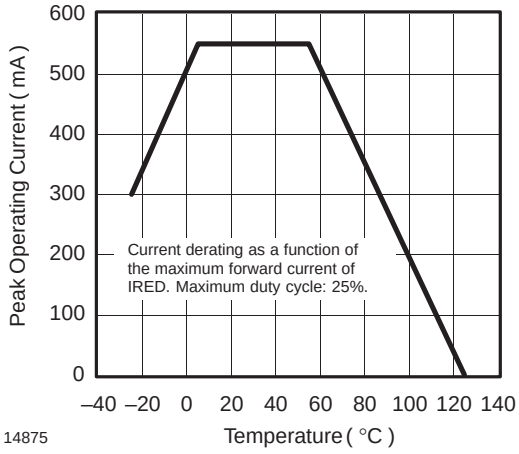
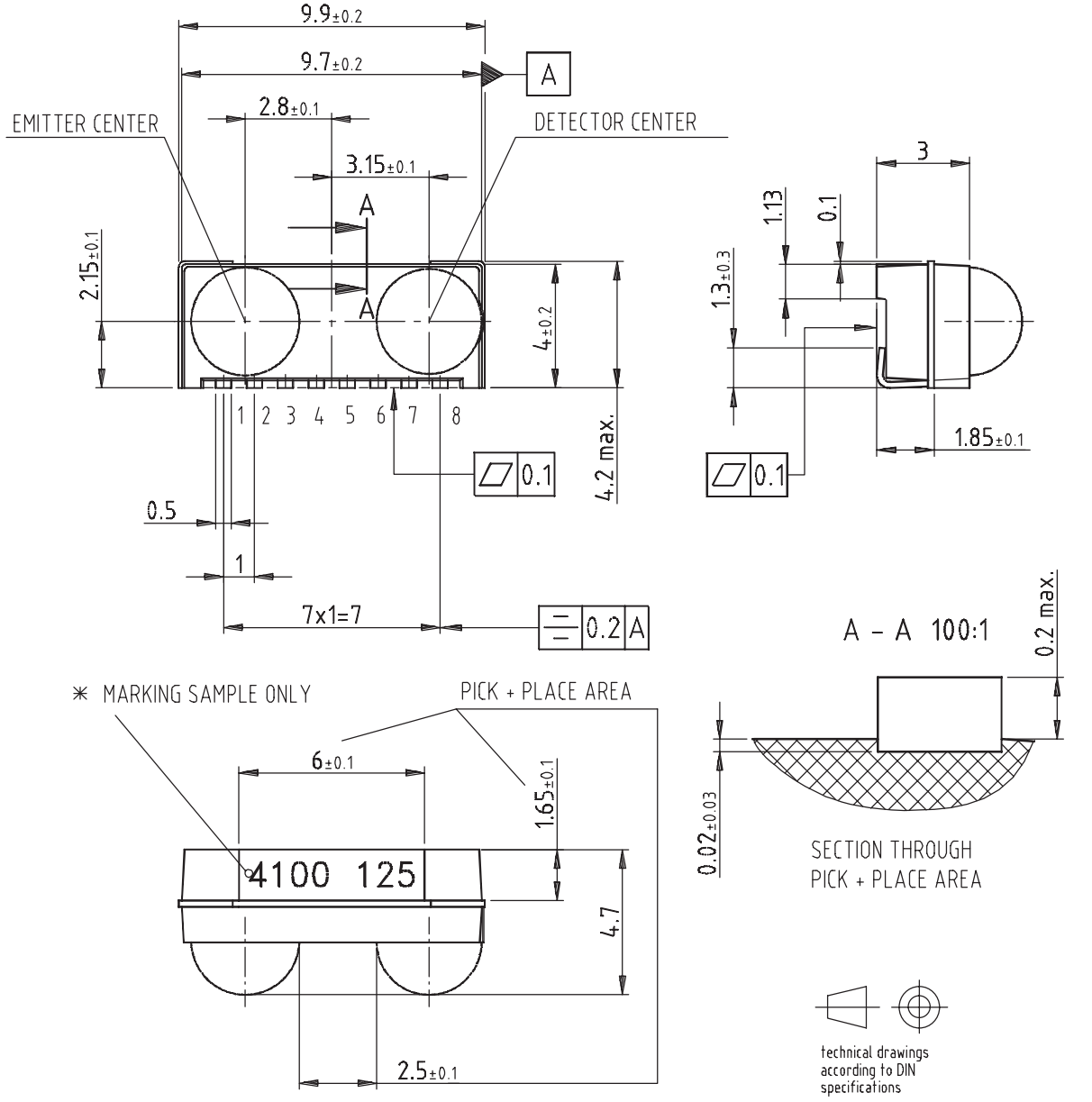


Figure 12. Current Derating Diagram

TFDU6102E – Baby Face (Universal) Package (Mechanical Dimensions)



✳ MARKING ORIENTATION
180 DEGREES ALLOWED

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Issue: 11; 29.01.01

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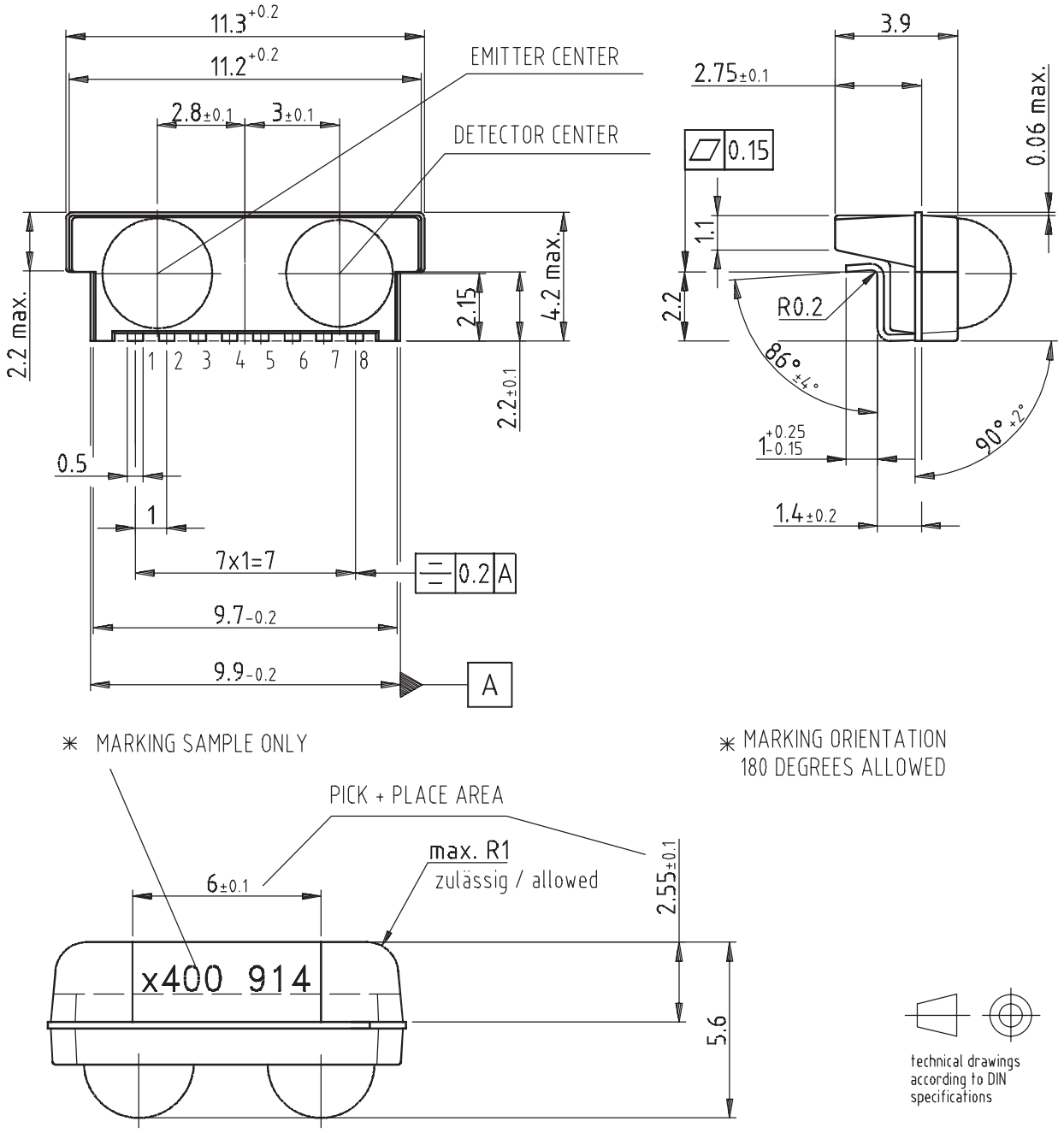
TFDS6402 Package (Mechanical Dimensions)



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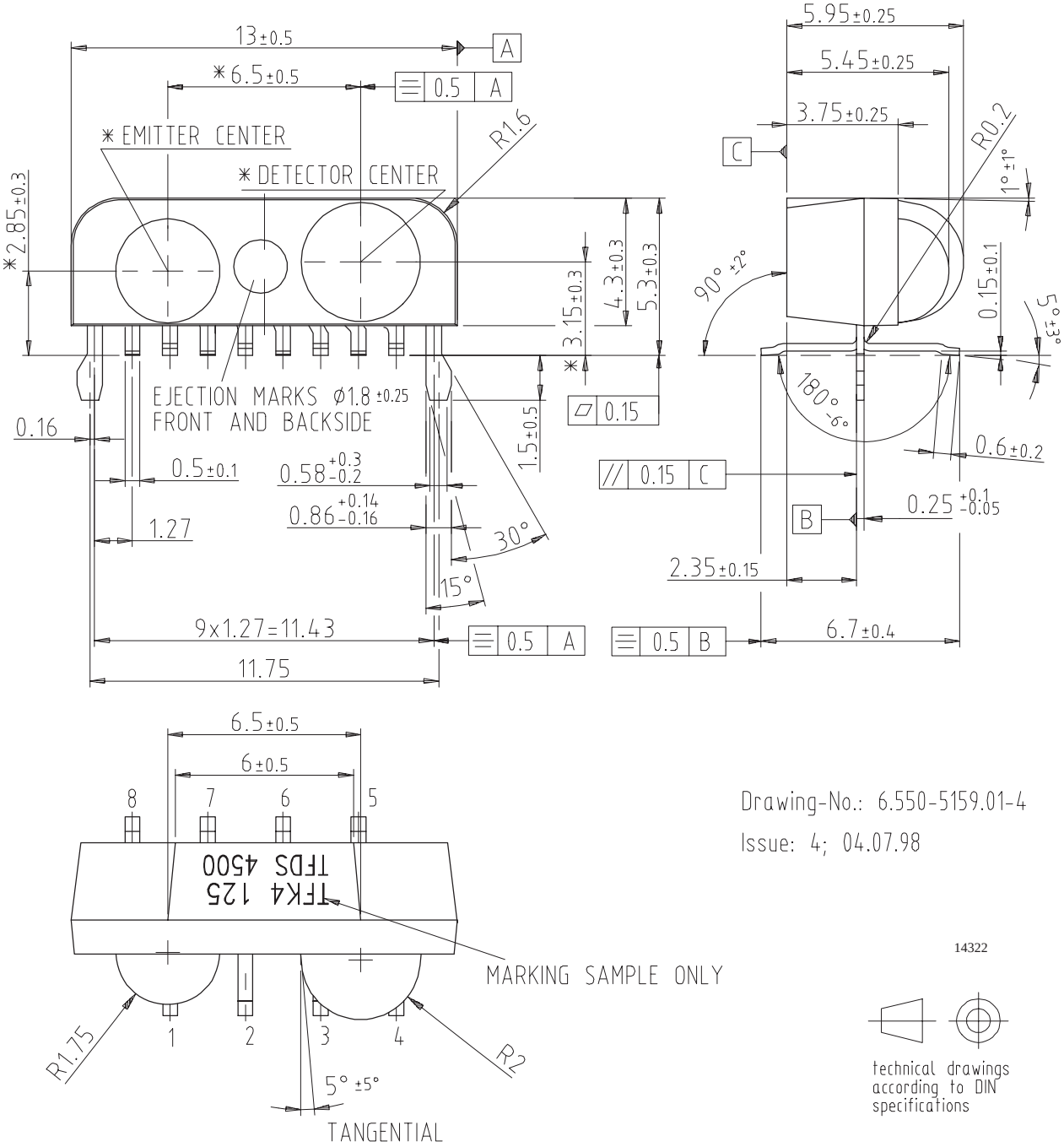
TFDS6502E – Side View Package (Mechanical Dimensions)



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Issue: 4; 04.07.98

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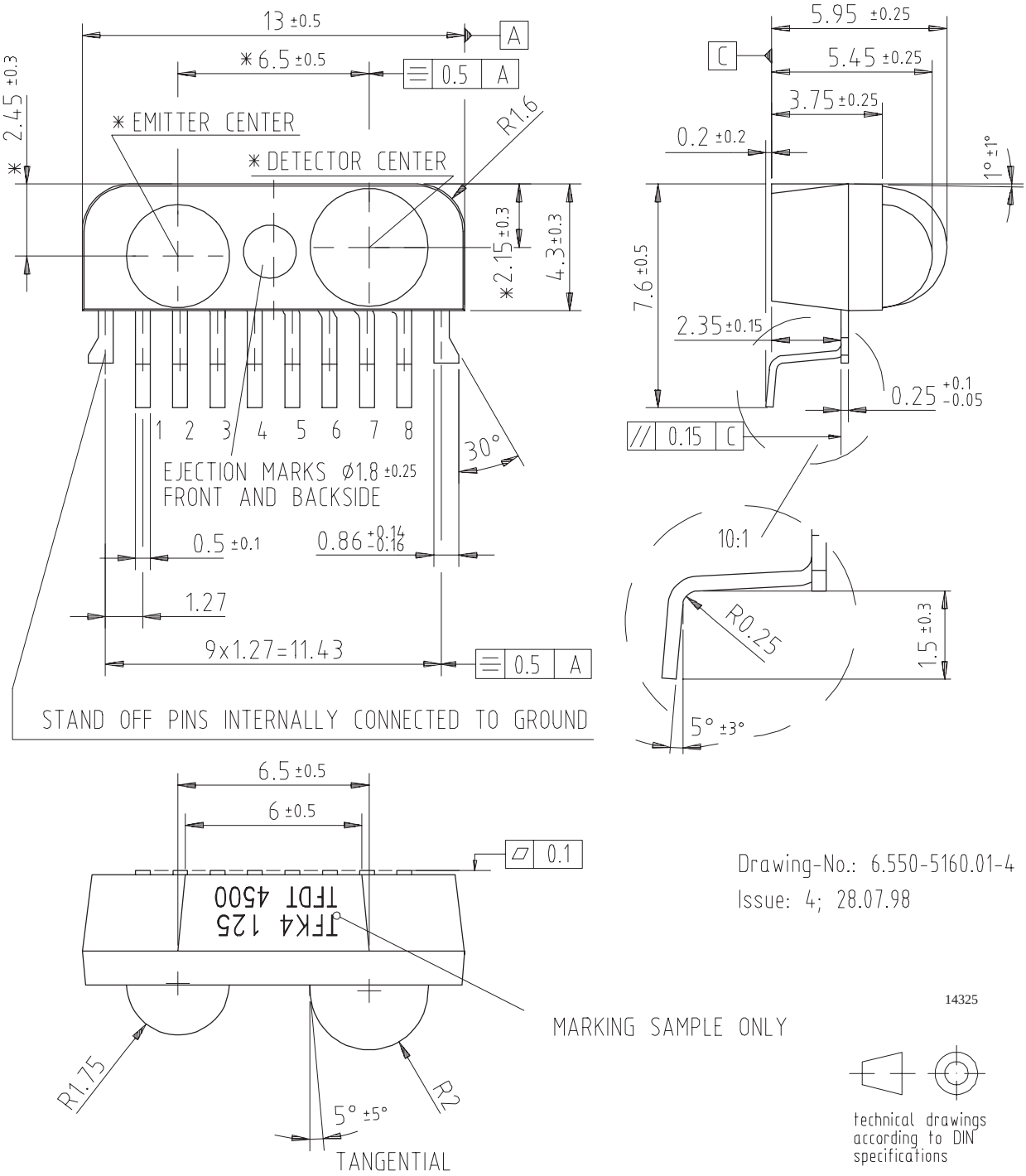
technical drawings
according to DIN
specifications

TFDT6502E – Top View Package (Mechanical Dimensions)



Drawing-No.: 6.550-5160.01-4
Issue: 4; 28.07.98

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Revision History:

B1.1, 01/03/1999: New edition for optimized E family. TFDxxx01E – RXD output is grounded when the device is switched to shutdown mode.

B1.2, 15/03/1999: A clean tri-state version with floating output in shutdown mode was added as 02 version. The output radiant intensity was increased.

B1.4a, 26/10/1999: TR3 changed to TR4 for 01 types, weight of packages added.

B1.4b, 22/11/1999: Max. operating current changed from 4.0 mA to 4.5 mA, Dracula package version added, some typos corrected.

B1.5, 13/10/2000: First typos corrected

B1.6, 02/11/2000: SMD pad layout tolerances added